PE43508

Document Category: Product Specification

UltraCMOS® RF Digital Step Attenuator, 9 kHz–55 GHz

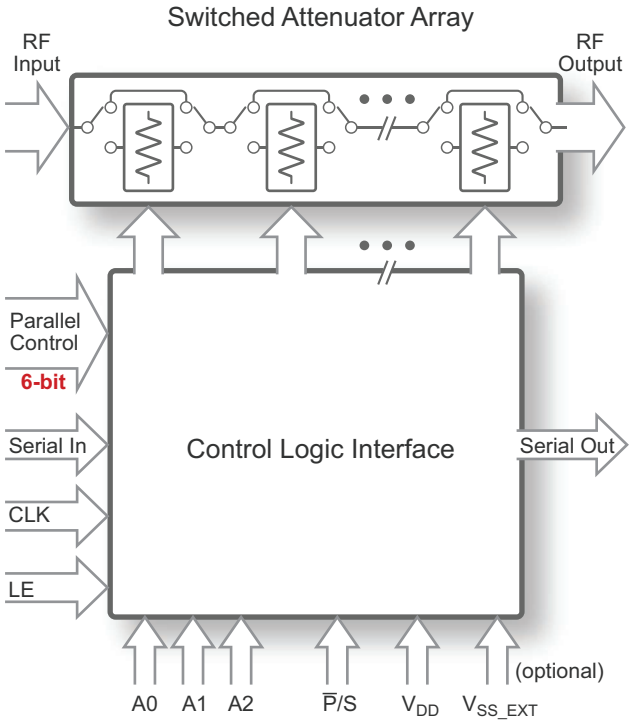
Features

- Wideband support up to 55 GHz
- Glitch-safe attenuation state transitions
- Flexible attenuation steps of 0.5 dB and 1 dB up to 31.5 dB
- Extended +105 °C operating temperature
- Parallel and serial programming interfaces with serial addressability
- Flip-chip die

Applications

- Test and measurement (T&M)
- Point-to-point communication systems
- Very small aperture terminals (VSAT)

Figure 1 ▪ PE43508 Functional Diagram



Product Description

The PE43508 is a 50Ω, HaRP™ technology-enhanced, 6-bit RF digital step attenuator (DSA) that supports a wide frequency range from 9k to 55 GHz. The PE43508 features glitch-safe attenuation state transitions, supports 1.8V control voltage and optional V_{SS_EXT} bypass mode to improve spurious performance, making this device ideal for test and measurement, point-to-point communication systems, and very small aperture terminals (VSAT).

The PE43508 provides an integrated digital control interface that supports both serial addressable and parallel programming of the attenuation. The PE43508 covers a 31.5 dB attenuation range in 0.5 dB and 1 dB steps. It is capable of maintaining 0.5 dB and 1 dB monotonicity through 55 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43508 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS} Control

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for the PE43508

Parameter/Condition	Min	Max	Unit
Positive supply voltage, V_{DD}	–0.3	5.5	V
Negative supply voltage, V_{SS_EXT}	–3.6	0.3	V
Digital input voltage	–0.3	3.6	V
Peak RF input power, 50Ω		**Fig. 7**	dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(*)		1000	V
Note: * Human body model (MIL–STD 883 Method 3015)			

Recommended Operating Conditions

Table 2 lists the recommending operating condition for the PE43508. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Condition for the PE43508

Parameter	Min	Typ	Max	Unit
Normal mode, V_{SS_EXT} = 0V(1)				
Positive supply voltage, V_{DD}	2.3	3.3	5.5	V
Positive supply current, I_{DD}(3)		170	250	µA
Bypass mode, V_{SS_EXT} = –3.0V(2)				
Positive supply voltage, V_{DD} (V_{DD} ≥ 3.4V. See Table 3 for full spec compliance.)	3.1	3.4	5.5	V
Positive supply current, I_{DD}(3)		122	166	µA
Negative supply voltage, V_{SS_EXT}	–3.3	–3.0	–2.7	V
Negative supply current, I_{SS}	-40	-16		µA
Normal or bypass mode				
Digital input high	1.17		3.60	V
Digital input low	–0.3		0.6	V
Digital input current(4)		10	20	µA
RF input power, CW(5) (7)			Fig. 7	dBm
RF input power, pulsed(6) (7)			Fig. 7	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: Connect V_{SS_EXT} (pin 15) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: Use V_{SS_EXT} (pin 15) to bypass and disable internal negative voltage generator.
3) Due to startup inrush current, a minimum current limit of 600 µA is allowed for normal operation of the DSA.
4) Applies to all pins except pins 10, 12, 19 and 20. $\overline{P}$/S (pin 10), A0/D4 (pin 12), A2/D6 (pin 19) and A1/D5 (pin 20) have internal 1.5 MΩ pull-up resistor to internal 1.8V V_{DD}.
5) 100% duty cycle, all bands, 50Ω.
6) ≤ 5% duty cycle, 50Ω.
7) The maximum peak envelope of any OFDM complex waveform signal, such as CP-OFDM, should not exceed the maximum peak RF input power in Table 1. The maximum average power of any complex waveform should not exceed the operating maximum RF input power, CW.

Electrical Specifications

Table 3 provides the PE43508 key electrical specifications at 25 °C, Z_S = Z_L = 50Ω, unless otherwise specified. Normal mode[1] is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode[2] is at V_{DD} = 3.4V and V_{SS_EXT} = –3.0V.

Table 3 ▪ PE43508 Electrical Specifications

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			9 kHz		55 GHz	As shown
Attenuation range	0.5 dB step 1 dB step			0–31.5 0–31.0		dB dB
Insertion loss		9.0 kHz–13.0 GHz 13.0–26.5 GHz 26.5–45.0 GHz 45.0–50.0 GHz 50.0–55.0 GHz		2.2 3.2 4.7 5.3 5.9	2.5 3.5 5.2 5.8 6.5	dB dB dB dB dB
Attenuation error	**0.5 dB step**					
	0–31.5 dB	9.0 kHz–13.0 GHz			+(1.00+4.5% of attenuation setting) / -1	dB
		13.0–26.5 GHz			+(1.15+4.5% of attenuation setting) / -1	dB
		26.5–45.0 GHz			+(1.60+8.5% of attenuation setting) / -1	dB
		45.0–50.0 GHz			+(1.75+10.0% of attenuation setting) / -1	dB
		50.0–55.0 GHz			+(1.80+12.5% of attenuation setting) / -1	dB
Attenuation error	**1 dB step**					
	0–31.0 dB	9.0 kHz–13.0 GHz			+(1.00+4.5% of attenuation setting) / -1	dB
		13.0–26.5 GHz			+(1.15+4.5% of attenuation setting) / -1	dB
		26.5–45.0 GHz			+(1.60+8.5% of attenuation setting) / -1	dB
		45.0–50.0 GHz			+(1.75+10.0% of attenuation setting) / -1	dB
		50.0–55.0 GHz			+(1.80+12.5% of attenuation setting) / -1	dB

Table 3 ▪ PE43508 Electrical Specifications (Cont.)

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Return loss	RF1, all states	9.0 kHz–13.0 GHz 13.0–26.5 GHz 26.5–45.0 GHz 45.0–50.0 GHz 50.0–55.0 GHz		13 16 14 13 13		dB dB dB dB dB
Return loss	RF2, all states	9.0 kHz–13.0 GHz 13.0–26.5 GHz 26.5–45.0 GHz 45.0–50.0 GHz 50.0–55.0 GHz		12 14 10 9 8		dB dB dB dB dB
Relative phase	All states	9.0 kHz–13.0 GHz 13.0–26.5 GHz 26.5–45.0 GHz 45.0–50.0 GHz 50.0–55.0 GHz		20 40 74 86 98		deg deg deg deg deg
Input 1 dB compression point[3]				Fig. 7		dBm
Input IP2	Two tones at +18 dBm, 1 MHz spacing, all states	2–16 GHz[4]		100		dBm
Input IP3	Two tones at +18 dBm, 1 MHz spacing, all states	2–16 GHz[4]		50		dBm
RF T_{rise}/T_{fall}	10%/90% RF			250		ns
Settling time	RF settled to within 0.05 dB of final value			500		ns
Switching time	50% CTRL to 90% or 10% RF			330	400	ns
Attenuation transient (envelope)				-7.5		dB

Notes:

1) Normal mode: Connect V_{SS_EXT} (pin 15) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: Use V_{SS_EXT} (pin 15) to bypass and disable internal negative voltage generator.
3) The input 1 dB compression point is a linearity figure of merit. Refer to Table 2 for the operating RF input power (50Ω).
4) Limited by the frequency range capabilities of the test systems.

Spur-free Performance

The PE43508 spur fundamental occurs around 4 MHz. Its typical spurious performance in normal mode is –168 dBm/Hz (pin 15 tied to ground), with 30 kHz bandwidth. If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 15).

Glitch-safe Attenuation State

The PE43508 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

Truth Tables

Table 4–Table 6 provide the truth tables for the PE43508.

Table 4 ▪ Parallel Truth Table

Parallel Control Setting						Attenuation Setting RF1–RF2
D6 (MSB)	D5	D4	D3	D2	D1 (LSB)	
L	L	L	L	L	L	Reference IL
L	L	L	L	L	H	0.5 dB
L	L	L	L	H	L	1 dB
L	L	L	H	L	L	2 dB
L	L	H	L	L	L	4 dB
L	H	L	L	L	L	8 dB
H	L	L	L	L	L	16 dB
H	H	H	H	H	H	31.5 dB

Table 5 ▪ Serial Address Word Truth Table

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	
L	L	L	L	L	L	L	L	000
L	L	L	L	L	L	L	H	001

Table 5 ▪ Serial Address Word Truth Table (Cont.)

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	
L	L	L	L	L	L	H	L	010
L	L	L	L	L	L	H	H	011
L	L	L	L	L	H	L	L	100
L	L	L	L	L	H	L	H	101
L	L	L	L	L	H	H	L	110
L	L	L	L	L	H	H	H	111

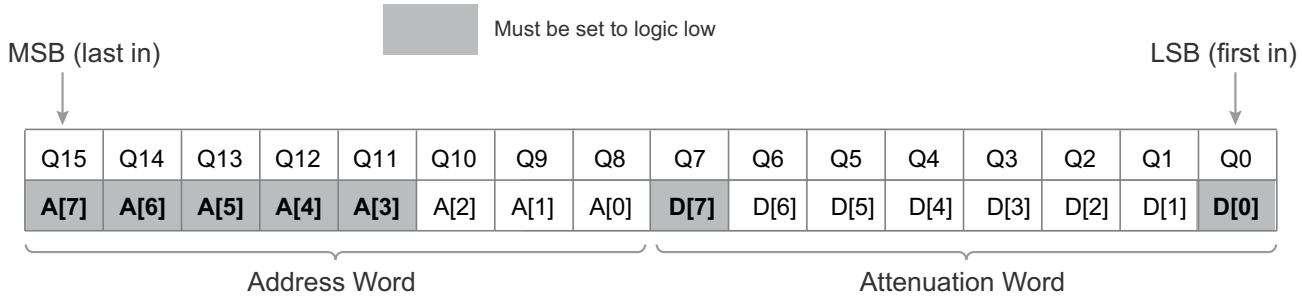
Table 6 ▪ Serial Attenuation Word Truth Table

Attenuation Word								Attenuation Setting RF1–RF2
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	L	31.5 dB

Serial Addressable Register Map

Figure 2 provides the serial addressable register map for the PE43508.

Figure 2 ▪ Serial Addressable Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 18.5 dB state at address 3:

$4 \times 18.5 = 74$
$74 \rightarrow 01001010$

Address Word: 00000011
Attenuation Word: **01001010**
Serial Input: 00000011**01001010**

Programming Options

Parallel/Serial Selection

Either a parallel or serial addressable interface can be used to control the PE43508. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the parallel interface and $\overline{P}$/S = HIGH selecting the serial interface. The $\overline{P}$/S pin has an internal tie HIGH (namely, the pin is internally tied to the 1.8V V_{DD}), so if this is left floating, the part defaults to serial mode. If there is a need to put this part in parallel mode, a LOW logic should be applied to this pin.

Parallel Mode Interface

The parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 4**.

The parallel interface timing requirements are defined by **Figure 4** (Latched-Parallel/Direct-Parallel Timing Diagram), **Table 10** (Parallel and Direct Interface AC Characteristics) and switching time (**Table 3**).

For latched parallel programming, the latch enable (LE) should be held LOW while changing attenuation state control values then pulse LE HIGH to LOW (per **Figure 4**) to latch new attenuation state into the device.

For direct parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values changes the device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial-Addressable Interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the attenuation word, which controls the state of the DSA. The second word is the address word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state remains unchanged. **Figure 3** illustrates an example timing diagram for programming a state.

The serial-addressable interface is controlled using three CMOS-compatible signals: SDI, CLK, and LE. The SDI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first. The serial interface data output, SDO, outputs serial input data delayed by 16 clock cycles to control the cascaded attenuator using a single serial peripheral interface (SPI) bus.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Address Word truth table is listed in **Table 5**. The address pins A0 (pin 12), A1 (pin 20), and A2 (pin 19) can either be grounded logic LOW or left floating (logic HIGH due to internal pull-up to 1.8V V_{DD}) depending upon what fixed address the user wants the DSA to be set at.The Attenuation Word truth table is listed in **Table 6**. A programming example of the serial register is illustrated in **Figure 2**. The serial timing diagram is illustrated in **Figure 3**.

Power-up Control Settings

The PE43508 always initializes to the maximum attenuation setting (31.5 dB) on power-up for both the serial addressable and latched parallel modes of operation (as long as the LE pin is logic LOW during start up) and it remains in this setting until the user latches in the next programming word.

In direct parallel mode ($\overline{P}$/S = LOW and logic HIGH present on the LE pin during the power-up), the DSA can be preset to any state within the 31.5 dB range by pre-setting the parallel control pins D[6:1] prior to power-up. In this mode, there is a 4 µs delay between the time the DSA is powered-up to the time the desired state is set. If the control pins are left floating in this mode during power-up, the device defaults to the 28dB attenuation setting.

In latched parallel mode ($\overline{P}$/S = LOW), if the LE pin is kept LOW during power-up, the part should default to maximum attenuation state (31.5dB). Logic LOW should be present on the LE pin during power-up and then logic HIGH should be written on the LE pin when the user wants to program the part. If the LE is kept floating during power-up, the part should default to maximum attenuation state (31.5dB).

In serial mode ($\overline{P}$/S = HIGH or left floating) logic HIGH on the LE pin during the power up: The part should default to minimum attenuation state

(reference state). But a logic LOW on the LE pin during the power up, the part should default to maximum attenuation state.

Dynamic operation between serial and parallel programming modes is not supported.

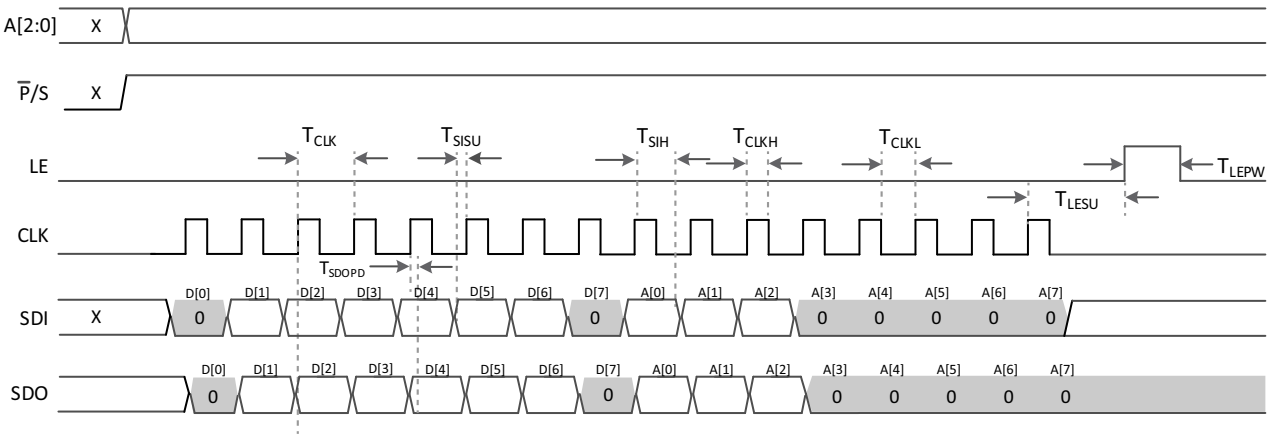
If the DSA powers up in serial mode ($\overline{P}$/S = HIGH), prior to toggling to parallel mode, the user must ensure that the pins LE, SDI/D1, CLK/D2, A0/D4, A1/D5, and A2/D6 are set to logic LOW.

If the DSA powers up in either latched or direct parallel mode, the pins LE, SDI/D1, CLK/D2, A0/D4, A1/D5, and A2/D6 must be set to logic LOW and the pin SDO/D3 set to high impedance prior to toggling to serial addressable mode ($\overline{P}$/S = HIGH).

Table 7 ▪ Summary of Power-up Functionality of the PE43508

Mode	$\overline{P}$/S	LE During Power-up	D[6:1] Pin Status	DSA State at Power-up
Serial mode	1	0		Maximum attenuation
	1	1		Reference state
	1	Floating		Maximum attenuation
Latch parallel mode	0	0	Don't care	Maximum attenuation
	0	Floating	Don't care	Maximum attenuation
Direct parallel mode	0	1	Data present on the D[6:1] lines	Attenuation state depends upon the logic present on the pins D[6:1]
			D[6:1] lines floating	28 dB attenuation state

Figure 3 ▪ Serial Addressable Timing Diagram



Notes:
1. SPI mode 0:
   - SDI data is captured on the CLK's rising edge
   - SDO data is valid on CLK falling edge
2. CLK shared pin with 1 dB parallel control bit D2
3. SDI shared pin with 0.5 dB parallel control bit D1
4. SDO shared pin with 2 dB parallel control bit D3
5. A0 shared pin with 4 dB parallel control bit D4
6. A1 shared pin with 8 dB parallel control bit D5
7. A2 shared pin with 16 dB parallel control bit D6
8. Serial data bits D[7], D[0], and A[7:3] must be set to logic low
9. X = Undefined

Table 8 ▪ Serial Interface AC Characteristics[1]

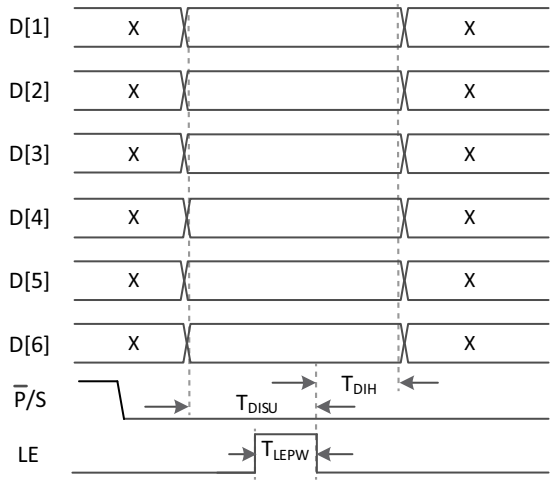
Parameter/Condition	Min	Max	Unit
Serial clock frequency, F_{CLK}		10	MHz
Serial clock time period, T_{CLK}	100		ns
Serial clock HIGH time, T_{CLKH}	30		ns
Serial clock LOW time, T_{CLKL}	30		ns
Last serial clock rising edge setup time to latch enable rising edge, T_{LESU}	10		ns
Latch enable minimum pulse width, T_{LEPW}	30		ns
Serial data setup time, T_{SISU}	10		ns
Serial data hold time, T_{SIH}	10		ns
Serial interface data output (SDO) propagation delay, T_{SDOPD}		30[2]	ns

1) V_{DD} = 3.3V or 5.5V, –40 °C, < T_A < +105 °C, unless otherwise specified.
2) Measured with 10 pF SDO load capacitance.

Table 9 ▪ Latch and Clock Specifications

Latch Enable (LE)	Clock (CLK)	Function
0	↑	Shift register clocked
↑ (rising edge)	X	Contents of shift register transferred to attenuator core

Figure 4 ▪ Latched-Parallel/Direct-Parallel Timing Diagram



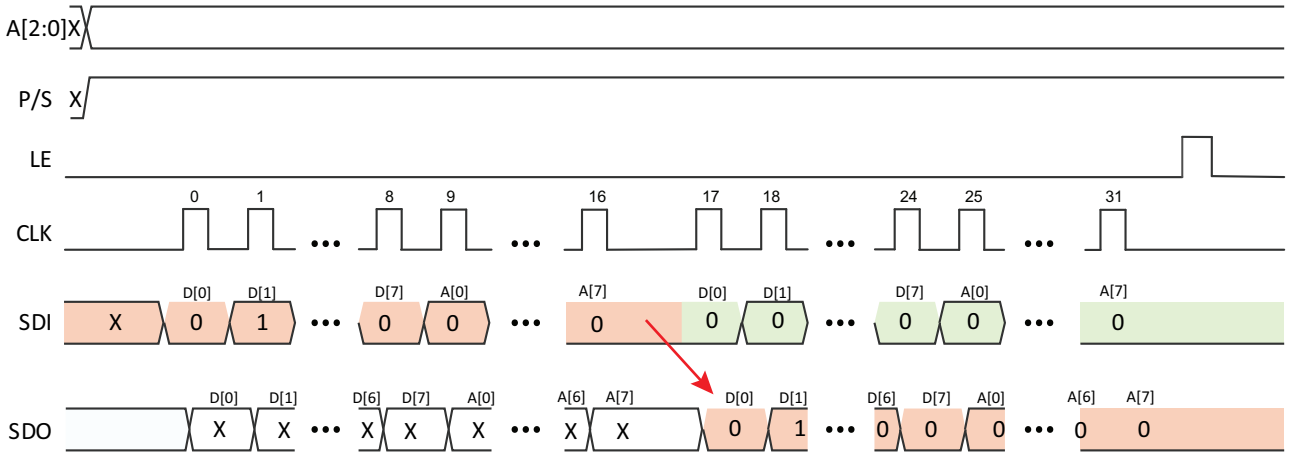
Notes:
1. D1 is shared with serial interface data input SDI
2. D2 is shared with serial interface clock input CLK
3. D3 is shared with serial interface data output SDO
4. D4 is shared with serial address bit A0
5. D5 is shared with serial address bit A1
6. D6 is shared with serial address bit A2
7. X = Undefined

Table 10 ▪ Parallel and Direct Interface AC Characteristics(*)

Parameter/Condition	Min	Max	Unit
Latch enable minimum pulse width, T_{LEPW}	30		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Note: * V_{DD} = 3.3V or 5.5V, –40 °C < T_A < +105 °C, unless otherwise specified.			

The following example shows a scenario where two DSAs are connected in series.

Figure 5 ▪ Serial Addressable Cascaded Devices Example



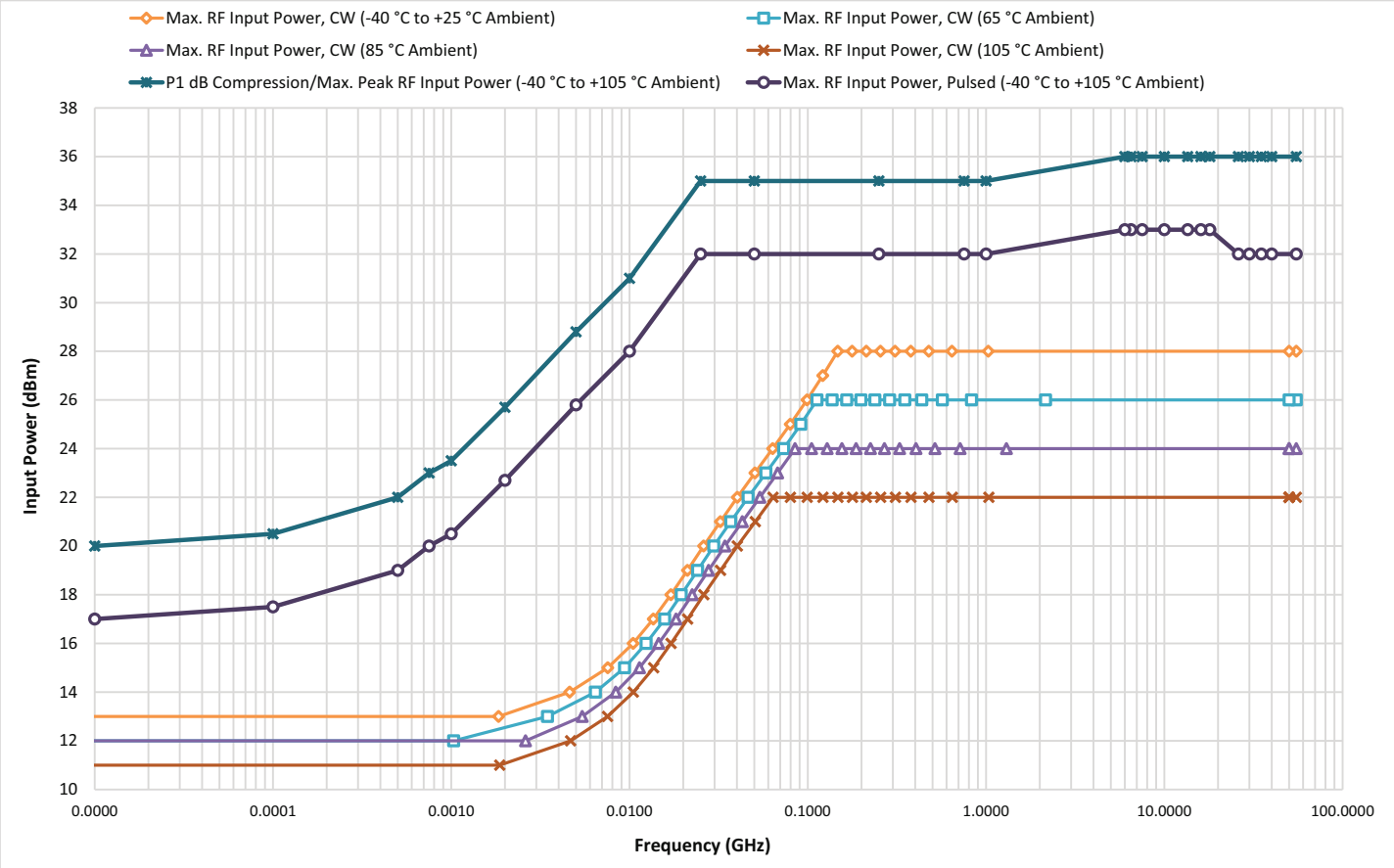
Example Scenario: 2 DSAs connected in series (SDO to SDI).
First write after power up
Signals from first DSA in chain
X = Undefined

The following table provides the complete SDI and SDO content for the example shown in **Figure 5**.

Figure 6 ▪ Serial Addressable Cascaded Devices Table

	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]
CLK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
SDI	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SDO	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 7 ▪ Power De-rating Curve, 9 kHz–55GHz, 50 Ω



Typical Performance Data

Figure 8–Figure 36 show the typical performance data at 25 °C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Figure 8 ▪ Insertion Loss vs. Temperature

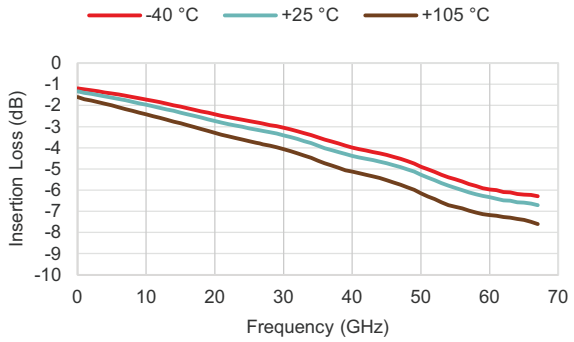


Figure 9 ▪ RF1 Return Loss (Major Attenuation States) vs. Attenuation Setting

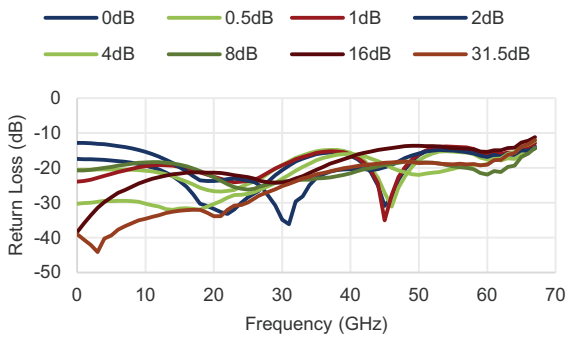


Figure 10 ▪ RF1 Return Loss (All Attenuation States) vs. Attenuation Setting

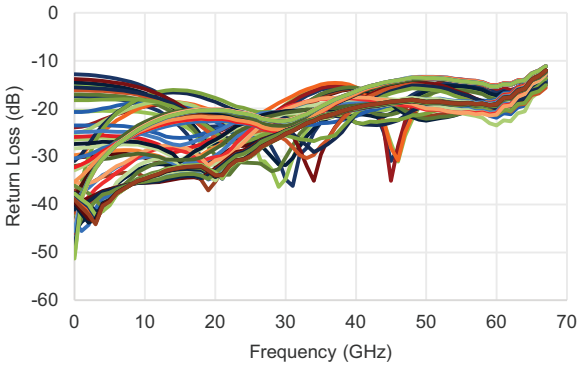


Figure 11 ▪ RF2 Return Loss (Major Attenuation States) vs. Attenuation Setting

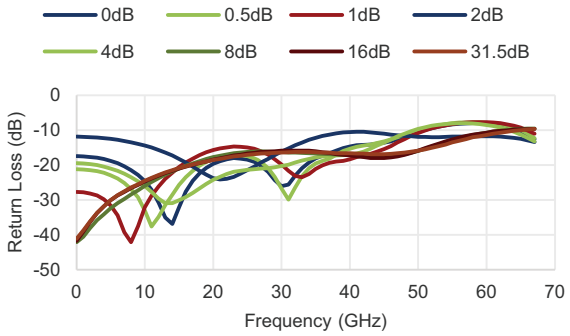


Figure 12 ▪ RF2 Return Loss (All Attenuation States) vs. Attenuation Setting

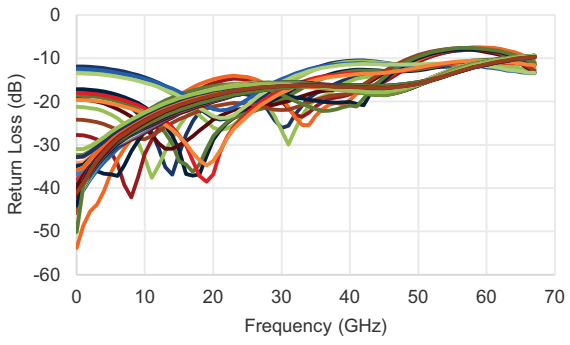


Figure 13 ▪ RF1 Return Loss for Reference State vs. Temperature

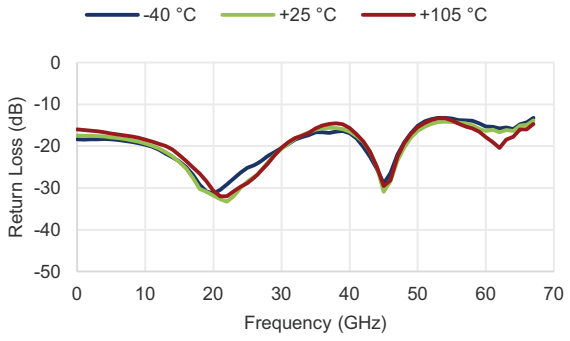


Figure 14 ▪ RF1 Return Loss for 31.5 dB Attenuation Setting vs. Temperature

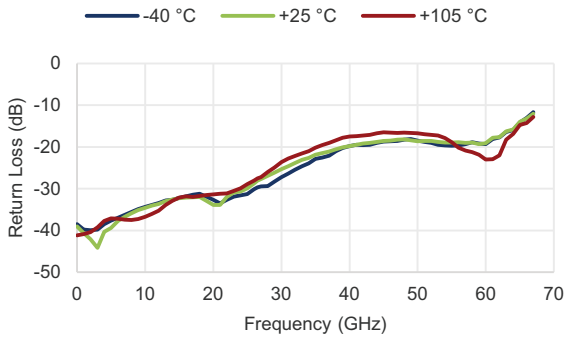


Figure 15 ▪ RF2 Return Loss for Reference State vs. Temperature

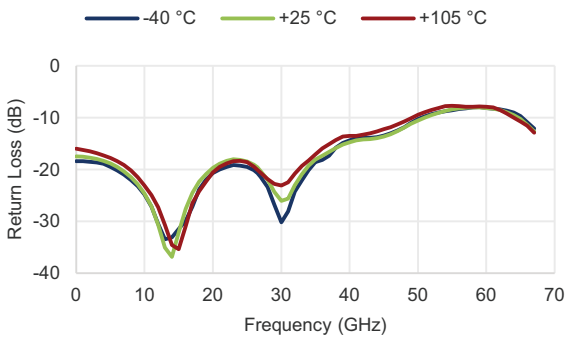


Figure 16 ▪ RF2 Return Loss for 31.5 dB Attenuation Setting vs. Temperature

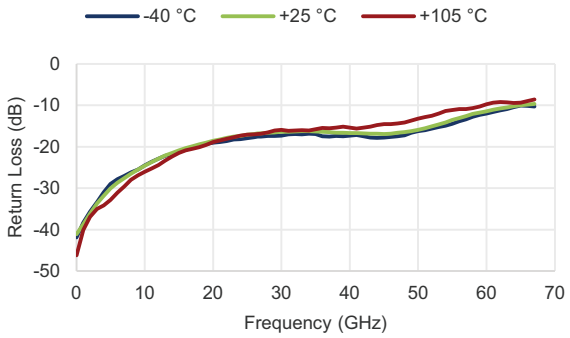


Figure 17 ▪ Relative Phase Error vs. Attenuation Setting

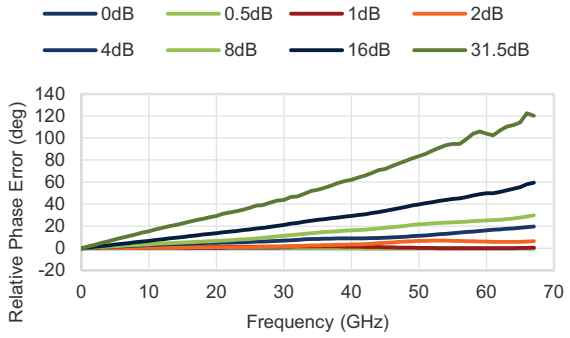


Figure 18 ▪ Relative Phase Error for 31.5 dB Attenuation Setting vs. Frequency

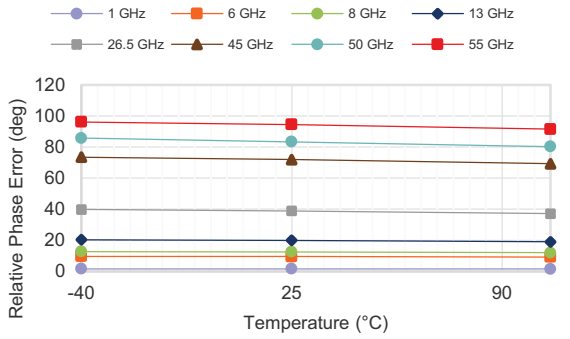


Figure 19 ▪ Attenuation Error @ 6 GHz vs. Temperature

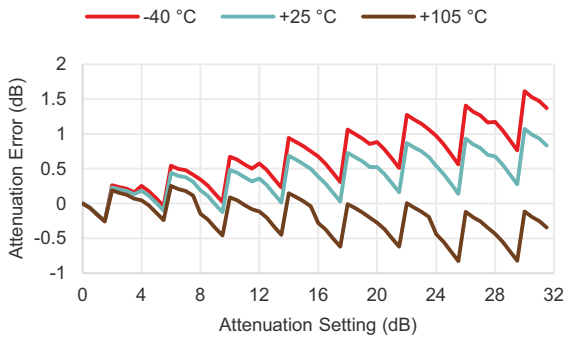


Figure 20 ▪ Attenuation Error @ 8 GHz vs. Temperature

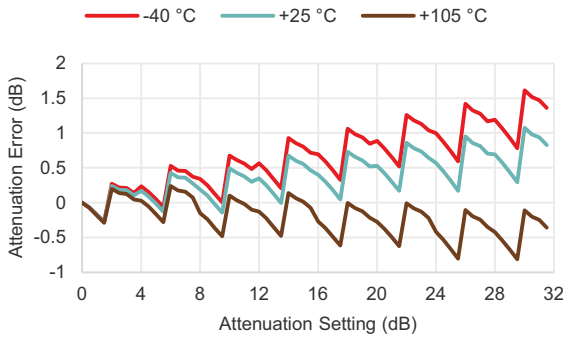


Figure 21 ▪ Attenuation Error @ 13 GHz vs. Temperature

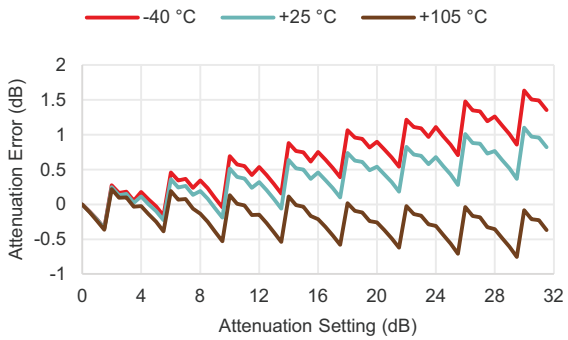


Figure 22 ▪ Attenuation Error @ 26.5 GHz vs. Temperature

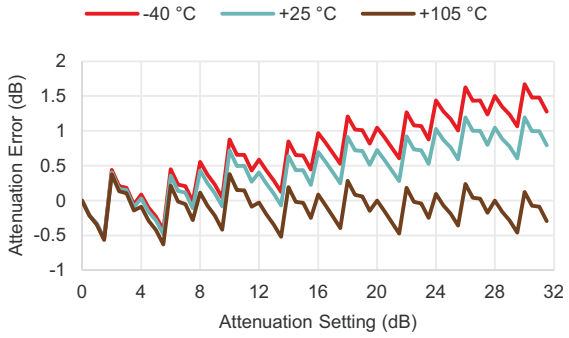


Figure 23 ▪ Attenuation Error @ 45 GHz vs. Temperature

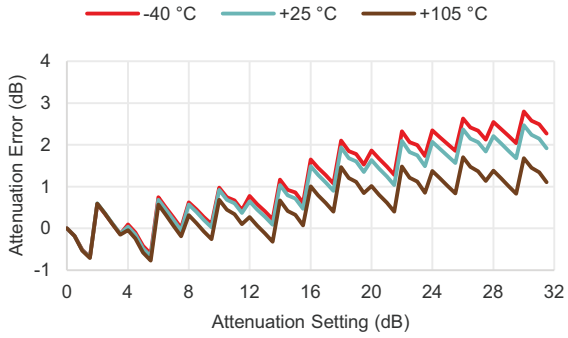


Figure 24 ▪ Attenuation Error @ 50 GHz vs. Temperature

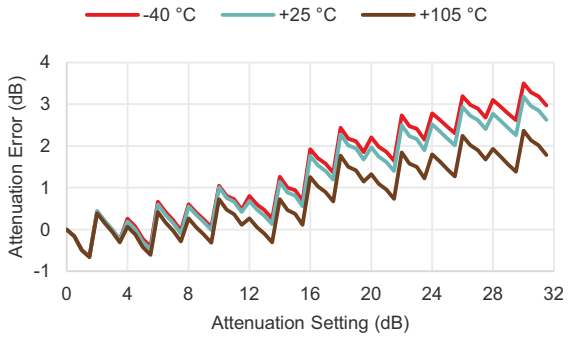


Figure 25 ▪ Attenuation Error @ 55 GHz vs. Temperature

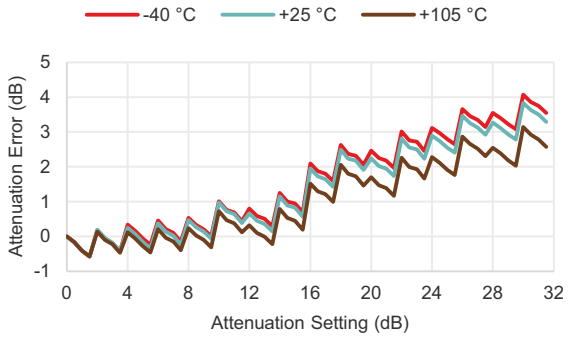


Figure 26 ▪ 0.5 dB Step Attenuation vs. Frequency[1]

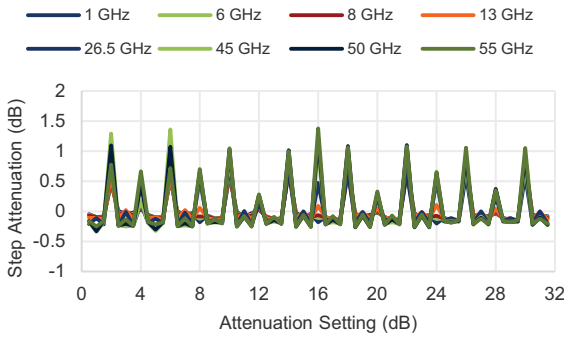


Figure 27 ▪ 1 dB Step Attenuation vs. Frequency[2]

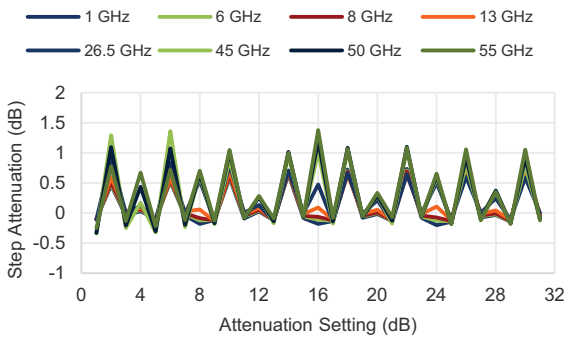


Figure 28 ▪ 0.5 dB Step, Actual vs. Frequency

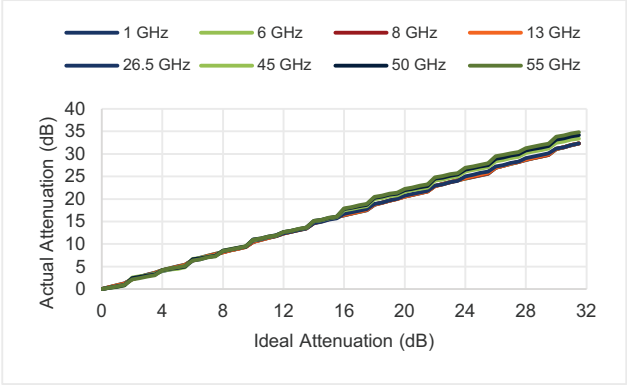


Figure 29 ▪ 1 dB Step, Actual vs. Frequency

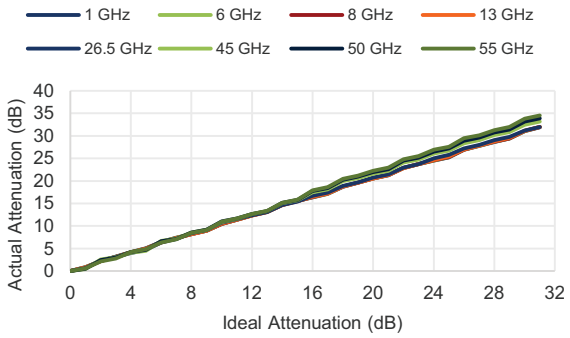


Figure 30 ▪ Major State Bit Error vs. Attenuation Setting

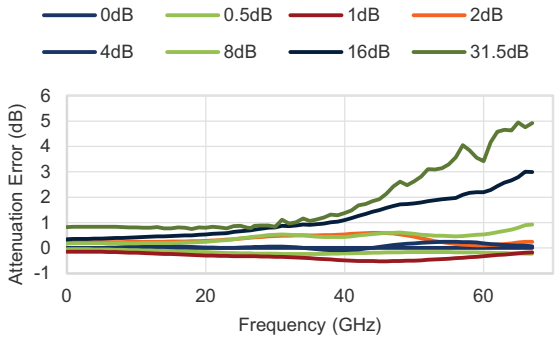
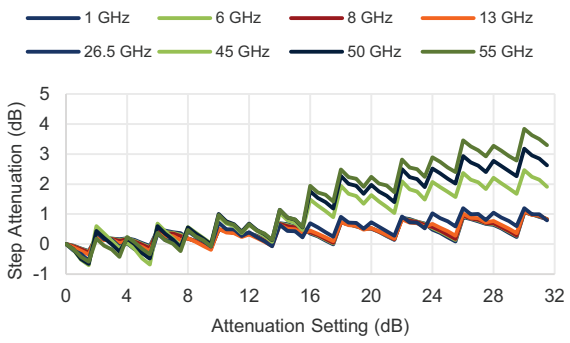


Figure 31 ▪ 0.5 dB Attenuation Error vs. Frequency



1) Monotonicity is held so long as step attenuation does not cross below -0.5 dB.
2) Monotonicity is held so long as step attenuation does not cross below -1.0 dB.

Figure 32 ▪ 1 dB Attenuation Error vs. Frequency

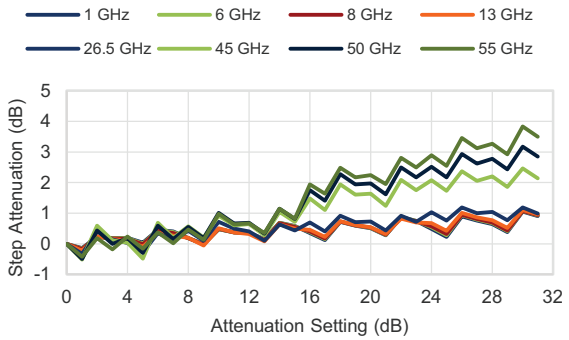


Figure 33 ▪ IIP2 vs. Attenuation Setting

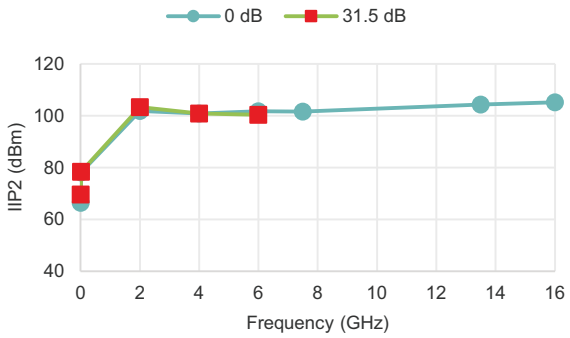


Figure 34 ▪ IIP3 vs. Attenuation Setting

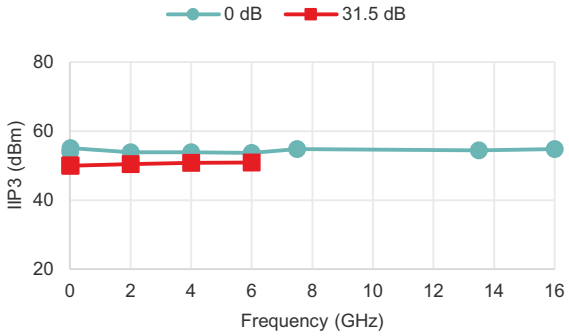


Figure 35 ▪ Attenuation Transient (23.5-24 dB)

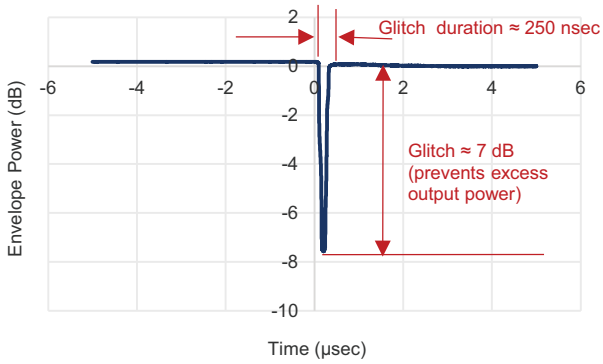
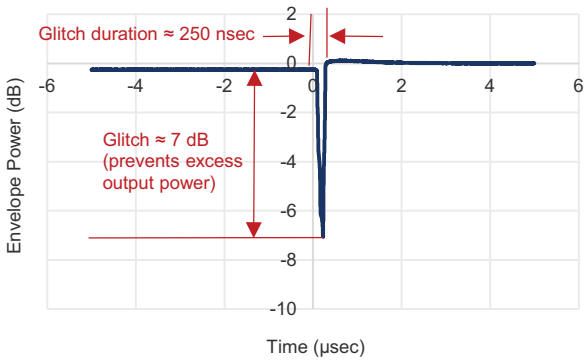


Figure 36 ▪ Attenuation Transient (24-23.5 dB)

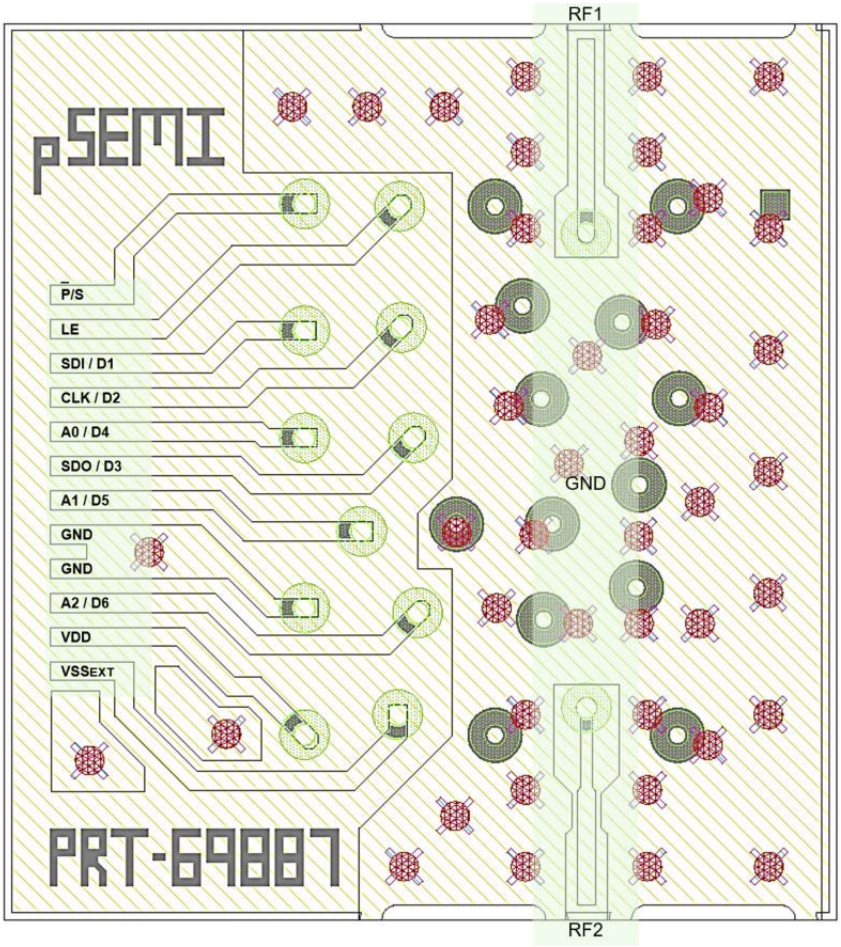


Evaluation Setup

The PE43508 s-parameter data up to 67 GHz (**Table 3** and **Figure 8–Figure 32**) were taken using either co-planar waveguide with ground (CPWG) or grounded co-planar waveguide (GCPW) on an alumina substrate (**Figure 37**) and RF probes.

The PE43508 input 1dB compression point below 40 GHz, input IP2 and IP3 measurements up to 16 GHz, settling time and switching time (**Table 3**) were taken on a mmWave PCB using 2.92 mm connectors.

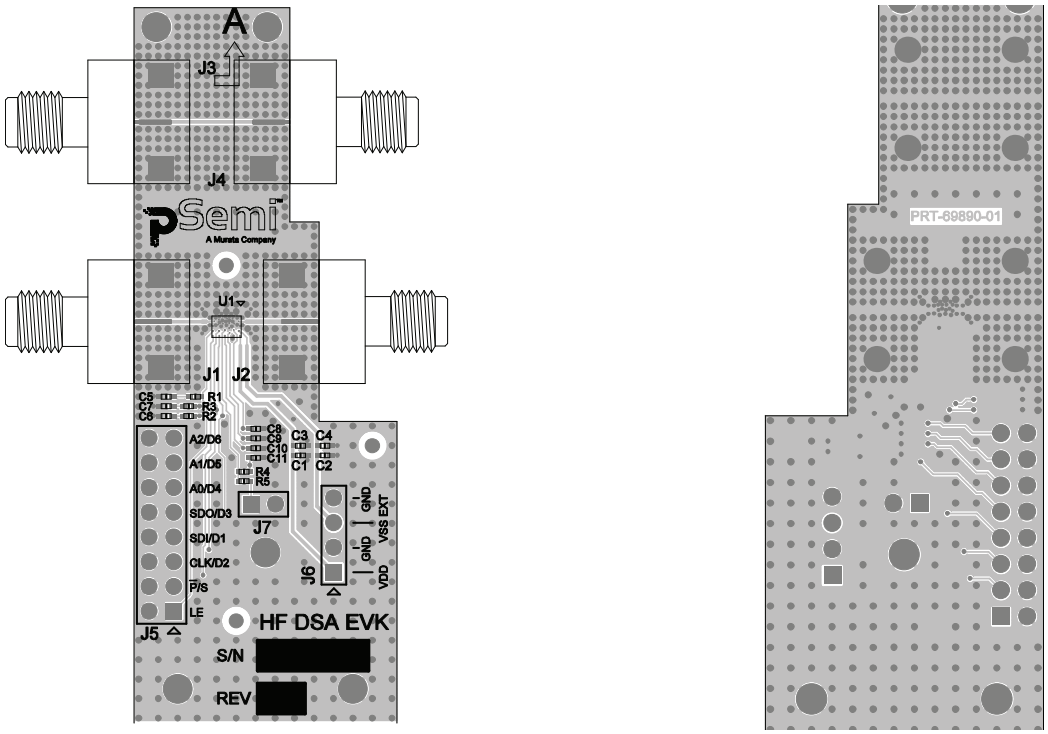
Figure 37 ▪ Alumina Substrate Board Used in the PE43508 Evaluation



Evaluation Kit

There are two types of evaluation kits, CPWG or GCPW on an alumina substrate (**Figure 37**) and a mmWave PCB using 2.92 mm connectors (**Figure 38**), designed to ease customer evaluation of the PE43508 digital step attenuator. For more information on the mmWave PCB evaluation kit, see the *PE43508 Evaluation Kit (EVK) User's Manual*. For more information on the alumina substrate evaluation kit, see Application Note 78, *PE43508 55 GHz DSA Substrate Carrier Assembly Guide*.

Figure 38 ▪ mmWave PCB Evaluation Kit Layout for the PE43508



Pin Configuration

This section provides pin information for the PE43508. **Figure 39** shows the pin configuration of this device. **Table 11** provides a description for each pin.

Figure 39 ▪ Pin Configuration (Bumps Up) for the PE43508

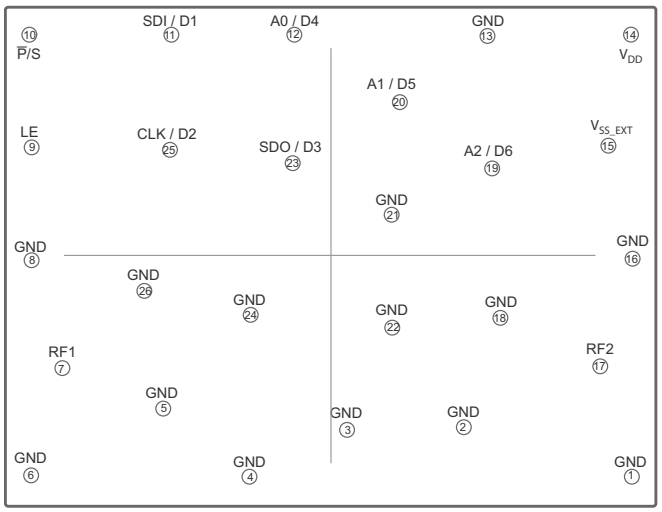


Table 11 ▪ Pin Descriptions for the PE43508

Pin No.	Pin Name	Description
1–6, 8, 13, 16, 18, 21, 22, 24, 26	GND	Ground
7	RF1(1)	RF1 port
9	LE	Serial/parallel interface latch enable input
10	$\overline{P}$/S(2)	Serial/parallel mode select
11	SDI/D1	Serial interface data input/parallel control bit, 0.5 dB
12	A0/D4(2)	Address bit A0 connection/parallel control bit, 4 dB
14	V_{DD}	Supply voltage
15	V_{SS_EXT}(3)	External V_{SS} negative voltage control
17	RF2(1)	RF2 port
19	A2/D6(2)	Address bit A2 connection/parallel control bit, 16 dB
20	A1/D5(2)	Address bit A1 connection/parallel control bit, 8 dB
23	SDO/D3	Serial interface data output/parallel control bit, 2 dB
25	CLK/D2	Serial interface clock input/parallel control bit, 1 dB

Notes:

1) RF pins 7 and 17 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) $\overline{P}$/S (pin 10), A0/D4 (pin 12), A2/D6 (pin 19) and A1/D5 (pin 20) have internal 1.5 MΩ pull-up resistor to internal 1.8V V_{DD}. These pins will have an internal logic HIGH on them if they are left floating by the user. In serial mode, the user can leave the $\overline{P}$/S pin floating and the part will default to serial mode.
3) Use V_{SS_EXT} (pin 15) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 15) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE43508.

Table 12 ▪ Mechanical Specifications forthe PE43508

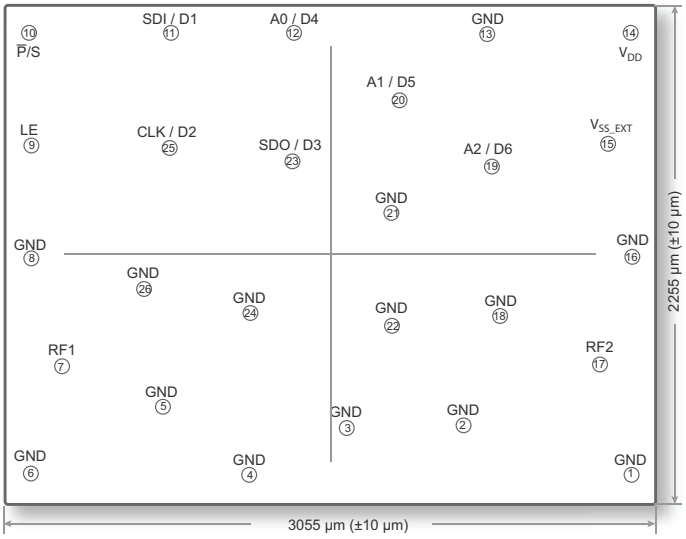
Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x, y)	3045 x 2245	3055 x 2255	3065 x 2265	µm	Including excess silicon, max. tolerance = ±10 µm
Wafer thickness	180	200	220	µm	
Bump pitch	500			µm	
Bump height	59.5	70	80.5	µm	
Bump diameter		91		µm	
UBM diameter	71	75	79	µm	

Table 13 ▪ Pin Coordinates for the PE43508

Pin No.	Pin Name	Pin Center (µm)	
		X	Y
1	GND	1397.760	–985.005
2	GND	621.680	–767.980
3	GND	80.290	–782.555
4	GND	–375.400	–994.535
5	GND	–776.255	–693.460
6	GND	–1386.755	–985.005
7	RF1	–1239.910	–504.810
8	GND	–1386.755	–24.480
9	LE	–1386.985	476.250
10	$\overline{P}$/S	–1399.635	977.150
11	SD1/D1	–732.120	977.150
12	A0/D4	–167.870	977.150
13	GND	727.870	977.150
14	VDD	1395.190	977.150
15	V_{SS_EXT}	1288.820	487.020
16	GND	1397.760	–24.480
17	RF2	1252.620	–505.905
18	GND	788.690	–280.620
19	A2/D6	753.100	383.070
20	A1/D5	323.530	677.170
21	GND	287.050	178.310
22	GND	285.870	–326.035
23	SDO/D3	–168.360	404.800
24	GND	–372.300	–267.810
25	CLK/D2	–749.140	468.770
26	GND	–862.865	–169.675

Note: * All pin locations originate from the die center and refer to the center of the pin.

Figure 40 ▪ Pin Layout for the PE43508[1][2]



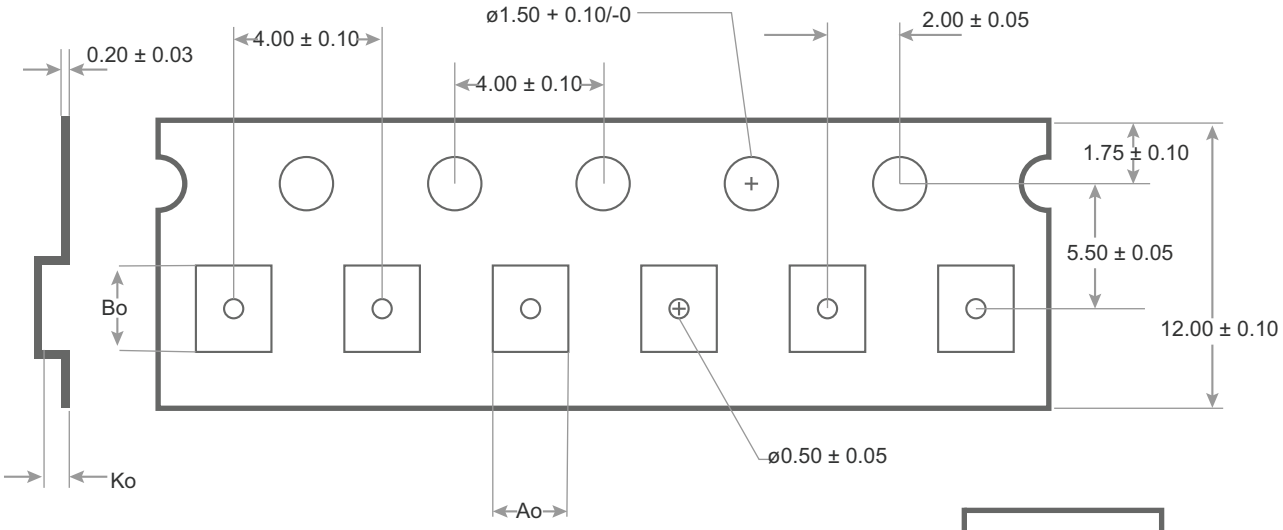
Notes:

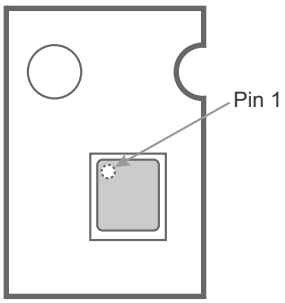
1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.

Tape and Reel Specification

This section provides the tape and reel specification for the PE43508.

Figure 41 ▪ Tape and Reel Specifications for the PE43508





Device Orientation in Tape

Pocket	Nominal	Tolerance
Ao	2.50	± 0.05
Bo	3.29	± 0.05
Ko	0.38	± 0.05

Notes:

Not Drawn to Scale
Dimensions are in millimeters
Maximum cavity angle 5 degrees
Bumped die are oriented active side down

Storage Recommendation

As a best practice, devices that will be stored for a long period of time (> 1 week) should be kept in a dry nitrogen environment.

Ordering Information

Table 14 lists the available ordering code for the PE43508 as well as the available shipping method.

Table 14 ▪ Order Code for the PE43508

Order Codes	Description	Packaging	Shipping Method
PE43508A–V	PE43508 Digital step attenuator	Die on tape and reel	250 die/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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