

Using a 50Ω Switch Within a 75Ω System



Application Note 48

Summary

Question: Can I use a switch defined for use in a 50Ω system within a 75Ω system?

Answer: Yes, provided you are prepared to accept some changes in the device performance. This may not always be degradation in performance.

Introduction

Switches are rarely designed to operate exclusively within a 50Ω defined characteristic impedance (Z_0) system. They are more commonly designed to perform optimally within a 50Ω system, but this does not exclude their use within a system of different characteristic impedance, such as 75Ω.

Generally switches are designed to meet the requirements of low loss, high isolation and good system impedance matching.

Designing for low loss means designing for the lowest series, through-path, resistance and lowest shunt capacitance. This means the through-path design is independent of characteristic impedance Z_0 .

Similarly in a short-terminated, reflective switch, the terminated unused port is designed to have the lowest impedance to ground. This is also independent of characteristic impedance Z_0 .

For a reflective switch, it is only the characterization of the device performance that is dependent on the system impedance. The results of this characterization can easily be used to estimate the performance of the device within a system of different characteristic impedance. This application note shows the performance within a 75Ω system of a reflective switch characterized within a 50Ω system.

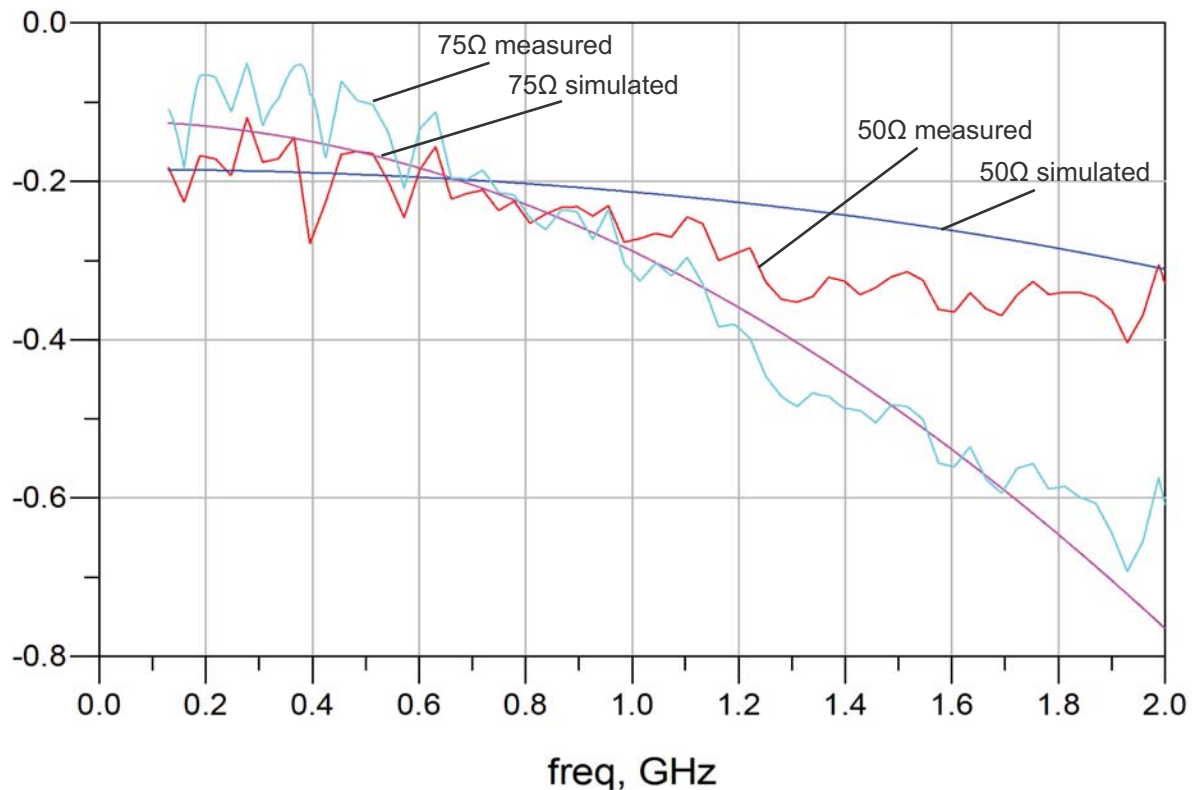
Absorptive switches are designed for an unused port termination of 50Ω. This is the only parameter that is designed for specific system impedance. This application note also shows how the 50Ω terminated port performs within a 75Ω system and the tradeoff required.

Analysis

50Ω Short Reflective Switch

Figure 1 shows the measured performance of a 50Ω characterized closed reflective switch within a 50Ω and 75Ω system. It also shows the same performance using a simplified device model. The purpose of this model is to validate the use of measured 50Ω S-parameters within the 75Ω analysis.

Figure 1 • Through Path Insertion Loss



As expected, the low frequency and DC insertion loss in a 75Ω system is slightly lower than in a 50Ω system. This is simply explained by viewing the switch conductive path resistance as a potential divider with the system load.

Similarly, as the frequency increases the switch shunt capacitive element impedance drops, and this has a greater effect on the system with the higher characterization impedance Z_0 (75Ω) over the lower Z_0 (50Ω). In this switch example, this results in crossover in the insertion loss curves at ~700 MHz.

Reduced insertion loss at lower frequency within the 75Ω system does not mean the power handling of the device has increased. In fact, the opposite is correct. Many product limitations such as max power handling, input IP3 (IIP3) and input 1dB compression point (P1dB) are dependent on the signal voltages within the device rather than the incident power.

In the 75Ω case, for a fixed incident power, the voltage present is $\sqrt{(75/50)} = 1.22x$ higher than the 50Ω case. In general, within a 75Ω system, the incident power needs to be reduced by 1.7 dB to maintain the same internal voltage. This means the max allowed power in a 75Ω system should be reduced by 1.7 dB compared to the 50Ω specification. Therefore the 75Ω IP3 figure will reduce by $3/2 \times 1.7 = 2.55$ dB when compared to the 50Ω specification.

The match of the device is also not heavily dependent on the system impedance. **Figure 2** to **Figure 5** show switch performance when terminated by the system characteristic impedance of either 50Ω or 75Ω.

Figure 2 • S11 Thru Port

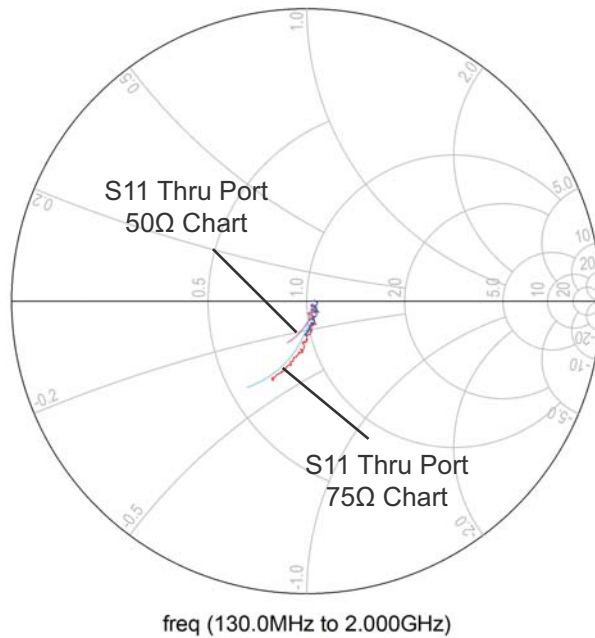


Figure 3 • S11 Thru Port dB Return Loss

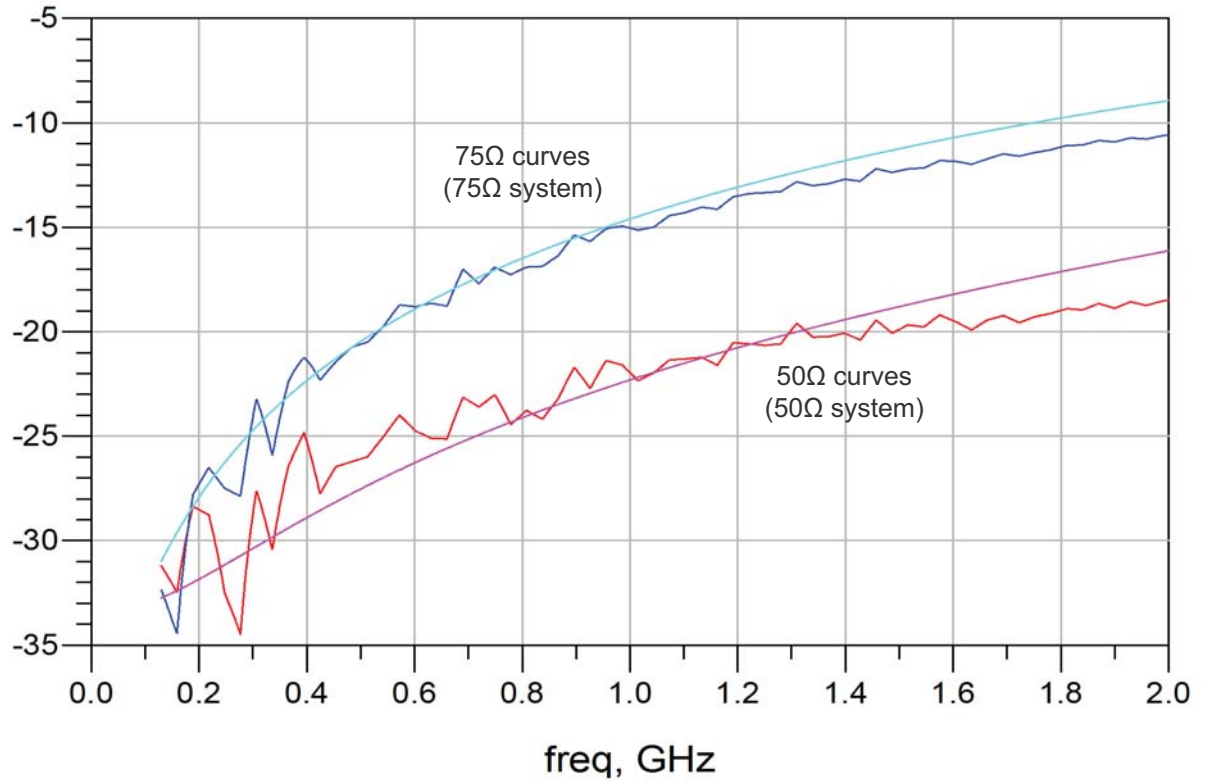


Figure 4 • Unused Port Shunt Termination

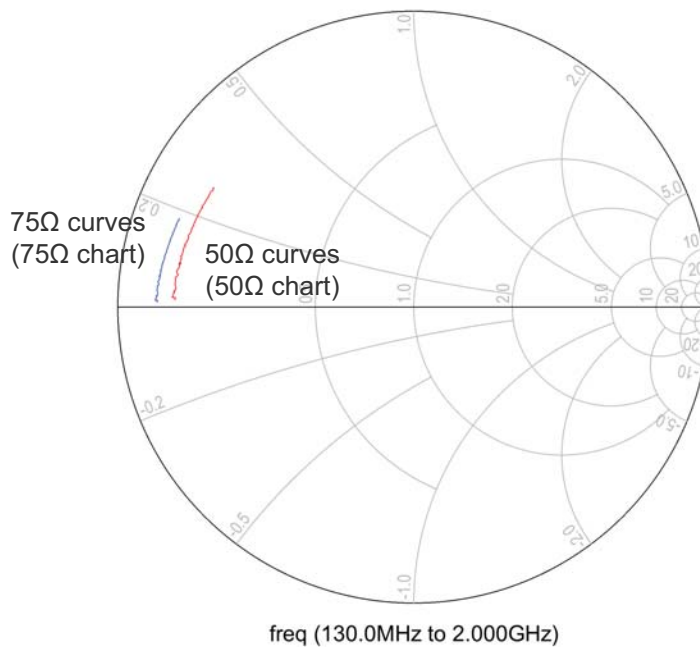
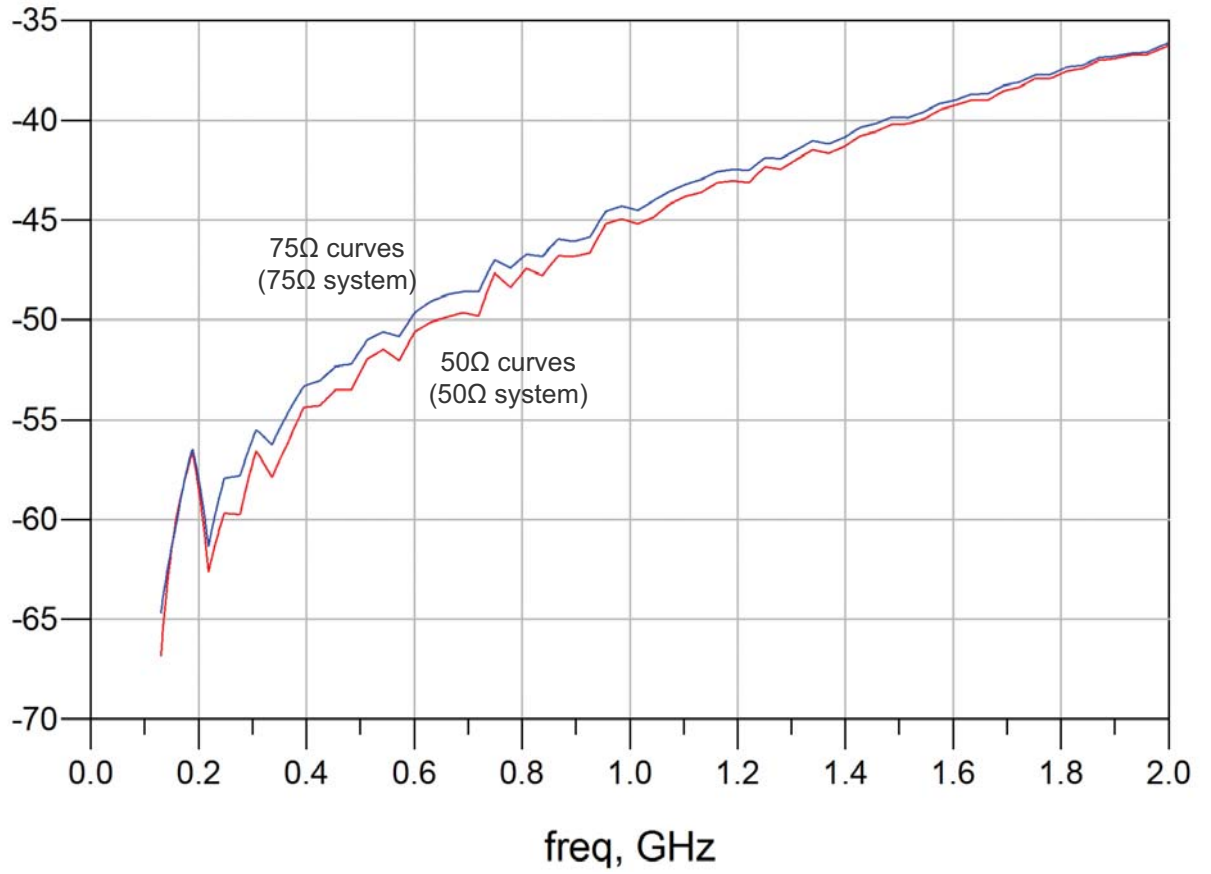


Figure 5 • Isolation (Short Reflective Switch)



50Ω Terminated Absorptive Switch

For a 50Ω absorptive switch the through path insertion loss and isolation have a similar performance as the reflective switch (see **Figure 6** and **Figure 7**).

Figure 6 • Through Path Insertion Loss

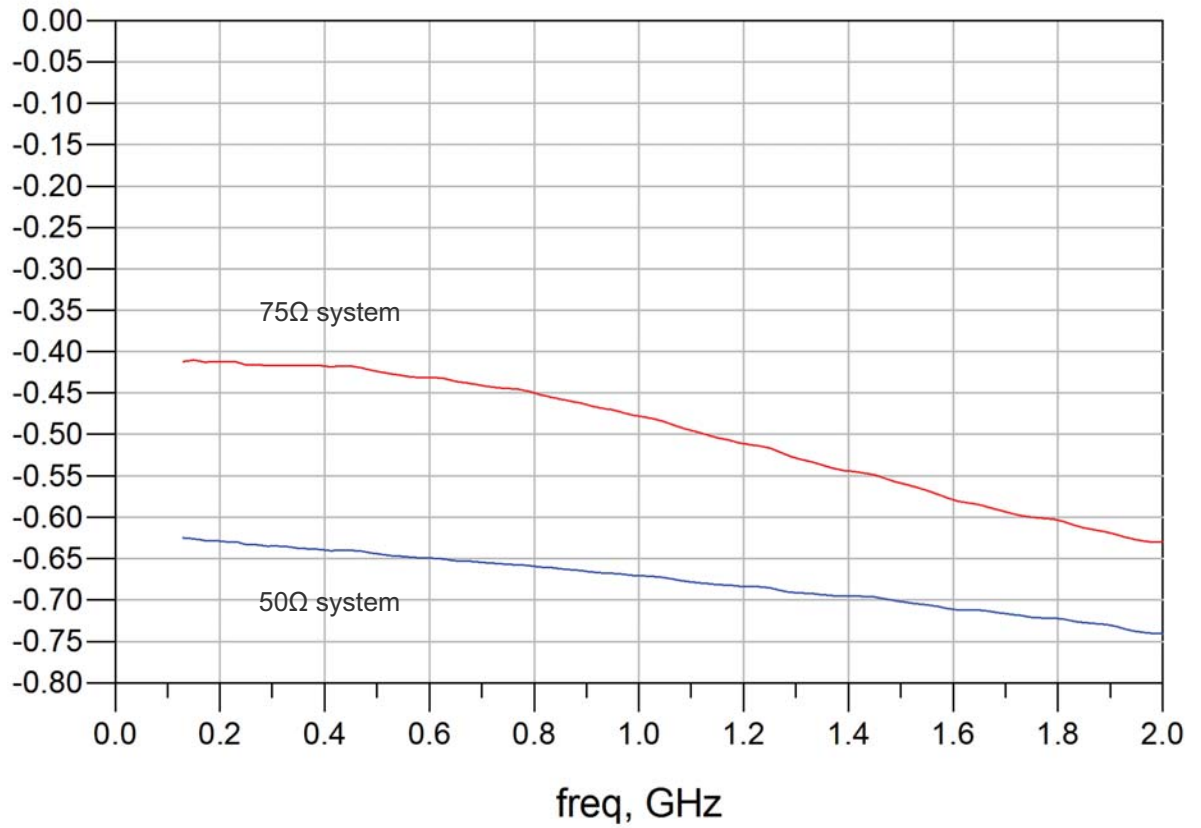
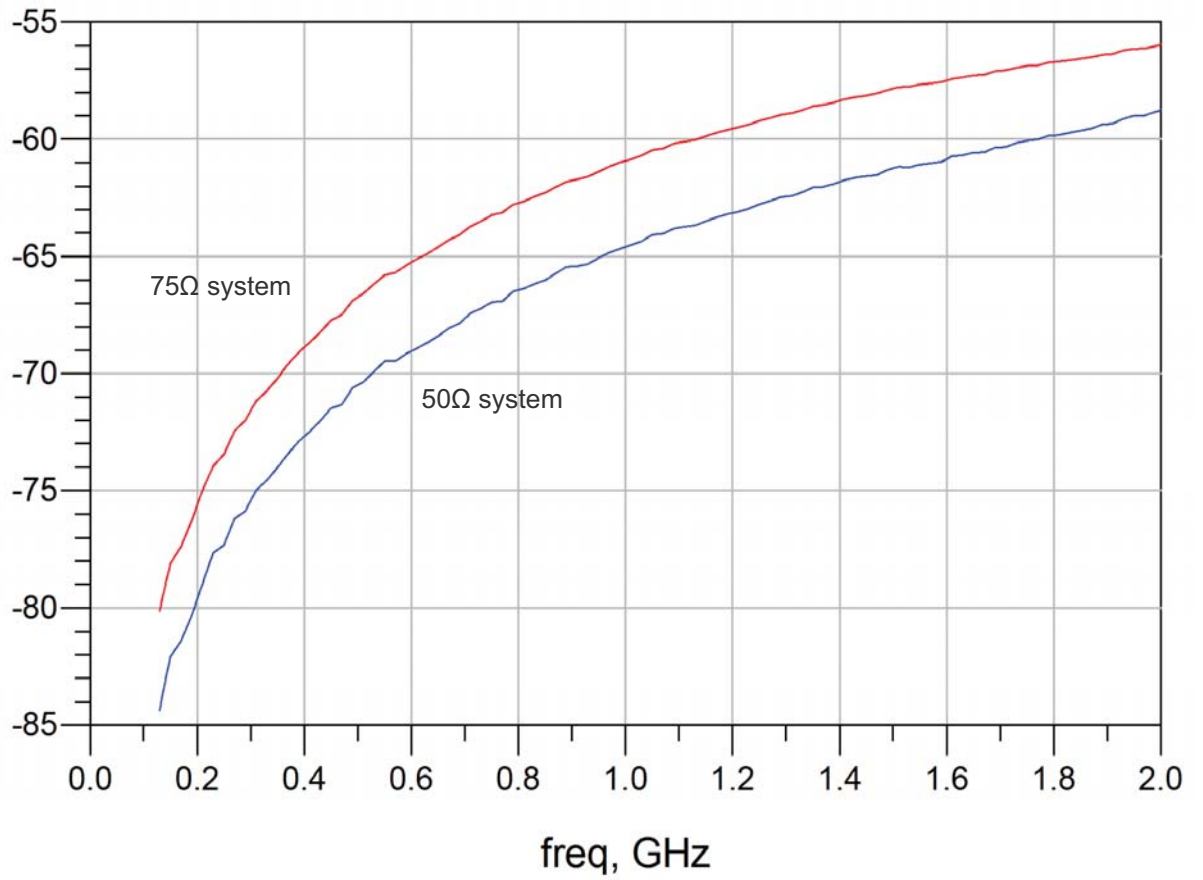


Figure 7 • Isolation



For a 50Ω absorptive switch, the fixed termination value of the unused port will result in an approximate 14 dB return loss due to the mismatch between the 50Ω termination and the 75Ω characteristic impedance (see **Figure 8** and **Figure 9**).

Figure 8 • 50Ω Absorptive Switch Port Match (75Ω System and Chart)

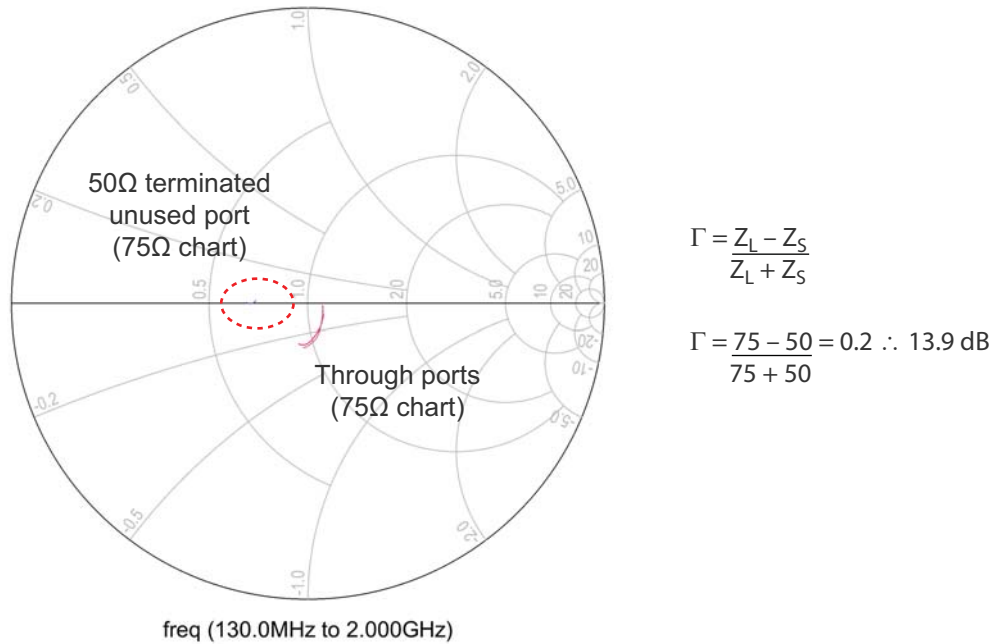
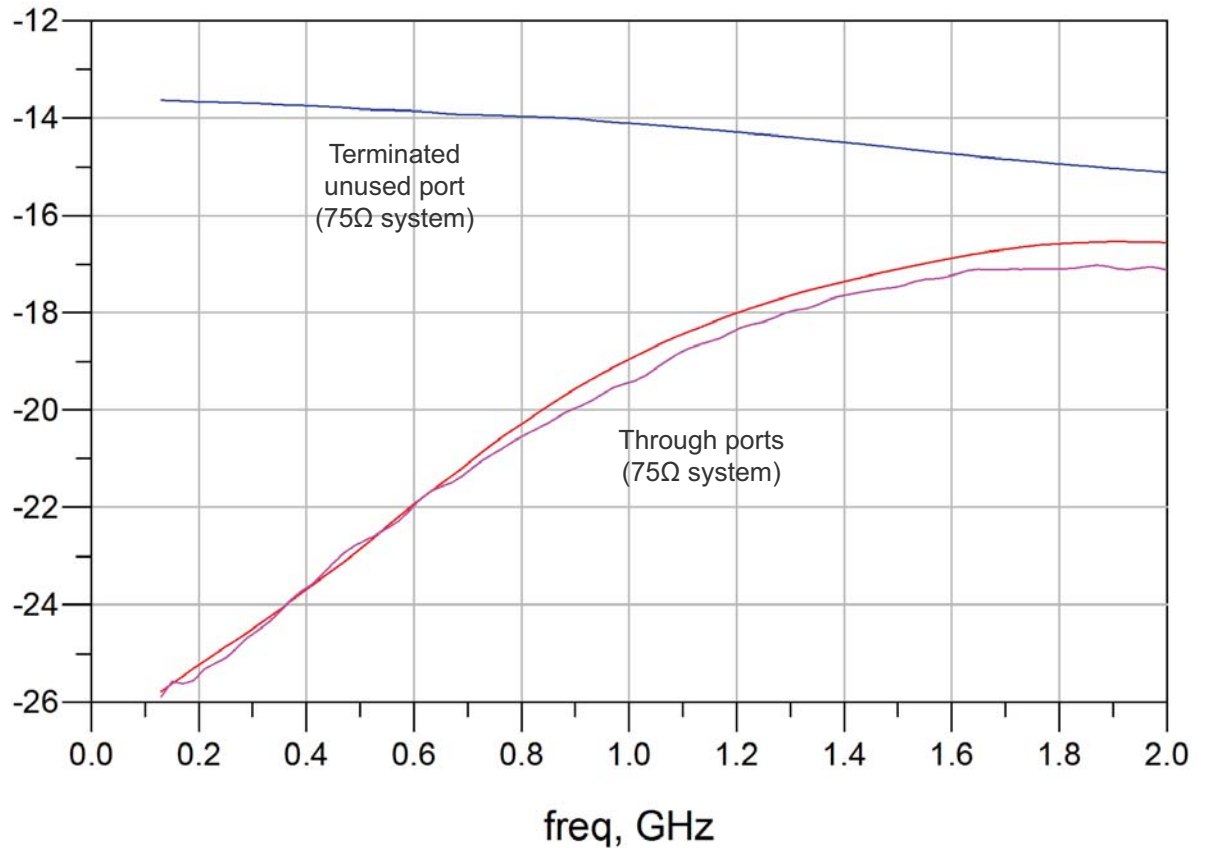


Figure 9 • 50Ω Absorptive Switch Port Return Loss (75Ω System)



Conclusion

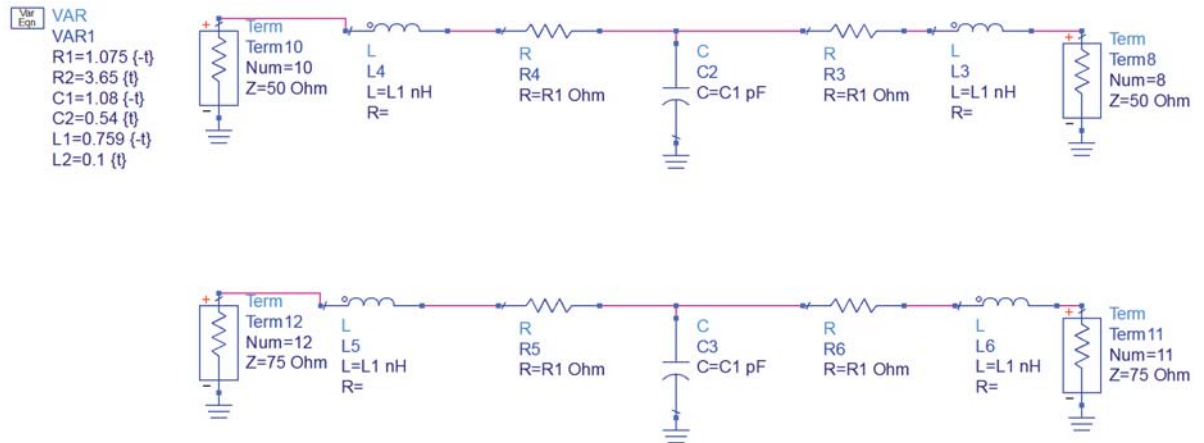
When considering a 50Ω switch for use in a 75Ω system the following points should be considered:

- In general the insertion loss of the switch will drop, especially at lower frequencies.
- The IIP3 will drop by ~2–2.5 dBm.
- The P1dB will drop by ~1.7 dB.
- The match will be very similar to 50Ω for the through path. It is more dependent on the external load rather than the switch.
- A short reflective port will have a very similar performance in both 50Ω and 75Ω.
- A 50Ω absorptive port will have a 12–14 dB return loss.
- A 50Ω absorptive switch isolation may drop by ~5 dB.

Appendix

Figure 10 is a simplified switch thru path model used to validate the analysis of the S-parameters. The component values are the same for each model.

Figure 10 • Switch Thru Path Simplified Model



Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark

©2015, Peregrine Semiconductor Corporation. All rights reserved. The Peregrine name, logo, UTSi and UltraCMOS are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.