PE43610

Document Category: Product Specification

UltraCMOS® RF Digital Step Attenuator, 9 kHz–13 GHz

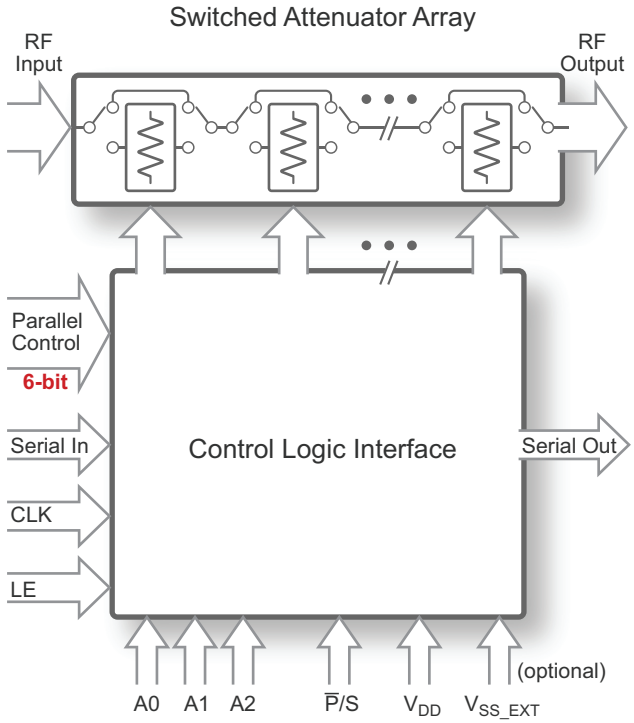
Features

- Wideband support from 9 kHz to 13 GHz
- Glitch-safe attenuation state transitions
- Flexible attenuation steps of 0.5 dB and 1 dB up to 31.5 dB
- +105 °C operating temperature
- Parallel and serial programming interfaces with serial addressability
- High HBM ESD of 1 kV
- Packaging – 24-lead 4 x 4 mm LGA

Applications

- Test and measurement (T&M)
- Point-to-point communication systems
- Very small aperture terminals (VSAT)

Figure 1 ▪ PE43610 Functional Diagram



Product Description

The PE43610 is a 50Ω, HaRP™ technology-enhanced, 6-bit RF digital step attenuator (DSA) that supports a wide frequency range from 9 kHz to 13 GHz. The PE43610 features glitch-safe attenuation state transitions, supports 1.8V control voltage and optional V_{SS_EXT} bypass mode to improve spurious performance, making this device ideal for test and measurement, point-to-point communication systems, and very small aperture terminals (VSAT).

The PE43610 provides an integrated digital control interface that supports both serial addressable and parallel programming of the attenuation. The PE43610 covers a 31.5 dB attenuation range in 0.5 dB and 1 dB steps. It is capable of maintaining 0.5 dB and 1 dB monotonicity through 13 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43610 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS} Control

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for the PE43610

Parameter/Condition	Min	Max	Unit
Positive supply voltage, V_{DD}	–0.3	5.5	V
Negative supply voltage, V_{SS_EXT}	–3.6	0.3	V
Digital input voltage	–0.3	3.6	V
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		1000	V
ESD voltage CDM, all pins(2)		500	V

Notes:
1) Human body model (MIL–STD 883 Method 3015)
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommending operating condition for the PE43610. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Condition for the PE43610

Parameter	Min	Typ	Max	Unit
Normal mode, V_{SS_EXT} = 0V(1)				
Positive supply voltage, V_{DD}	2.3	3.3	5.5	V
Positive supply current, I_{DD}(3)		170	260	µA
Bypass mode, V_{SS_EXT} = –3.0V(2)				
Positive supply voltage, V_{DD} (V_{DD} ≥ 3.4V. See Table 3 for full spec compliance.)	3.1	3.4	5.5	V
Positive supply current, I_{DD}(3)		125	170	µA
Negative supply voltage, V_{SS_EXT}	–3.3	–3.0	–2.7	V
Negative supply current, I_{SS}	-40	-16		µA
Normal or bypass mode				
Digital input high	1.17		3.60	V
Digital input low	–0.3		0.6	V
Digital input current(4)		10	20	µA
RF input power, CW(5) (7)			28	dBm
RF input power, pulsed(6) (7)			31	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: Connect V_{SS_EXT} (pin 2) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: Use V_{SS_EXT} (pin 2) to bypass and disable internal negative voltage generator.
3) Due to startup inrush current, a minimum current limit of 600 µA is allowed for normal operation of the DSA.
4) Applies to all pins except pins 18, 22, 23 and 24. $\overline{P}$/S (pin 18), A0/D4 (pin 22), A1/D5 (pin 23), and A2/D6 (pin 24) have internal 1.5 MΩ pull-up resistor to internal 1.8V V_{DD}.
5) 100% duty cycle, all bands, 50Ω.
6) ≤ 5% duty cycle, 50Ω.
7) The maximum peak envelope of any OFDM complex waveform signal, such as CP-OFDM, should not exceed the maximum peak RF input power in Table 1. The maximum average power of any complex waveform should not exceed the operating maximum RF input power, CW.

Electrical Specifications

Table 3 provides the PE43610 key electrical specifications at 25 °C, $Z_S = Z_L = 50\Omega$, unless otherwise specified. Normal mode is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode is at V_{DD} = 3.4V and V_{SS_EXT} = –3.0V.

Table 3 ▪ PE43610 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operation Frequency	9 kHz min frequency	9 kHz		13.00	GHz
Attenuation Range	5-bit, 1.0 dB step programming	0.00		31.00	dB
	6-bit, 0.5 dB step programming	0.00		31.50	dB
Attenuation Error	0.5 dB, 0–31.5 dB step, 9 kHz–13 GHz			+(1.0+4.5% of attenuation setting) / -1	dB
Attenuation Error	1 dB, 0–31dB step, 9 kHz–13 GHz			+(1.0+4.5% of attenuation setting) /-1	dB
Insertion Loss	9 kHz–2 GHz		1.60	1.90	dB
	2–4 GHz		1.80	2.10	
	4–6 GHz		2.00	2.30	
	6–8 GHz		2.20	2.60	dB
	8–13 GHz		2.50	3.00	
Return Loss	All states, 9 kHz–13 GHz		13.00		dB
Relative Phase	All states, 9 kHz–13 GHz		20.00		deg
Input IP2	18 dBm tone @ 13 GHz	95.00			dBm
Input IP3	18 dBm per tone, 20 MHz spacing @ 13 GHz	50.00			dBm
Input 1 dB Compression Pt.	Bi-directional	32.00	34.00		dBm
Input 0.1dB Compression Pt.	Bi-directional	25.00	28.00		dBm
RF Rise and Fall Time	10%/90% RF		250.00		ns
Settling Time	RF settled to within 0.05 dB of final value		500.00		ns
Switching Time	50% CTRL to 90% or 10% RF		330.00	430.00	ns
Attenuation Transient	Any state change		-7.50		dB

Switching Frequency

The PE43610 has a maximum 400 kHz switching rate in normal mode (pin 2 tied to ground). A faster switching rate is available in bypass mode (pin 2 tied to V_{SS_EXT}). The rate at which the PE43610 can be switched is then limited to the switching time as specified in **Table 3**.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spur-free Performance

The PE43610 spur fundamental occurs around 4 MHz. Typical spurious performance in normal mode is –168 dBm/Hz (pin 2 tied to ground), with 30 kHz bandwidth. If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 2).

Glitch-safe Attenuation State

The PE43610 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

Truth Tables

Table 4–**Table 6** provide the truth tables for the PE43610.

Table 4 ▪ Parallel Truth Table

Parallel Control Setting						Attenuation Setting RF1–RF2
D6 (MSB)	D5	D4	D3	D2	D1 (LSB)	
L	L	L	L	L	L	Reference IL
L	L	L	L	L	H	0.5 dB
L	L	L	L	H	L	1 dB
L	L	L	H	L	L	2 dB
L	L	H	L	L	L	4 dB

Table 4 ▪ Parallel Truth Table (Cont.)

Parallel Control Setting						Attenuation Setting RF1–RF2
D6 (MSB)	D5	D4	D3	D2	D1 (LSB)	
L	H	L	L	L	L	8 dB
H	L	L	L	L	L	16 dB
H	H	H	H	H	H	31.5 dB

Table 5 ▪ Serial Address Word Truth Table

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	
L	L	L	L	L	L	L	L	000
L	L	L	L	L	L	L	H	001
L	L	L	L	L	L	H	L	010
L	L	L	L	L	L	H	H	011
L	L	L	L	L	H	L	L	100
L	L	L	L	L	H	L	H	101
L	L	L	L	L	H	H	L	110
L	L	L	L	L	H	H	H	111

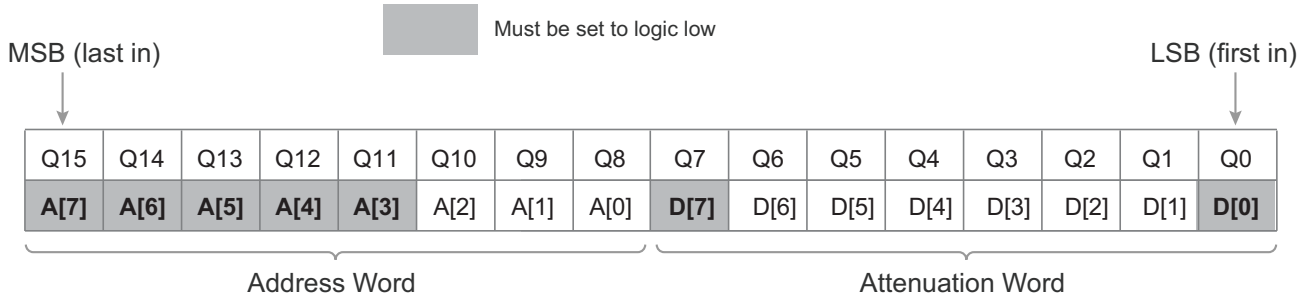
Table 6 ▪ Serial Attenuation Word Truth Table

Attenuation Word								Attenuation Setting RF1–RF2
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	L	31.5 dB

Serial Addressable Register Map

Figure 2 provides the serial addressable register map for the PE43610.

Figure 2 ▪ Serial Addressable Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 18.5 dB state at address 3:

$$4 \times 18.5 = 74$$
$$74 \rightarrow 01001010$$

Address Word: 00000011
Attenuation Word: **01001010**
Serial Input: 00000011**01001010**

Programming Options

Parallel/Serial Selection

Either a parallel or serial addressable interface can be used to control the PE43610. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the parallel interface and $\overline{P}$/S = HIGH selecting the serial interface. The $\overline{P}$/S pin has an internal tie HIGH (namely, the pin is internally tied to the 1.8V V_{DD}), so if this is left floating, the part defaults to serial mode. If there is a need to put this part in parallel mode, a LOW logic should be applied to this pin.

Parallel Mode Interface

The parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 4**.

The parallel interface timing requirements are defined by **Figure 4** (Latched-Parallel/Direct-Parallel Timing Diagram), **Table 10** (Parallel and Direct Interface AC Characteristics) and switching time (**Table 3**).

For latched parallel programming, the latch enable (LE) should be held LOW while changing attenuation state control values then pulse LE HIGH to LOW (per **Figure 4**) to latch new attenuation state into the device.

For direct parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values changes the device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial-Addressable Interface

The serial-addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the attenuation word, which controls the state of the DSA. The second word is the address word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state remains unchanged. **Figure 3** illustrates an example timing diagram for programming a state.

The serial-addressable interface is controlled using three CMOS-compatible signals: SDI, CLK, and LE. The SDI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first. The serial interface data output, SDO, outputs serial input data delayed by 16 clock cycles to control the cascaded attenuator using a single serial peripheral interface (SPI) bus.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Address Word truth table is listed in **Table 5**. The address pins A0 (pin 22), A1 (pin 23), and A2 (pin 24) can either be grounded logic LOW or left floating (logic HIGH due to internal pull-up to 1.8V V_{DD}) depending upon what fixed address the user wants the DSA to be set at.The Attenuation Word truth table is listed in **Table 6**. A programming example of the serial register is illustrated in **Figure 2**. The serial timing diagram is illustrated in **Figure 3**.

Power-up Control Settings

The PE43610 always initializes to the maximum attenuation setting (31.5 dB) on power-up for both the serial addressable and latched parallel modes of operation (as long as the LE pin is logic LOW during start up) and it remains in this setting until the user latches in the next programming word.

In direct parallel mode ($\overline{P}$/S = LOW and logic HIGH present on the LE pin during the power-up), the DSA can be preset to any state within the 31.5 dB range by pre-setting the parallel control pins D[6:1] prior to power-up. In this mode, there is a 4 µs delay between the time the DSA is powered-up to the time the desired state is set. If the control pins are left floating in this mode during power-up, the device defaults to the 28dB attenuation setting.

In latched parallel mode ($\overline{P}$/S = LOW), if the LE pin is kept LOW during power-up, the part should default to maximum attenuation state (31.5dB). Logic LOW should be present on the LE pin during power-up and then logic HIGH should be written on the LE pin when the user wants to program the part. If the LE is kept floating during power-up, the part should default to maximum attenuation state (31.5dB).

In serial mode ($\overline{P}$/S = HIGH or left floating) logic HIGH on the LE pin during the power up: The part should default to minimum attenuation state

(reference state). But a logic LOW on the LE pin during the power up, the part should default to maximum attenuation state.

Dynamic operation between serial and parallel programming modes is not supported.

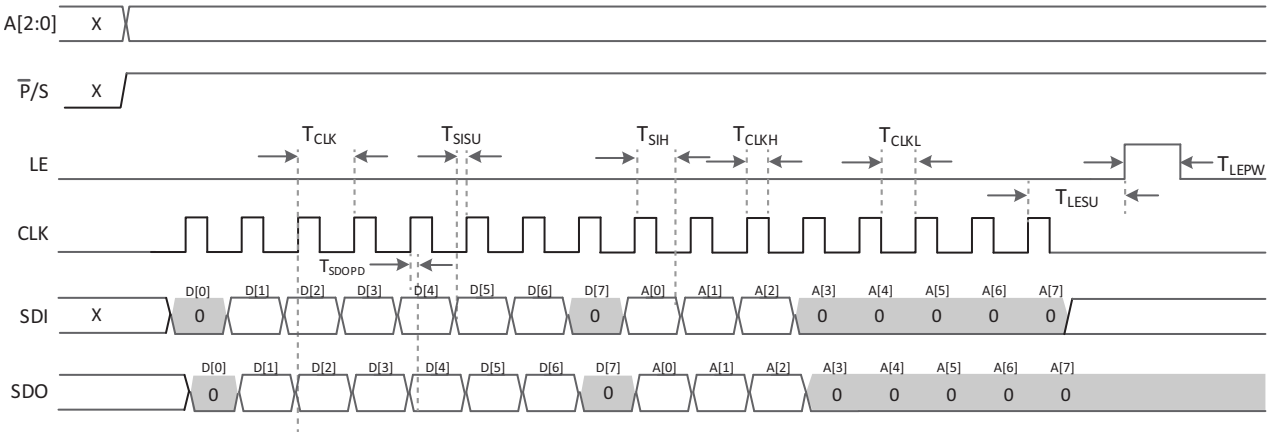
If the DSA powers up in serial mode ($\overline{P}$/S = HIGH), prior to toggling to parallel mode, the user must ensure that the pins LE, SDI/D1, CLK/D2, A0/D4, A1/D5, and A2/D6 are set to logic LOW.

If the DSA powers up in either latched or direct parallel mode, the pins LE, SDI/D1, CLK/D2, A0/D4, A1/D5, and A2/D6 must be set to logic LOW and the pin SDO/D3 set to high impedance prior to toggling to serial addressable mode ($\overline{P}$/S = HIGH).

Table 7 ▪ Summary of Power-up Functionality of the PE43610

Mode	$\overline{P}$/S	LE During Power-up	D[6:1] Pin Status	DSA State at Power-up
Serial mode	1	0		Maximum attenuation
	1	1		Reference state
	1	Floating		Maximum attenuation
Latch parallel mode	0	0	Don't care	Maximum attenuation
	0	Floating	Don't care	Maximum attenuation
Direct parallel mode	0	1	Data present on the D[6:1] lines	Attenuation state depends upon the logic present on the pins D[6:1]
			D[6:1] lines floating	28 dB attenuation state

Figure 3 ▪ Serial Addressable Timing Diagram



Notes:
1. SPI mode 0:
   - SDI data is captured on the CLK's rising edge
   - SDO data is valid on CLK falling edge
2. CLK shared pin with 1 dB parallel control bit D2
3. SDI shared pin with 0.5 dB parallel control bit D1
4. SDO shared pin with 2 dB parallel control bit D3
5. A0 shared pin with 4 dB parallel control bit D4
6. A1 shared pin with 8 dB parallel control bit D5
7. A2 shared pin with 16 dB parallel control bit D6
8. Serial data bits D[7], D[0], and A[7:3] must be set to logic low
9. X = Undefined

Table 8 ▪ Serial Interface AC Characteristics[1]

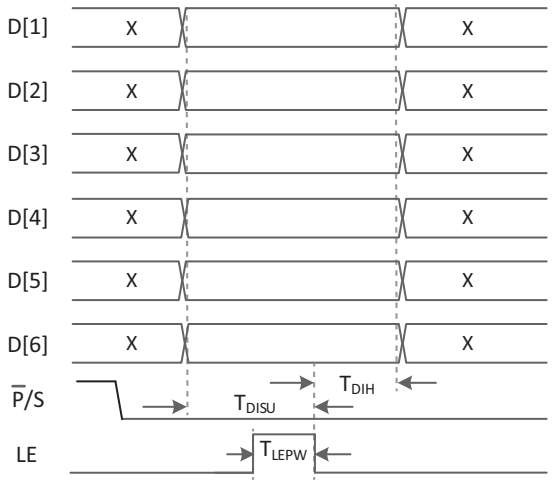
Parameter/Condition	Min	Max	Unit
Serial clock frequency, F_{CLK}		10	MHz
Serial clock time period, T_{CLK}	100		ns
Serial clock HIGH time, T_{CLKH}	30		ns
Serial clock LOW time, T_{CLKL}	30		ns
Last serial clock rising edge setup time to latch enable rising edge, T_{LESU}	10		ns
Latch enable minimum pulse width, T_{LEPW}	30		ns
Serial data setup time, T_{SISU}	10		ns
Serial data hold time, T_{SIH}	10		ns
Serial interface data output (SDO) propagation delay, T_{SDOPD}		30[2]	ns

1) V_{DD} = 3.3V or 5.5V, –40 °C, < T_A < +105 °C, unless otherwise specified.
2) Measured with 10 pF SDO load capacitance.

Table 9 ▪ Latch and Clock Specifications

Latch Enable (LE)	Clock (CLK)	Function
0	↑	Shift register clocked
↑ (rising edge)	X	Contents of shift register transferred to attenuator core

Figure 4 ▪ Latched-Parallel/Direct-Parallel Timing Diagram



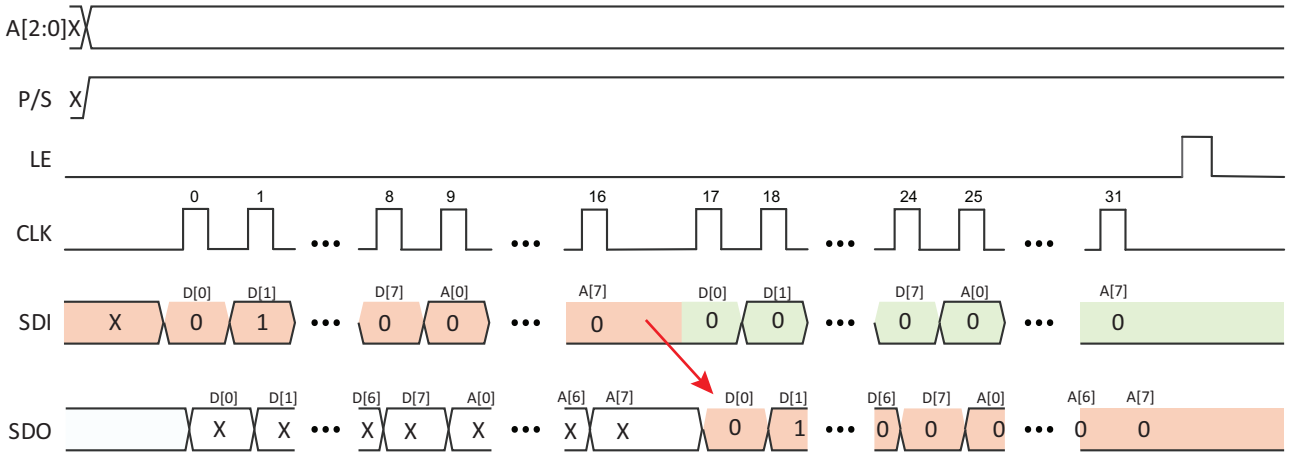
Notes:
1. D1 is shared with serial interface data input SDI
2. D2 is shared with serial interface clock input CLK
3. D3 is shared with serial interface data output SDO
4. D4 is shared with serial address bit A0
5. D5 is shared with serial address bit A1
6. D6 is shared with serial address bit A2
7. X = Undefined

Table 10 ▪ Parallel and Direct Interface AC Characteristics(*)

Parameter/Condition	Min	Max	Unit
Latch enable minimum pulse width, T_{LEPW}	30		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Note: * V_{DD} = 3.3V or 5.5V, –40 °C < T_A < +105 °C, unless otherwise specified.			

The following example shows a scenario where two DSAs are connected in series.

Figure 5 ▪ Serial Addressable Cascaded Devices Example



Example Scenario: 2 DSAs connected in series (SDO to SDI).
First write after power up
Signals from first DSA in chain
X = Undefined

The following table provides the complete SDI and SDO content for the example shown in **Figure 5**.

Figure 6 ▪ Serial Addressable Cascaded Devices Table

	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]
CLK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
SDI	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SDO	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Typical Performance Data

Figure 7–Figure 32 show the typical performance data at 25 °C, $Z_S = Z_L = 50\Omega$, unless otherwise specified.

Figure 7 ▪ Insertion Loss vs. Temperature @VDD 3.3 V

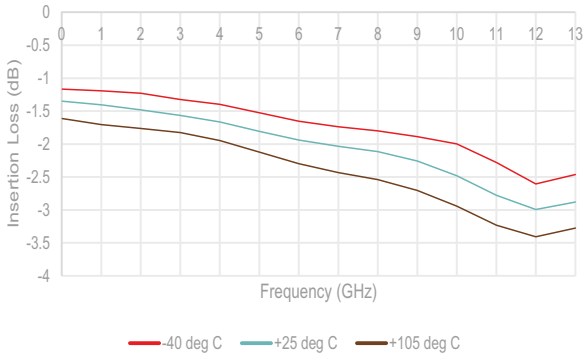


Figure 8 ▪ Input Return Loss (Ref State) vs. Temperature

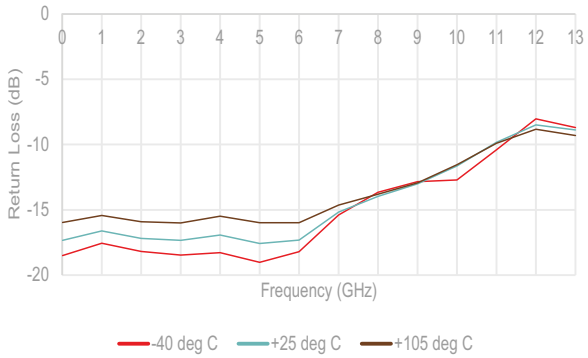


Figure 9 ▪ Input Return Loss (31.5dB Attn) vs. Temperature

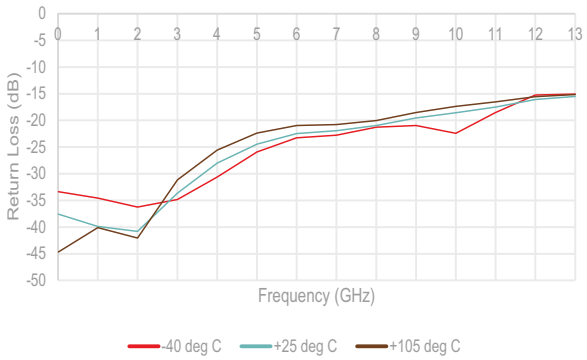


Figure 10 ▪ Output Return Loss (Ref State) vs. Temperature

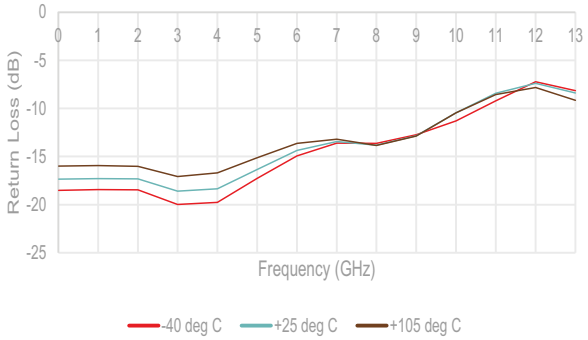


Figure 11 ▪ Output Return Loss (Ref State) vs. Temperature

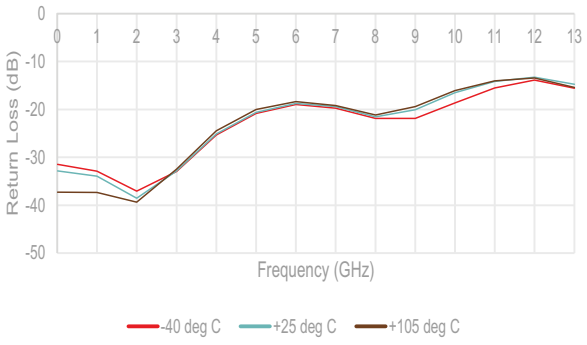


Figure 12 ▪ Input Return Loss (Major Attenuation States)

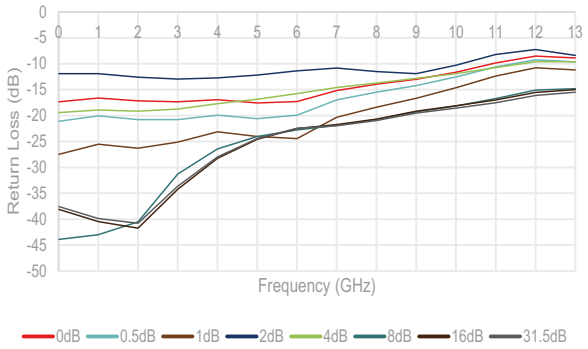


Figure 13 ▪ Input Return Loss (All Attenuation States)

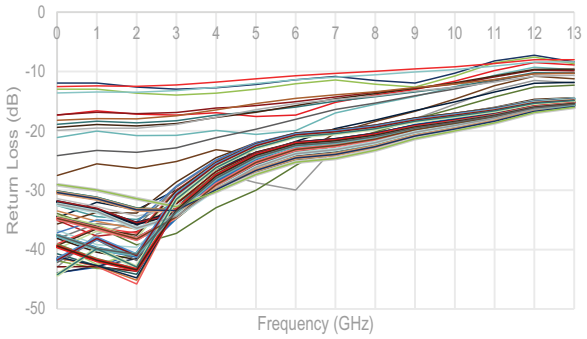


Figure 14 ▪ Output Return Loss (Major Attenuation States)

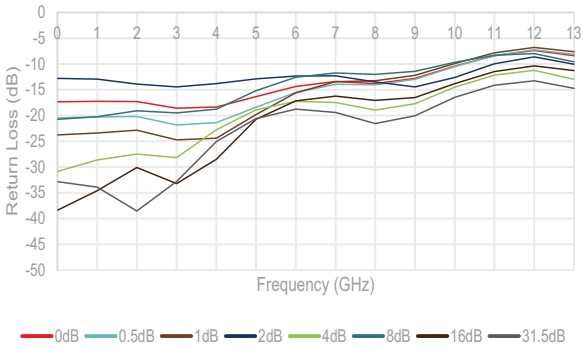


Figure 15 ▪ Output Return Loss (All Attenuation States)

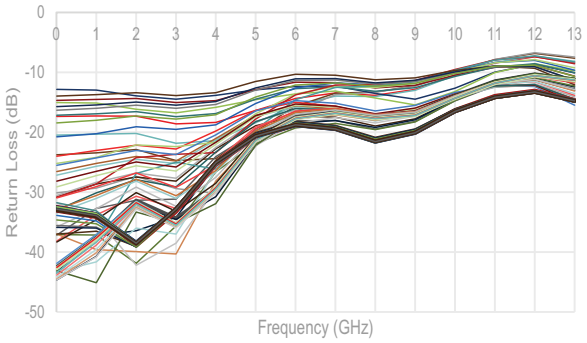


Figure 16 ▪ Relative Phase Error vs. Frequency [GHz]

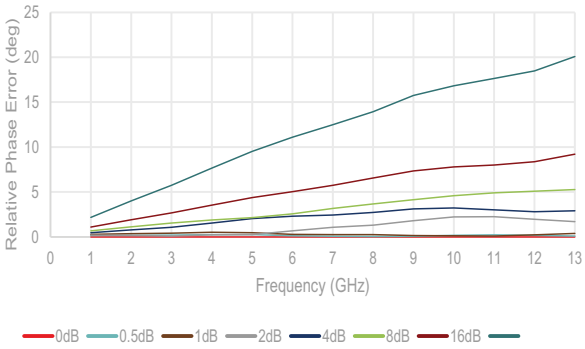


Figure 17 ▪ Relative Phase Error (31.5 dB Attn State) vs Temperature

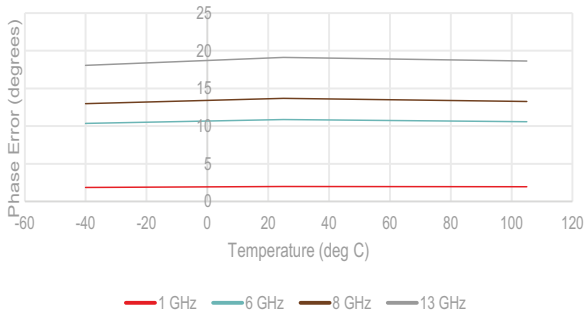


Figure 18 ▪ Attenuation Error @ 1 GHz vs. Temperature

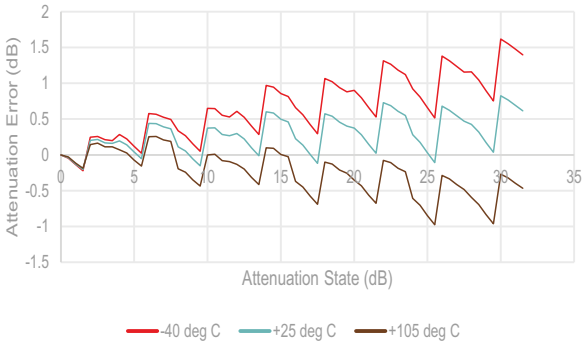


Figure 19 ▪ Attenuation Error @ 6 GHz vs. Temperature

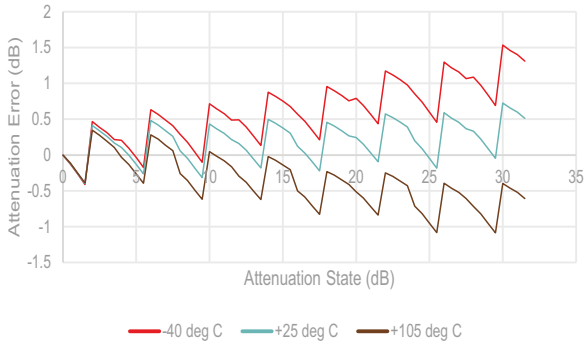


Figure 20 ▪ Attenuation Error @ 8 GHz vs. Temperature

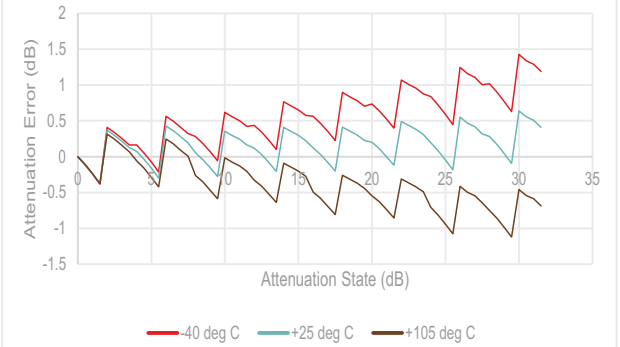


Figure 21 ▪ Attenuation Error @ 13 GHz vs. Temperature

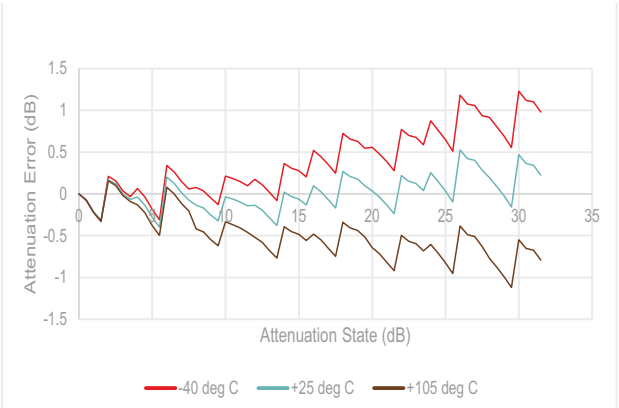


Figure 22 ▪ 0.5 dB Step Attenuation vs Frequency

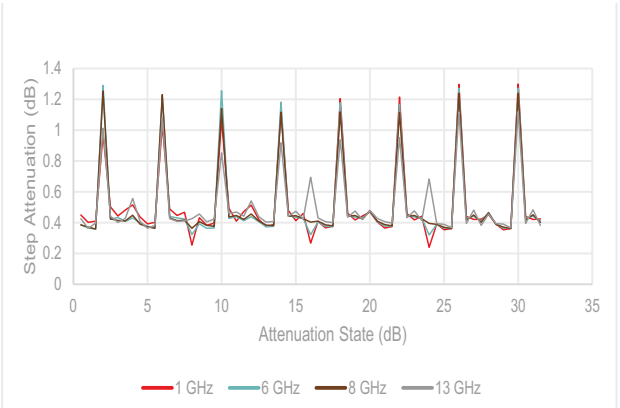


Figure 23 ▪ 1 dB Step Attenuation vs. Frequency

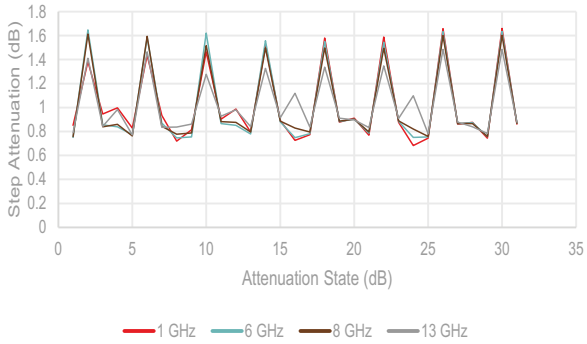


Figure 24 ▪ 0.5 dB Step Actual vs. Frequency

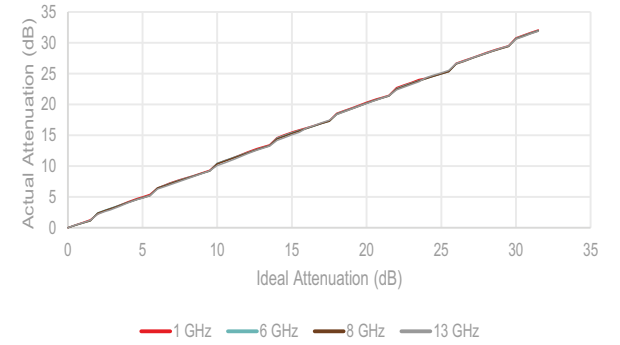


Figure 25 ▪ 1 dB Setup Actual vs. Frequency

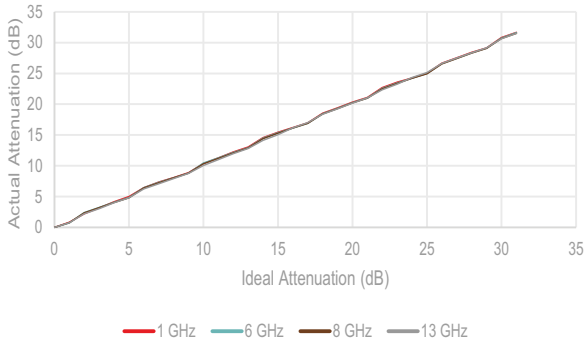


Figure 26 ▪ 0.5 dB Major State Bit Error vs. Attenuation State

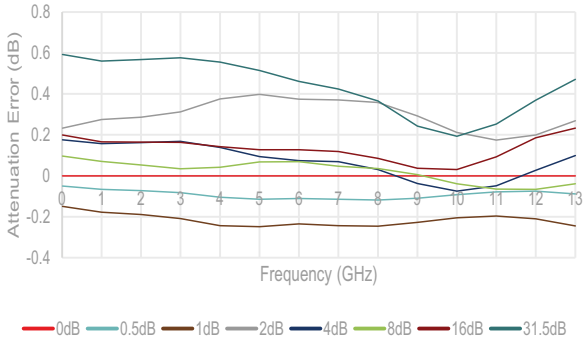


Figure 27 ▪ 0.5 dB Attenuation Error vs. Frequency

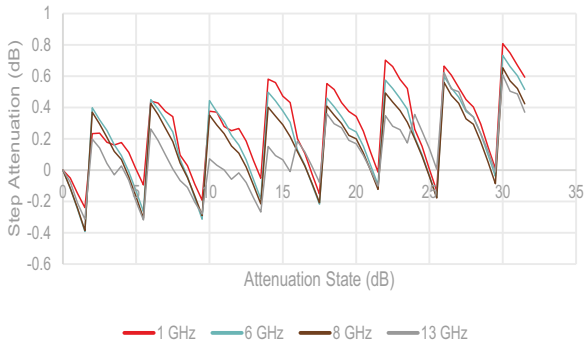


Figure 28 ▪ 1 dB Attenuation Error vs. Frequency

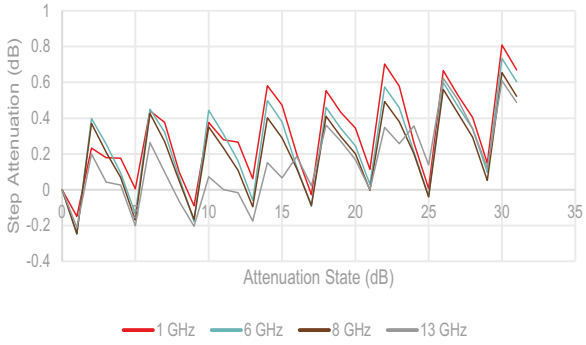


Figure 29 ▪ Attenuation Transient (23.5 dB to 24 dB)

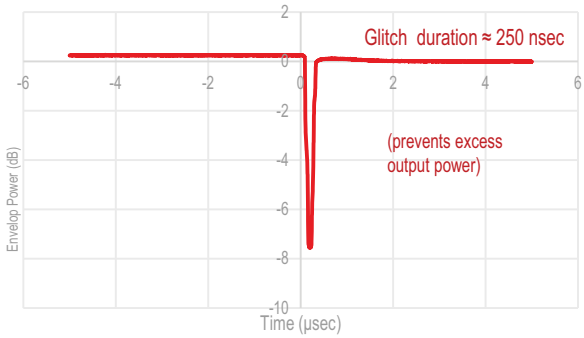


Figure 30 ▪ Attenuation Transient (24 dB to 23.5 dB)

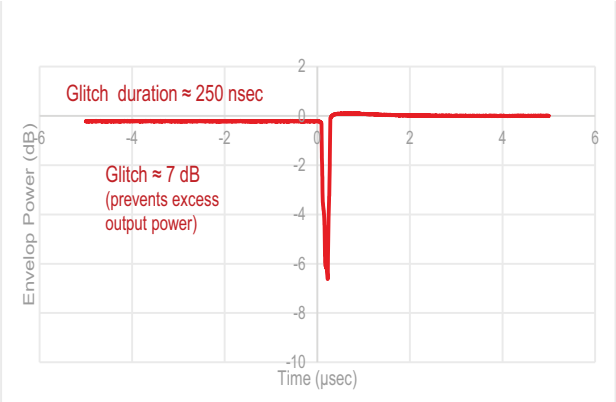


Figure 31 ▪ IIP2

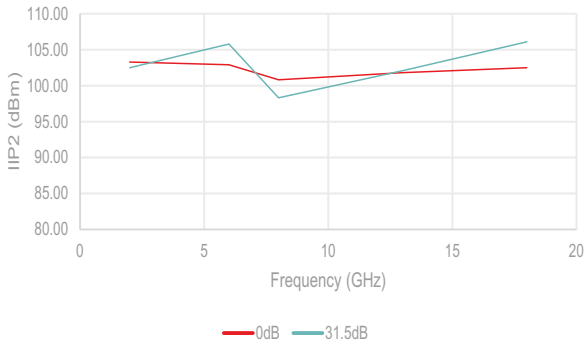
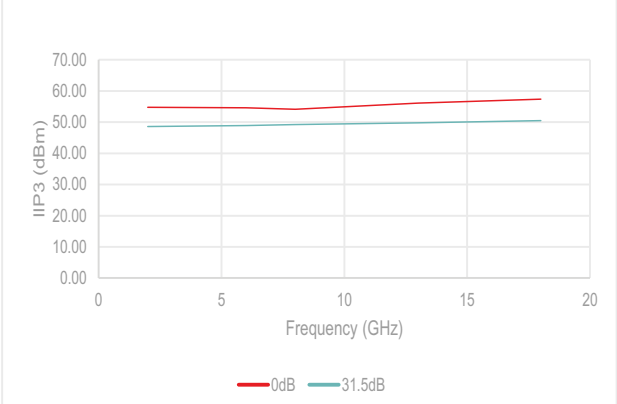


Figure 32 ▪ IIP3



Pin Configuration

This section provides pin information for the PE43610. **Figure 33** shows the pin configuration of this device. **Table 11** provides a description for each pin.

Figure 33 ▪ Pin Configuration (Top View) for the PE43610

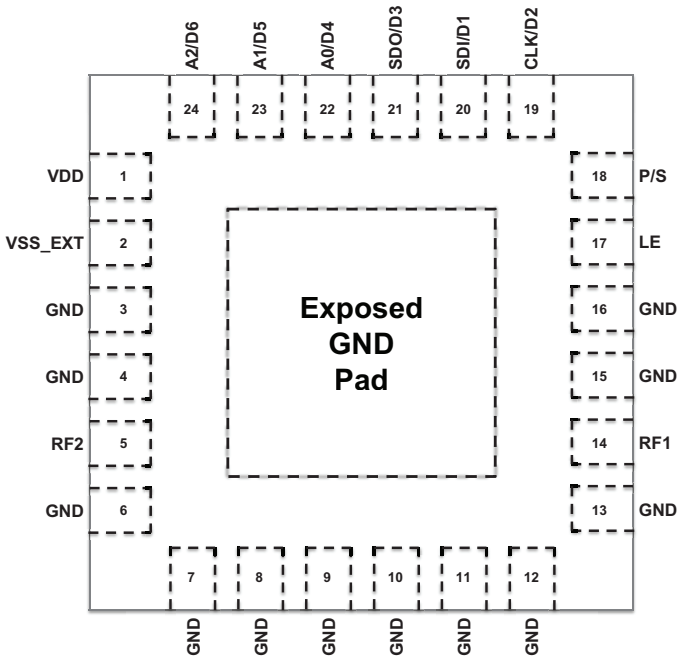


Table 11 ▪ Pin Descriptions for the PE43610

Pin No.	Pin Name	Description
3–4, 6–13, 15–16	GND	Ground
1	V_{DD}	Supply voltage
2	V_{SS_EXT} (3)	External V_{SS} negative voltage control
5	RF2 (1)	RF2 port
14	RF1 (1)	RF1 port
17	LE	Serial/parallel interface latch enable input
18	$\overline{P}$/S (2)	Serial/parallel mode select
19	CLK/D2	Serial interface clock input/parallel control bit, 1 dB
20	SDI/D1	Serial interface data input/parallel control bit, 0.5 dB
21	SDO/D3	Serial interface data output/parallel control bit, 2 dB
22	A0/D4 (2)	Address bit A0 connection/parallel control bit, 4 dB
23	A1/D5 (2)	Address bit A1 connection/parallel control bit, 8 dB
24	A2/D6 (2)	Address bit A2 connection/parallel control bit, 16 dB

Notes:

1) RF pins 14 and 5 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) $\overline{P}$/S (pin 18), A0/D4 (pin 22), A1/D5 (pin 23) and A2/D6 (pin 24) have internal 1.5 MΩ pull-up resistor to internal 1.8V V_{DD}. These pins will have an internal logic HIGH on them if they are left floating by the user. In serial mode, the user can leave the $\overline{P}$/S pin floating and the part will default to serial mode.
3) Use V_{SS_EXT} (pin 2) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 2) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Packaging Information

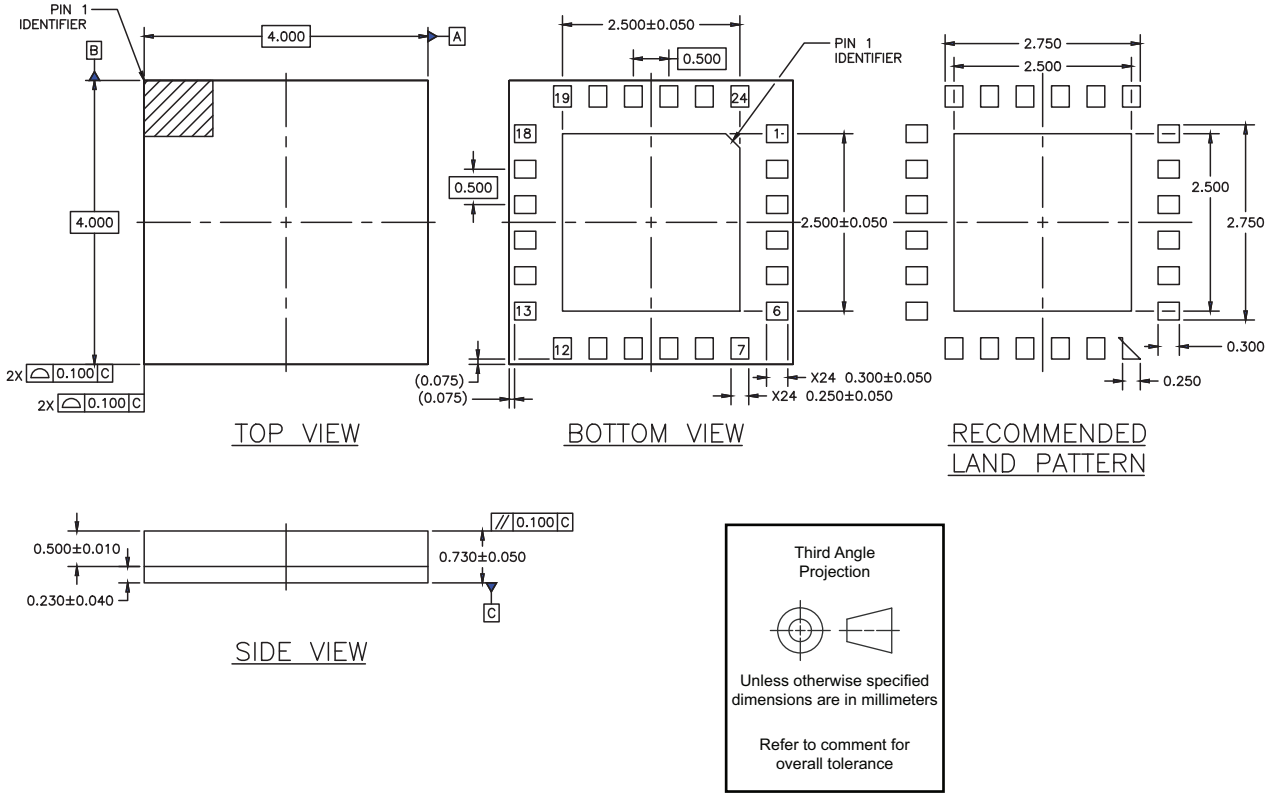
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE43610 in the 24-lead 4 x 4 mm LGA package is MSL 3.

Package Drawing

Figure 34 ▪ Package Mechanical Drawing for 24-lead 4 x 4 mm LGA



Top-Marking Specification

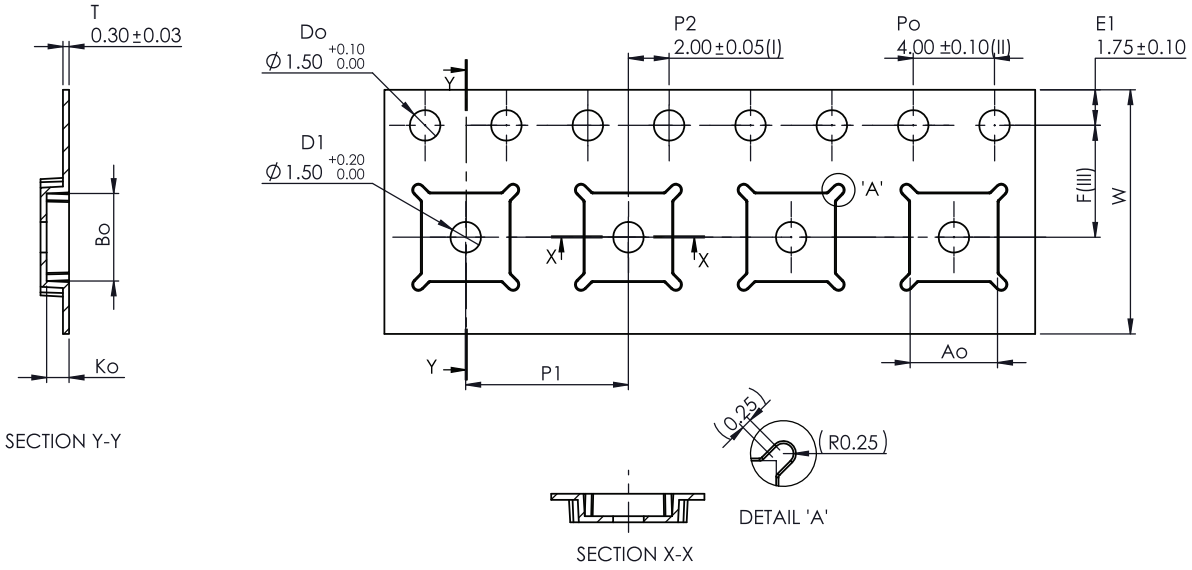
Figure 35 ▪ Package Marking Specifications for PE43610

● = Pin 1 indicator
PPPPP = Product part number
YY = Last two digits of assembly year (2020 = 20)
WW = Work week of assembly lot start date (01, ..., 52)
ZZZZZZ = Assembly lost code (max six characters)

DOC-93635-1

Tape and Reel Specification

Figure 36 ▪ Tape and Reel Specifications for 24-lead 4 x 4 mm LGA

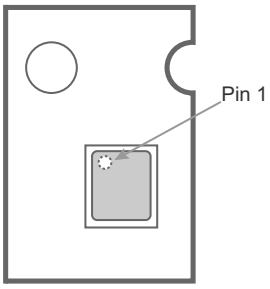


Direction of Feed

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with () is used for design refernce purposes. No measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Ao	4.30	+/- 0.10
Bo	4.30	+/- 0.10
Ko	1.10	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+0.30 / -0.10



Device Orientation in Tape

Ordering Information

Table 12 lists the available ordering code for the PE43610 as well as the available shipping method.

Table 12 ▪ Order Code for the PE43610

Order Codes	Description	Packaging	Shipping Method
PE43610A–X	PE43610 Digital step attenuator	24-lead 4 x 4 mm LGA	500/T&R
EK43610-01	PE43610 Evaluation Kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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