PE42020
Power Supply and Control Logic

Application Note 110

Summary

The PE42020 is a HaRP™ technology-enhanced SPDT true DC RF switch that operates from 0 Hz–8 GHz with integrated RF, analog, and digital functions. The PE42020 true DC RF switch delivers excellent RF performance and high-power handling down to 0 Hz, making this device ideal for handling the complex combination of DC, RF/analog, and digital signals in test and measurement (T&M) and automated test equipment (ATE) applications. With an optimum supply voltage range and the recommended logic pin selection, you can achieve the full performance of the PE42020 across a wide power and frequency operational space.

Introduction

Spurious at low frequency

Having a significant difference between the absolute voltage levels of VDD and VSS can cause spurious to occur at low frequency. The transient startup caused by applying the VSS voltage first can lead to improper operation of the internal bias circuits that generate the bias currents. This can result in spurious generation at low frequencies, as indicated by the yellow no-good (NG) trace in Figure 1, if the subsequently applied VDD level is not well aligned with that of the VSS level.

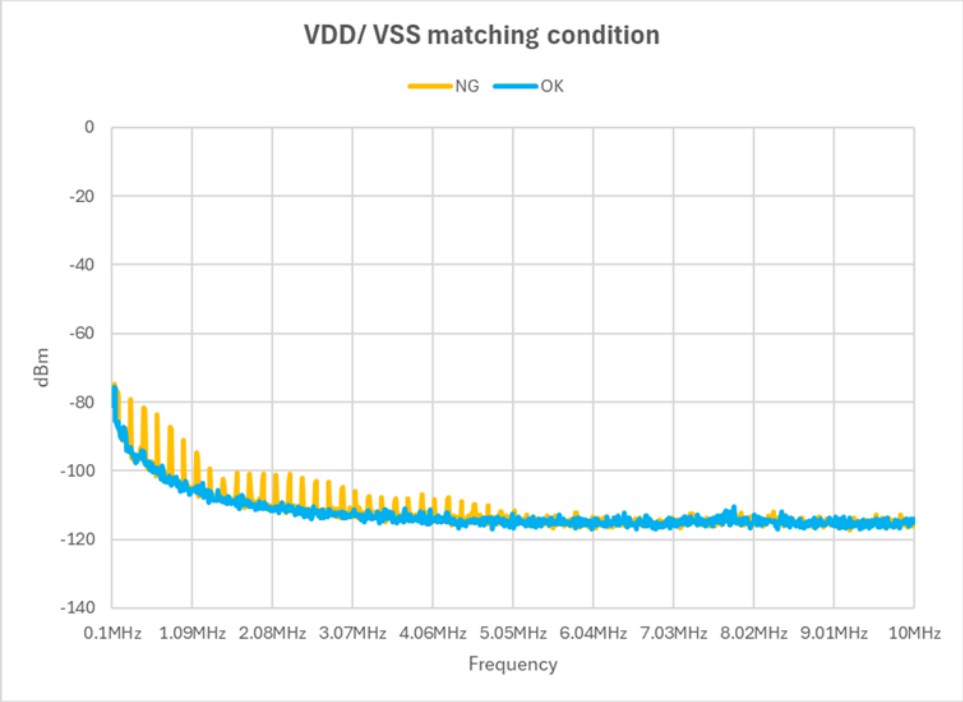

Figure 1. PE42020 low-frequency comparison of spurious (NG) vs. no spurious (OK) performance dependent on the VDD/VSS supply levels

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Figure 2 shows the spurious reference table with the VDD and VSS voltage levels shown in 0.1V steps.

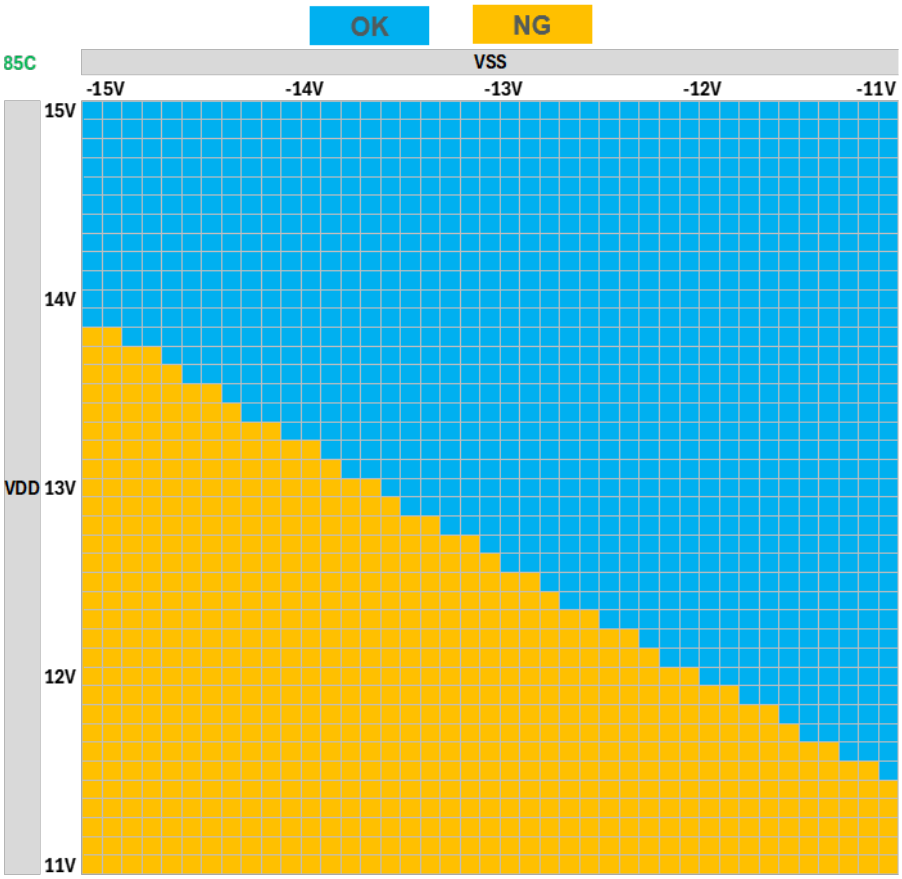

Figure 2. Spurious reference table: OK = no spurious and NG = spurious at low frequency

Follow the power up and power down sequences:

- During the power-up sequence, turn VSS on *before* VDD.
- During the power-down sequence, turn VDD off *before* VSS.

⚠ A mismatch between VDD and VSS must not exceed the absolute maximum of 8%, as described in the *PE42020 Data Sheet*.

Control logic selection

Two PE42020 logic control pins—LS and CTRL—can control the RF1 and RF2 switch path:

- Logic low = -0.3–0.6V
- Logic high = 1.17–3.6V

For high-frequency applications supporting over 30 dBm, pSemi recommends using the LS pin. The CTRL pin, when its digital input high is at its lower range (1.17V), is not as reliable as LS. Figure 3 shows the input and output power plots with various logic control options applied to the evaluation board. As shown, no impact to performance is seen when using the LS pin to control the RF1 and RF2 switch path with the CTRL pin set to 0V across the PIN range.

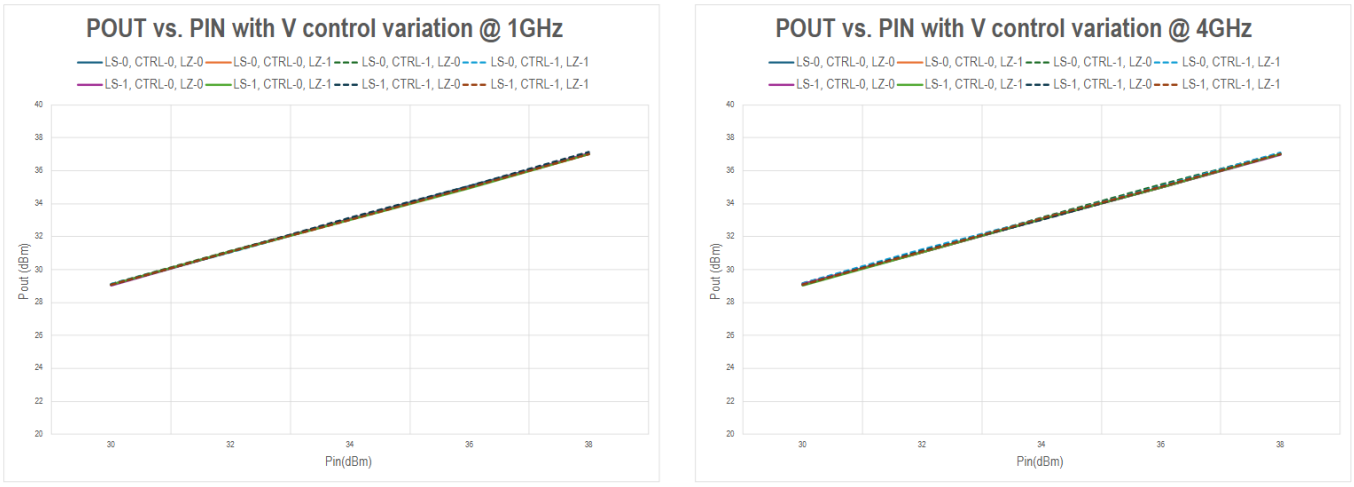

Figure 3. POUT vs. PIN plots with the control logic (Logic 0 = 0V, Logic 1 = 1.17V) with no impact under 4 GHz

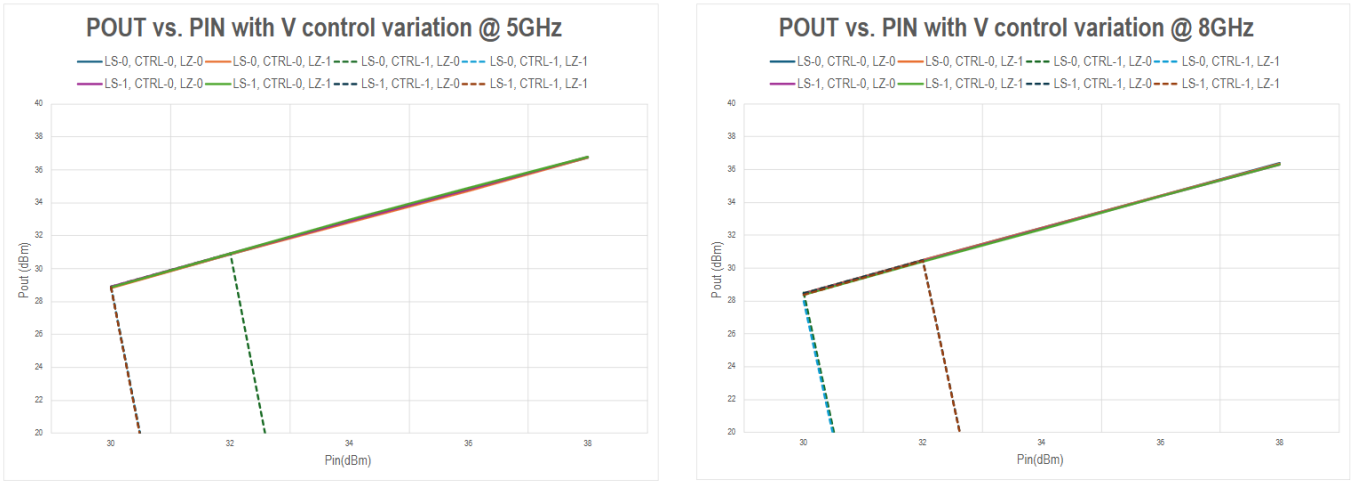

Figure 4. POUT vs. PIN plots with the control logic (Logic 0 = 0V, Logic 1 = 1.17V) with higher insertion loss using CTRL logic high over 5 GHz

In the RFC-RF1 through state with CTRL = 1.17V for digital input high, over 30 dBm PIN causes the logic condition to switch to the RFC-RF2 through state as shown in Figure 5. If the input signal source is located at the RF1 port or the RF2 port, the device could be damaged with over 30 dBm input because the maximum allowed input power at the terminated port is 26 dBm at 8 GHz.

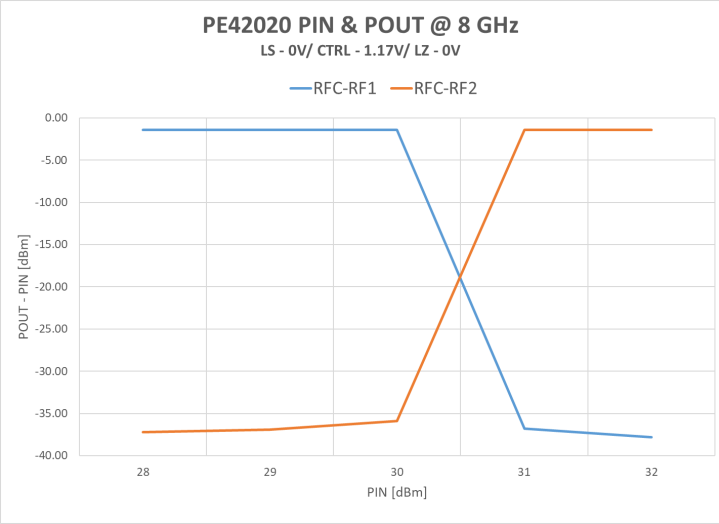

Figure 5. PIN vs POUT at 8 GHz

For proper performance with the minimum digital input high (1.17V) control voltage, use the LS pin with the CTRL pin shorted to GND, as listed in Table 1.

Table 1. Recommended control logic truth table

LS	LZ	CTRL	RFC–RF1	RFC–RF2	Off port terminated
0	0	0	OFF	ON	Yes
0	1	0	OFF	ON	No (high-Z)
1	0	0	ON	OFF	Yes
1	1	0	ON	OFF	No (high-Z)

Conclusion

The power up and power down sequences must be followed before implementing the recommendation discussed in this application note. With proper selection of the VDD and VSS voltage levels and the LS control logic, the PE42020 can achieve its maximum performance as described in the *PE42020 Data Sheet*.

Sales contact

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