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REV

ECN#

DESCRIPTION

DATE

APPROVED

LAYUP DETAIL

2 LAYER

SILKSCREEN (TOP SIDE)

SOLDERMASK (TOP SIDE)

LAYER 1 (TOP SIDE)1.5 oz FINISHED

ISOLA 370 HR

LAYER 2 (BOTTOM SIDE)1.5 oz FINISHED

SOLDERMASK (BOTTOM SIDE)

.71mm (CORE)

.81 +/- .1 mm

TOP to BOTTOM

ALL UNITS ARE IN MILLIMETERS

FIG	FINISHED SIZE	ROTATION	TOLERANCE	PLATED	QTY
x	0.25	-	+0.0/-0.25	PLATED	19
+	0.3	-	+0.0/-0.3	PLATED	666
□	0.95	-	+0.075/-0.075	PLATED	14
◇	1.575	-	+0.05/-0.05	NON-PLATED	1
⊗	1.702x1.575	45.000	+0.05/-0.05	NON-PLATED	1

TOTAL HOLES: 701

36.0mm

56.4mm

DIMENSIONS IN mm/[Inches]

TOLERANCES UNLESS OTHERWISE NOTED

X.X = +/- .25/[.1]

X.XX = +/- .25/[.01]

X.XXX = +/- .127/[.005]

X.XXXX = +/- .0127/[.0005]

ANGLES = +/- 1/2 °

PCB DESIGNER

M. MOREY

ELECTRICAL ENGINEER

L. PRESTIA

PROJECT MANAGER

DATE

03-16-2026

DATE

03-16-2026

DATE

9380 Carroll Park Drive

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PCB, 3X3 12L 75 OHM EVB

SIZE

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RoHS COMPLIANCE

4-24-06

DRAWING NO.

PRT-60916

REV

02

SCALE: 1/1

SHEET 1 of 1

NOTES: UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN METRIC

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.

2. GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES, REMOVE PRIOR TO FABRICATION.

3. FABRICATION VENDOR MAY ADD TEARDROPS, SOLDER TAILS TO PADS IN DUT AREA.

4. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2.

THE DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS.

BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.

5. NUMBER OF ELECTRICAL LAYERS IS 2". SEE LAYER STACKUP DETAIL FOR MATERIALS AND OVERALL THICKNESS.

MINIMUM TRACE WIDTH FOR OUTER LAYERS = .25mm (.010") +/-20%.

MINIMUM AIR GAP FOR OUTER LAYERS = .175mm (.0075") +/-20%.

MINIMUM VIA PAD DIAMETER = .55mm (.022") +/-20%.

NOTE: THIS PCB HAS < .076mm (.003") TRACE/SPACE IN DUT AREA.

6. MATERIAL: LAMINATE AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.

MINIMUM FINISHED EXTERNAL LAYER COPPER WEIGHT = 1 OZ. 1.5 OZ. 2 OZ. MINIMUM.

THE MATERIAL'S GLASS TRANSITION TEMPERATURE (Tg) SHALL BE A MINIMUM OF 170 DEGREES CENTIGRADE.

MATERIAL MUST MEET UL796 WITH A FLAMMABILITY RATING OF 94V-0

VENDOR'S UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE.

7. LAYER TO LAYER REGISTRATION WITHIN .076 (.003"). ALL HOLES TO BE LOCATED WITHIN .076mm (.003") OF ORIGINAL CAD DATA.

ALL HOLES SURROUNDED BY COPPER LAND SHALL HAVE A MINIMUM ANNULAR RING OF .025mm (.001").

ALL PLATED THROUGH HOLES TO HAVE A MINIMUM .025mm (.001") OF PLATING.

HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.

.XX (XXX") VIAS MAY HAVE AN ANNULAR RING OF ZERO

8. PLATING OPTIONS:

X ENIG (ELECTROLESS NICKEL / IMMERSION GOLD) 2-10 MICROINCHES OF GOLD OVER A MINIMUM OF 120 MICROINCHES OF NICKEL PER IPC-4552. THIS FINISH COMPLIES WITH RoHS DIRECTIVES.

SELECTIVE HARD GOLD FINISH IN THE DUT AND POGOPAD AREA(S).

CLASS 1 50-100 MICROINCHES THICK (KNOOP HARDNESS 130-200) OVER NICKEL PLATE IN ACCORDANCE WITH IPC-A-600, LATEST REVISION, SECTION 4.0, CLASS 3 (200-600 MICROINCHES THICK).

HASL (HOT AIR SOLDER LEVEL) SMT PADS MUST BE FLAT TO A MAX OF .003" ABOVE SURFACE. HASL FINISH TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH RoHS DIRECTIVES.

9. APPLY LPI (LIQUID PROTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840 CLASS T TO BOTH SIDES OF PCB. SOLDERMASK COLOR TO BE: X GREEN BLUE RED CLEAR BLACK ORANGE.

GERBER FILES REFLECT A ZERO OVERSIZE. FABRICATION VENDOR MAY OVERSIZE AS NEEDED. MAX THICKNESS .025mm (.001").

IT IS ACCEPTABLE FOR SOLDERMASK WEBBING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.

10. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL SOLDER PADS.

X TOP SIDE ONLY BOTTOM SIDE ONLY BOTH SIDES

11. FABRICATION VENDOR MAY REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS. FABRICATION VENDOR MAY ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.

12. TOLERANCES: WARP AND TWIST NOT TO EXCEED .010 IN/IN, CONDUCTOR WIDTHS/SPACINGS TO BE WITHIN +/-20% OF GERBER DATA. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381mm (.015") MAXIMUM. INSIDE CORNER MAXIMUM RADIUS

X NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.

MATRIX DRAWING PROVIDED, SEE FABRICATION DRAWING SHEET 2 OF 2.

VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY PEREGRINE SEMICONDUCTOR.

PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK AWAY TABS. SEE DETAIL B. SUPPORT RAIL WIDTH TO BE 6.35mm (.25") - 12.7mm (.50") WITH 1.52mm (.060") FIDUCIALS AND 3.175mm (.125") TOOLING HOLES IN 3 CORNERS

PANELIZED SOLDERPASTE GERBER TO BE SUBMITTED TO PEREGRINE SEMICONDUCTOR.

13. PLANARITY:

VARIATION OF BUMP PADS IN THE Z AXIS TO BE <=5um.

ALL 0.XXmm (.XXX") VIAS TO BE EPOXY FILLED AFTER PLATING AND BEFORE FINAL SURFACE FINISH.

NON-CONDUCTIVE EPOXY (SANEI 900 OR EQUIVALENT) IS RECOMMENDED.

EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES.

A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.

ALL OTHER VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.

14. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST "PRT-60916-02.IPC".

15. CONTROLLED IMPEDANCE REQUIREMENTS: FABRICATION VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM PEREGRINE SEMICONDUCTOR.

X VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.

.32mm (.0126") TRACES ON LAYER 1 ARE 75 OHMS, CO-PLANAR TRANSMISSION LINE X +/-5% +/- 10%.

.XXmm (.XXX") TRACES ON LAYER Y ARE 50 OHMS, MICROSTRIP, +/- 10%.

.XXmm (.XXX") TRACES ON LAYER Y ARE 100 OHMS, DIFFERENTIAL, +/- 10%.

16. SHORTS DESIGNED IN BOARD: X NO YES

NET XXXXXX TO GND, LAYER 1

NET XXXXXX TO GND, LAYER 4

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