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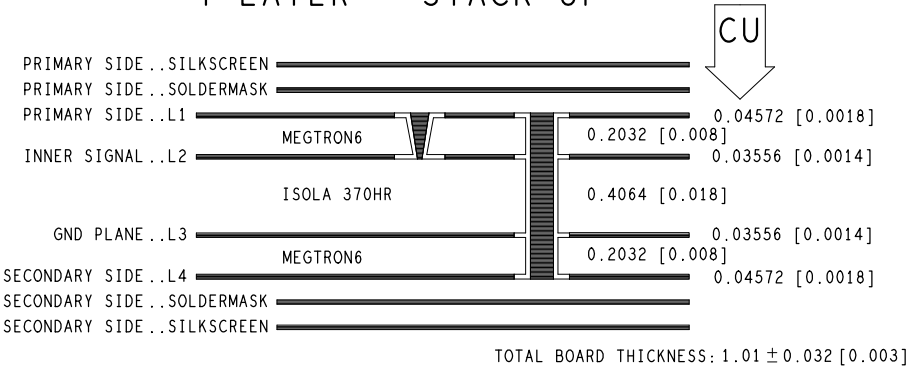
DWG NO.	SH	REV
PRT-89252	1	01

NOTES: UNLESS OTHERWISE SPECIFIED:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
2. GERBER FILES CONTAIN BOARD OUTLINE FOR ALIGNMENT PURPOSES, REMOVE PRIOR TO FABRICATION.
3. FABRICATE PCB PER IPC-6012, LATEST REVISION, TYPE 3, CLASS 2. DETAILED NOTES AND INSTRUCTIONS ON THIS DRAWING SUPERCEDE IPC REQUIREMENTS. BARE BOARD ACCEPTANCE PER IPC-A-600, LATEST REVISION.
4. TRACE WIDTH/SPACE/VIA:
TRACE WIDTHS/SPACING/VIA SIZE TO BE WITHIN $\pm 20\%$ OF GERBER DATA.
MINIMUM TRACE WIDTH: OUTER LAYERS= 0.127 (0.005)
INNER LAYERS= 0.127 (0.005)
MINIMUM AIR GAP: OUTER LAYERS= 0.127 (0.005)
INNER LAYERS= 0.127 (0.005)
MINIMUM VIA PAD DIAMETER: 0.2032 (0.008)
5. MATERIAL:
NUMBER OF ELECTRICAL LAYERS IS 4.
MATERIALS AND OVERALL THICKNESS SEE STACKUP DETAIL.
LAMINATE AND PREPREG PER IPC-4101. COPPER FOIL PER IPC-MF-150.
MATERIAL'S GLASS TRANSITION TEMPERATURE (T_g) SHALL BE A MINIMUM OF 170° CENTIGRADE.
MATERIAL MUST MEET UL796 WITH A FLAMMABILITY RATING OF 94V-0
VENDOR UL LOGO AND DATE CODE TO BE SCREENED ON THE BOTTOM SIDE. IF NO BOTTOM SILKSCREEN PROVIDED VENDOR MAY ADD BOTTOM SILKSCREEN.
6. TOLERANCES:
6A. LAYER TO LAYER REGISTRATION WITHIN 0.076 [0.003].
6B. ALL HOLES TO BE LOCATED WITHIN 0.076 [0.003] OF ORIGINAL CAD DATA.
6C. ALL HOLES SURROUNDED BY COPPER SHALL HAVE A MINIMUM ANNULAR RING OF 0.076 [0.003].
6D. ALL PLATED THROUGH HOLES TO HAVE A MINIMUM 0.025 [0.001] OF PLATING.
6E. HOLE DIMENSIONS AND TOLERANCES APPLY AFTER PLATING, SEE DRILL HOLE CHART.
6F. WARP AND TWIST NOT TO EXCEED 0.254 mm/mm [0.010 IN/IN].
6G. ALL PLATED THROUGH HOLES TO HAVE A MINIMUM 0.025 [0.001] OF PLATING.
7. PLATING OPTIONS: USE 7A
7A. ENIG (ELECTROLESS NICKEL/IMMERSION GOLD) 2-10 MICROINCHES OF GOLD OVER A MINIMUM OF 120 MICROINCHES OF NICKEL PER IPC-4552. THIS FINISH COMPLIES WITH RoHS DIRECTIVES.
~~7B. SELECTIVE HARD GOLD FINISH IN THE BUT AND POCOPAD AREA(S), CLASS 1 50-100 MICROINCHES MICROINCHES THICK (KNOOP HARDNESS 130-200) OVER NICKEL PLATE IN ACCORDANCE WITH IPC-A-600, LATEST REVISION. SECTION 4.0 CLASS 2 (200-600 MICROINCHES THICK).~~
~~7C. HASL (HOT AIR SOLDER LEVEL) SMT PADS MUST BE FLAT TO A MAX OF 0.076 [0.003] ABOVE SURFACE. HASL FINISH TO BE USED ON TEST OR PROTOTYPE BOARDS ONLY. THIS FINISH DOES NOT COMPLY WITH RoHS DIRECTIVES.~~
~~7D. IAG - IMMERSION SILVER 6-20 MICROINCHES PER IPC-4553.~~
8. APPLY LPI (LIQUID PROTO-IMAGEABLE) SOLDERMASK OVER BARE COPPER (SMOBC) PER IPC-SM-840 CLASS "T" TO BOTH SIDES OF PCB. SOLDERMASK COLOR TO BE: GREEN
GERBER FILES REFLECT A ZERO OVERSIZE. VENDOR MAY OVERSIZE AS NEEDED, MAX THICKNESS 0.025 [0.001]. ACCEPTABLE FOR SOLDERMASK WEBBING TO DISAPPEAR BETWEEN FINE PITCH BALL PADS.
9. APPLY SILKSCREEN LEGEND USING WHITE NON-CONDUCTIVE EPOXY INK. TRIM SILKSCREEN FROM ALL EXPOSED COPPER, BOTH SIDE(S).
10. VENDOR MAY REMOVE NON-FUNCTIONAL PADS FROM INTERNAL LAYERS.
11. VENDOR MAY ONLY ADD THIEVING OUTSIDE THE BOARD OUTLINE TO COMPENSATE FOR LOW COPPER DENSITY.
12. REMOVE ALL BURRS AND BREAK SHARP EDGES, INSIDE CORNER MAXIMUM RADIUS 3.81[0.015].
13. BARE BOARD ELECTRICAL TEST IS REQUIRED. USE THE SUPPLIED IPC-D-356 NETLIST.
14. MATRIX DRAWING: USE 14A
~~14A. NO MATRIX DRAWING IS REQUIRED. BOARDS TO BE DELIVERED FULLY ROUTED.~~
~~14B. MATRIX DRAWING PROVIDED. SEE FABRICATION DRAWING SHEET 2 OF 2.~~
~~14C. VENDOR TO GENERATE MATRIX DRAWING. VENDOR GENERATED MATRIX DRAWINGS REQUIRE APPROVAL BY pSEMI CORPORATION. PANELIZED BOARDS TO HAVE SAME ORIENTATION AND SHALL BE ROUTED AND RETAINED WITH BREAK AWAY TABS. SEE DETAIL D. SUPPORT RAIL WIDTH TO BE 6.35[0.25] - 12.7[0.50] WITH 1.52[0.060] FIDUCIALS AND 3.175[0.125] TOOLING HOLES IN 3 CORNERS. PANELIZED SOLDERPASTE GERBER TO BE SUBMITTED TO pSEMI CORPORATION.~~
15. PLANARITY: USE 15B and 15D
~~15A. VARIATION OF BUMP PADS IN THE Z AXIS TO BE $\leq 5\mu m$.~~
15B. ALL VIAS TO BE COPPER FILLED OR NON-CONDUCTIVE EPOXY FILLED AND COPPER OVERPLATED AFTER PLATING AND BEFORE FINAL SURFACE FINISH. NON-CONDUCTIVE EPOXY (SAN EI 900 OR EQUIVALENT) IS RECOMMENDED. EPOXY SHALL NOT PROTRUDE FROM HOLES. THIS APPLIES TO ALL VIAS THAT ARE EXPOSED ON BOTH SIDES. A SMOOTH COPLANAR FINISH IS REQUIRED WHEN EXPOSED BY SOLDERMASK.
~~15C. ALL VIAS ARE TO BE PLUGGED AND FILLED WITH SOLDERMASK MATERIAL.~~
~~15D. MICROVIAS SHALL BE PLATED SHUT AND PLANARIZED. VOIDS IN MICROVIAS SHALL BE LIMITED PER IPC-6012.~~
16. CONTROLLED IMPEDANCE REQUIREMENTS: USE 16B
VENDOR MAY MODIFY DIELECTRIC THICKNESS BY 25% WITHOUT WRITTEN CONSENT. ANY MODIFICATION GREATER THAN 25% REQUIRES WRITTEN CONSENT FROM pSEMI CORPORATION.
~~16A. NO CONTROLLED IMPEDANCE MEASUREMENTS REQUIRED.~~
16B. VENDOR TO PROVIDE TEST COUPON AND IMPEDANCE REPORT.
0.2032 [0.008] TRACES ON LAYER 2 ARE 50 OHMS, MICROSTRIP, +/- 10%.
17. SHORTS DESIGNED IN BOARD: NO
~~NET XXXXXX TO GND, LAYER 1~~
~~NET XXXXXX TO GND, LAYER 4~~
18. DEVIATIONS BY FABRICATION FACILITY TO BE REPORTED TO pSEMI CORPORATION.

REVISIONS				APPROVALS	DATE
ZONE	REV				

4 LAYER - STACK UP



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TOLERANCES UNLESS OTHERWISE NOTED X.X +/- .25/[.1] X.XX +/- .25/[.01] X.XXX +/- .127/[.005] X.XXXX +/- .0127/[.0005] ANGLES +/- 1/2 DEG	CONTRACT NO.		COMPANY	
	APPROVALS	DATE	TITLE	
	DRAWN J. SAMBRANO CHECKED J. DYKSTRA ISSUED	03/10/25 03/10/25	PCB, ALSIP PCB	
MATERIAL			SIZE B	RoHS COMPLIANCE RELEASE DATE
FINISH			DWG NO. PRT-89252	REV 01
DO NOT SCALE DRAWING		REVISIED BY	SCALE: NONE	SHEET: 1 of 1

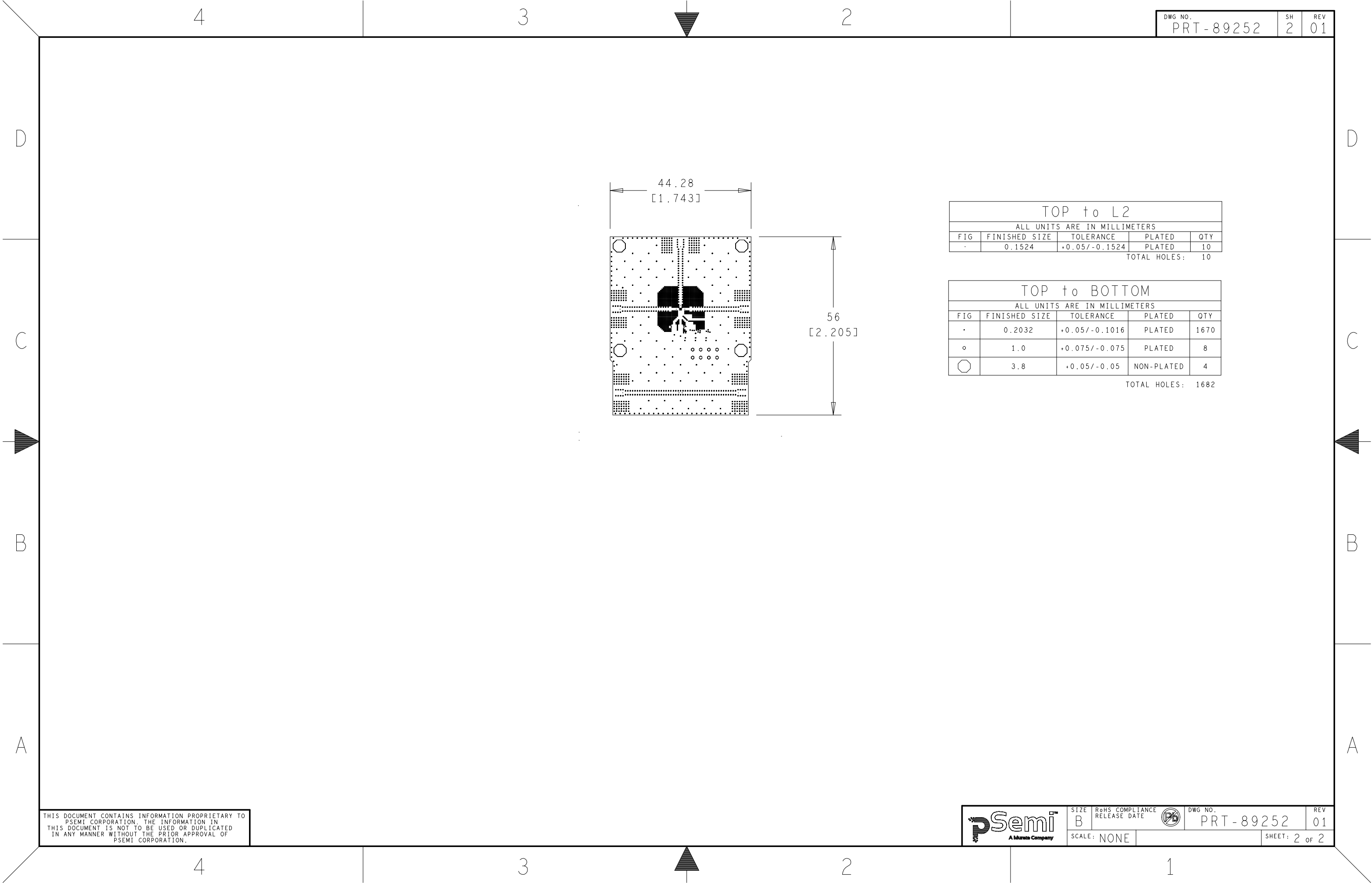
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