ARC2C0608

Document Category: Product Specification

High-efficiency LED Backlight Driver

General Description

The ARC2C0608 is an ultra-high efficiency DC/DC converter solution with integrated programmable current sinks that drive up to six LED strings. The ARC2C0608 integrates all MOSFETs and their control and driver circuitry. With its proprietary architecture, the ARC2C0608 provides the highest efficiency (>94%) possible in a 35-lead compact wafer-level chip scale package (WLCSP). The 0.4 mm pitch and high switching frequency enables small solution size aligned with the needs of the newest mobile products.

Features

- Synchronous DC/DC converter with integrated FETs
- 2-cell Li-Ion battery input voltage: 4.5V to 13.2V
- Patented architecture for ultra-high LED efficiency, above 90% over entire operating range
- Integrated output disconnect switch
- Up to 30V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- 12 bits hybrid (mixed) linear dimming mode and 10 bits logarithmic mapping
- Up to 12 bits resolution with DC or PWM dimming
- Supports direct PWM dimming for maximum flexibility and resolution
- LED brightness ramp-up/ramp-down control with programmable ramp rate and linear/logarithmic ramp profiles
- Phase-shifted PWM dimming among active strings to minimize audible noise
- 1 MHz I²C 3.0-compatible serial interface to program the brightness, or an external resistor on ISET to set the maximum brightness
- External PWM input for fine dimming resolution
- Six independently enabled current sinks, up to 30 mA per current sink, and up to 40 mA for lower string counts or lower V_{OUT}
- 0.5% typical current matching accuracy at 30 mA
- Wide range of input and output voltages with 2x charge pump ratio
- Selectable boost switching frequency from 320 kHz to 3.4 MHz
- Extensive fault protection including boost over current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Applications

2-cell platforms, including the following:

- Ultrabooks and ultraportable notebooks
- 2-in-1, convertible, and detachable notebooks
- Full-size tablet computers
- LCD panels
- Ultra-thin form factor mobile platforms

Efficiency

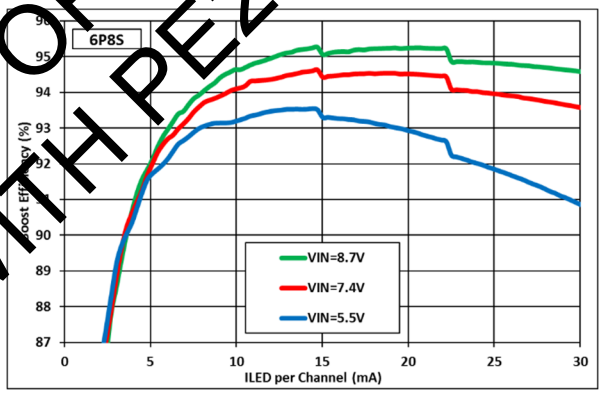

Figure 1. Typical Boost Efficiency (6p8s)

Application

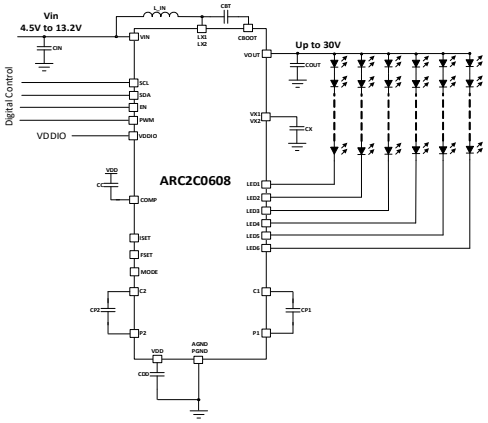

Figure 2. Typical Application Circuit

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Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. ARC2C0608 Absolute Maximum Ratings

Parameter	Min	Max[1]	Unit
VIN to AGND	-0.3	17.6	V
VDD, VDDIO, PWM, COMP, EN, ISET, MODE, FSET, SCL, and SDA to AGND	-0.3	6	V
VDDP to AGND	-0.3	6	V
VOUT, C1, C2 to PGND	-0.3	32	V
LEDx to AGND	-0.3	26.4	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1, and P2 to PGND	-0.3	17.6	V
VX to LX	-0.3	17.6	V
CBOOT to VDD	-0.3	17.6	V
CBOOT to LX	-0.3	6	V
C1, C2 to VX	-0.3	17.6	V
VOUT to C1, C2	-0.3	17.6	V
Storage temperature	-65	150	°C
Junction temperature (J_T)	–	150	°C
Bump or lead temperature (soldering and reflow)	–	260	°C
ESD tolerance, HBM[2]	–	2000	V
ESD tolerance, CDM[3]	–	750	V

Notes:

1. These “Absolute Maximum Ratings” are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human body model, per JEDEC standard JS-001-2012.
3. Field-induced charge device model, per JEDEC standard JESD22-C101.

Recommended Operating Conditions

Table 2 lists the ARC2C0608 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. ARC2C0608 Recommended Operating Conditions

Parameter	Min	Max	Unit
VIN input voltage range	4.5	13.2	V
VOUT output voltage range, relative to AGND or PGND	18	30	V
VX boost output voltage range	1.2 × VIN	16	V
VDDIO voltage range	1.08	3.63	V
Junction temperature range, T_J	-30	+125	°C

Package Thermal Characteristics

Table 3 lists the package thermal characteristics.

Table 3. Package Thermal Characteristics[1][2]

Parameter	Max	Unit
Junction-to-ambient thermal resistance (Θ_{JA}), soldered thermal pad, connected to plane	44.4	°C/W
Junction-to-board thermal characterization (Ψ_{JB})	10.8	°C/W
Junction-to-top case thermal characterization (Ψ_{JC})	6.5	°C/W

Notes:

1. Package thermal characteristics and performance are measured and reported in a manner consistent with JEDEC standards JESD51-8 and JESD51-12.
2. Junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight/routes, and air flow. To realize the expected thermal performance, pay close attention to the board layout.

Electrical Specifications

Table 4 lists the ARC2C0608 key electrical specifications at the following conditions, unless otherwise noted. Typical values are at 25 °C with 6p8s.

V_{IN} = 7.4V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -30 °C to +85 °C

Table 4. ARC2C0608 Electrical Specifications(1)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input supply							
Input voltage range	V_{VIN}	Full parametric performance		4.5	–	13.2	V
Voltage regulator output voltage	V_{DD}	–		–	4.0	4.4	V
Under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{VIN} rising		–	4.275	4.45	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	–		–	75	–	mV
Shutdown supply current	I_{VIN_SD}	IVIN with VEN = 0V		–	–	1	µA
Standby supply current	I_{VIN_STDBY}	VEN = 1.8V, I2C_STDBY = 1		–	–	175	µA
Supply voltage for digital I/O	V_{DDIO}	–		1.08	–	3.63	V
Supply current for digital I/O	I_{VDDIO}	EN = 0V or 1.8V, SDA = SCL = 0V or VDDIO, measure at VDDIO = 1.8V		–	8	–	µA
Thermal shutdown threshold(3)	T_{TSD}	–		–	150	–	°C
Thermal shutdown hysteresis(3)	T_{TSD_HYST}	–		–	20	–	°C
Soft start timeout duration	–	–		–	10	–	ms
Step-up converter: boost							
Boost switching frequency range	f_{SW_BOOST}	I²C interface only FSW_BOOST[4:0]	13h	–	–	–	MHz
			09n	–	–	–	
			05h	–	–	–	
			03h	–	–	–	
		Non-I²C interface only	FSET = VDD	–	2.56	–	
			FSET = Open	–	1.024	–	
			FSET = AGND	–	0.512	–	
Boost switching frequency accuracy	–	–		-10	–	+10	%
Boost minimum off-time	$T_{OFF\_BOOST\_MIN}$	–		–	50	–	ns
Boost minimum on-time	$T_{ON\_BOOST\_MIN}$	–		–	50	–	ns
Boost low-side switch current limit, cycle-by-cycle	I_{BOOST_LIMIT}	I_{LX} rising		–	2.9	–	A
VOUT-COMP transconductance(2)	g_m	I_{LX} rising		–	1.56	–	µA/V

Gm amplifier unity gain bandwidth	F_O	20 KΩ on COMP pin		–	1.9	–	MHz
Gm amplifier max source current	–	–		–	8	–	µA
Gm amplifier max sink current	–	–		–	8	–	µA
Step-up converter: charge pump							
Output voltage range[2,8]	V_{OUT}	V_{VIN} =4.5V~8.7V		18	–	30	V
Maximum continuous load current	I_{OUT}	–		180	–	–	mA
Output over-current threshold	I_{OUT_OC}	I_{OUT} rising		250	–	–	mA
Output over-voltage threshold	V_{OUT_OVP}	OVP_{TH}[1:0]	00	–	31.4	–	V
			01	–	24	–	
			10	–	20	–	
Output over-voltage hysteresis	$V_{OUT\_OVP\_HYST}$	–		–	0.5	–	V
Accuracy of output over-voltage protection threshold	–	–		-4	–	+4	%
LED current sinks (LED1 to LED6)							
ISET voltage	V_{ISET}	–		–	0.4	–	V
ISET pin voltage accuracy[7]	–	–		-3.25	–	4.0	%
ISET recommended resistor range	R_{ISET}	Excluding resistor tolerance		24.9	–	250	kΩ
Current multiplier	K_{ISET}	I^2C register setting MAX_I[1:0]	00	–	937.5	–	A/A
			01	–	1250	–	
			10	–	1562.5	–	
			11	–	1876	–	
LED current full-scale output range	I_{LED_MAX}	I^2C register setting MAX_I[1:0]	00	–	15	–	mA
			01	–	20	–	
			10	–	25	–	
			11	–	30	–	
Minimum sink current LED1–6	I_{LED_MIN}	I_{LED} programmed to 30 mA		–	7.3	–	µA
Leakage current	$I_{LED\_LEAKAGE}$	LEDEN1…6 = 0, V_{OUT} = 26.4V		–	–	1	µA
LED current matching[4]	$I_{LED\_MATCHING}$	I_{LEDX} programmed to 30 mA, T_A = 25 °C, DC IDAC output		–	0.5	–	%
LED current accuracy[4]	$I_{LED\_ACCURACY}$	I_{LEDX} programmed to 30 mA, T_A = 25 °C, DC IDAC output		-3	–	+3	%
LED dropout voltage	$V_{LED\_REGULATION}$	I_{LEDX} programmed to 30 mA, T_A = 25 °C, DC IDAC output		–	180	–	mV
LED shorted string detection threshold	–	V_{LEDX} rising		–	6.3	–	V
Current ripple[2]	–	I_{LEDX} programmed to 30 mA, T_A = 25 °C, DC IDAC output		–	1	–	%

Internal PWM dimming						
Transition point between internal PWM and analog dimming[6]	–	DIM_MODE = 0	–	0	–	%
		DIM_MODE = 1 PVWM-IX[1:0] 00	–	12.5	–	
		DIM_MODE = 1 PVWM-IX[1:0] 01	–	25 (default)	–	
		DIM_MODE = 1 PVWM-IX[1:0] 10	–	50	–	
		DIM_MODE = 1 PVWM-IX[1:0] 11	–	100	–	
		Non-I²C mode	–	25	–	
LED PWM output frequency	f_{LEDX}	Non-I²C mode with MODE pin floating	–	2.5	–	kHz
		DIMCODE[1:0] = 00, 10, or 01 in I²C mode	2.5	–	40	
LED current sink minimum output pulse width	–	–	–	200	–	ns
Direct PWM dimming						
Direct PWM input to output timing skew	–	–	–	-25	–	ns
Logic interface (EN, PWM, and FSET)						
EN logic input high voltage	V_{IH_EN}	–	1.1	–	–	V
EN logic input low voltage	V_{IL_EN}	–	–	–	0.4	V
PWM logic input high voltage	V_{IH_PWM}	–	0.9	–	–	V
PWM logic input low voltage	V_{IL_PWM}	–	–	–	0.5	V
Logic input current	$I_{PWM, IEN}$	–	-1.0	–	1.0	µA
FSET input resistance	I_{FSET_R}	Non-I²C mode only	–	100	–	kΩ
FSET input low voltage	V_{IL_FSET}	Non-I²C mode only	–	–	0.4	V
FSET input high voltage	V_{IH_FSET}	Non-I²C mode only	V_{DD} - 0.4	–	–	V
MODE pin input resistance	I_{MODE_R}	Non-I²C mode only	–	100	–	kΩ
MODE pin input low voltage	V_{IL_MODE}	Non-I²C mode only	–	–	0.4	V
MODE pin input high voltage	V_{IH_MODE}	Non-I²C mode only	V_{DD}- 0.4	–	–	V
PWM pin input frequency for internal PWM mode	F_{IPWM}	–	0.2	–	40	kHz
PWM pin input frequency for direct PWM mode	F_{DPWM}	–	0.2	–	20	KHz
PWM pin minimum input high pulse	–	–	100	–	–	ns
PWM pin minimum input low pulse	–	–	100	–	–	ns
I²C serial interface (SCL, SDA, and VDDIO)						
VDDIO supply voltage range	V_{DDIO}	–	1.08	–	3.63	V

SDA, SCL input high voltage	V_{IH}	–	0.7 × V_{DDIO}	–	3.6	V
SDA, SCL input low voltage	V_{IL}	–	–	–	0.3 × V_{DDIO}	V
SDA, SCL input hysteresis	V_{HYS}	–	0.05 × V_{DDIO}	–	–	V
SDA, SCL input current	I_{SCL}, I_{SDA}	–	-1	–	1	µA
SDA output low level	V_{OL}	I_{SDA} = 20 mA	–	–	0.4	V
I^2C interface initial wait time	–	Initial wait time from EN logic high to the first I^2C command	1000	–	–	µs
SDA, SCL pin capacitance(2)	$C_{I/O}$	–	–	–	10	pF
I^2C interface timing characteristics for standard mode, fast mode, and fast mode plus						
Serial clock frequency	F_{SCL}	Standard mode	–	–	100	kHz
		Fast mode	–	–	400	
		Fast mode plus	–	–	1000	
Clock low period	t_{LOW}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Clock high period	t_{HIGH}	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
BUS free time between a STOP and a START condition	t_{BUF}	Standard mode	4.7	–	–	µs
		Fast mode	1.3	–	–	
		Fast mode plus	0.5	–	–	
Setup time for a repeated START condition	$t_{SU:STA}$	Standard mode	4.7	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Hold time for a repeated START condition	$t_{HD:STA}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Setup time of STOP condition	$t_{SU:STO}$	Standard mode	4	–	–	µs
		Fast mode	0.6	–	–	
		Fast mode plus	0.26	–	–	
Data setup time	$t_{SU:DAT}$	Standard mode	0.25	–	–	µs
		Fast mode	0.1	–	–	
		Fast mode plus	0.05	–	–	
Data hold time	t_{HD_DAT}	Standard mode	0	–	–	µs
		Fast mode	0	–	–	
		Fast mode plus	0	–	–	
Rise time of SCL signal	t_{RCL}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	

		Fast mode plus	–	–	0.12	
Fall time of SCL signal	t_{FCL}	Standard mode	–	–	0.3	µs
		Fast mode	–	–	0.3	
		Fast mode plus	–	–	0.12	
Rise time of SDA signal	t_{RDA}	Standard mode	–	–	1	µs
		Fast mode	0.02	–	0.3	
		Fast mode plus	–	–	0.12	
Fall time of SDA signal(2)	t_{FDA}	Standard mode	–	–	0.3	µs
		Fast mode	20 × V_{DDIO}/ 5.5V	–	0.3	
		Fast mode plus	20 × V_{DDIO}/ 5.5V	–	0.12	
Data valid time	t_{VD}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Data valid acknowledge time	t_{VDA}	Standard mode	–	–	3.45	µs
		Fast mode	–	–	0.9	
		Fast mode plus	–	–	0.45	
Capacitive load for SDA and SCL	C_{BUS}	Standard mode	–	–	400	pf
		Fast mode	–	–	400	
		Fast mode plus	–	–	550	

Notes:

1. The minimum and maximum specifications are 100% production tested at T_A = 25 °C, unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Guaranteed by design.
3. Thermal shutdown is not production tested.
4. The LED current accuracy is defined/tested as: 100 × (ILED_AVG-ILED_Target)/ILED_AVG. The sink current matching is defined/tested as (ILED_MAX-ILED_MIN)/ILED_AVG.
5. Dropout voltage is the LEDx voltage at which the current has decreased by 1% relative to its value when the LEDx voltage is 1V.
6. The default is 25%. It can be trimmed to 0, 12.5%, 50%, or 100% if needed for non-I²C mode.
7. If the ISET pin is used the LED full scale current is trimmed to compensate for voltage variation.
8. At very light loads in DCM mode, VOUT could be higher than expected. However, the LED current regulation is not adversely affected.

I²C Timing Diagram

Figure 3 shows the ARC2C0608 serial interface timing for standard mode, fast mode, and fast mode plus.

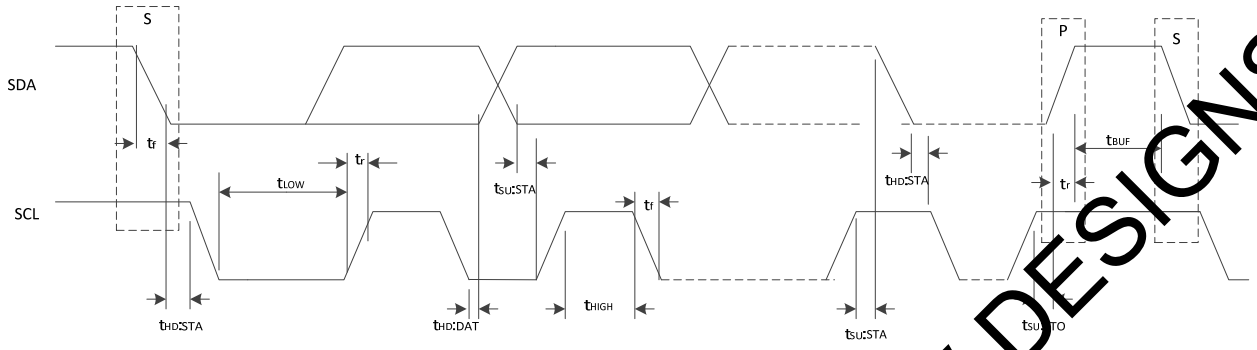

Figure 3. Serial Interface Timing Diagram for Standard Mode, Fast Mode, and Fast Mode Plus

Pin Configuration

Figure 4 shows the ARC2C0608 pin map for the 2.985 mm × 2.315 mm WLCSP.

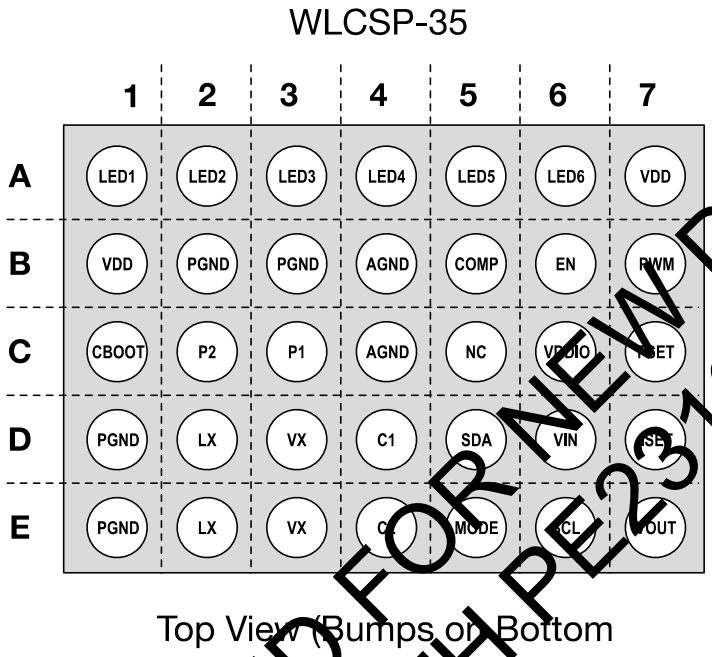

Figure 4. Pin Configuration (Top View, Bumps on Bottom)

Pin Descriptions

Table 5 lists the ARC2C0608 pin descriptions. For the capacitor and inductor selection guidelines, see Component Selection on page 49.

Table 5. ARC2C0608 Pin Descriptions

Pin No.	Pin Name	Description
D6	VIN	Input voltage, battery power supply pin.
D2, E2	LX	Fully synchronous switching node for the boost power inductor, which connects between LX and the input voltage.
E5	MODE	Float this pin or tie it to ground or VDD (LDO output only) to select one of three LED current output options in non-I²C mode. For details, see the Application Schematic on page 48.
D4	C1	Externally connect the charge pump fly capacitor between C1 and P1.
E4	C2	Externally connect the charge pump fly capacitor between C2 and P2.
C3	P1	Phase node for charge pump fly capacitor C1.
C2	P2	Phase node for charge pump fly capacitor C2.
C1	CBOOT	Bootstrap capacitor for Boost stage high side FET.
D3, E3	VX	Charge pump input node, internally driven by output of boost converter. Connect externally to CX capacitor. For details, see the Application Schematic on page 48.
E7	VOUT	Power converter output voltage. Connect to the high side of all LED strings.
B7	PWM	PWM dimming input for brightness control. If not used, connect to VDD.
B5	COMP	Compensation pin.
A1-A6	LEDx	Individual LED current sink. Connect to the low side of the individual LED strings.
B4, C4,	AGND	Analog ground. Tie externally to the ground plane.
B2, B3, D1, E1	PGND	Power ground. Tie externally to the ground plane. High current path.
E6	SCL	Serial clock for I²C bus. Also used in non-I²C mode for current setting using IMAXTUNE.
D5	SDA	Serial data for I²C bus. Also used in non-I²C mode for current setting using IMAXTUNE.
D7	ISET	LED current setting pin. Connect a resistor from this pin to AGND to set the full-scale LED current in non-I²C mode or when the ISET_EXT bit is set to high in I²C mode.
C6	VDDIO	Digital I/O supply voltage for the I²C interface.
B1	VDD	Internal LDO output pin. Connect capacitor CVDD between this pin and AGND. Use this pin to power FSET and MODE. Can also be used as pull up for PWM, (and SDA and SCL in non-I²C mode).
A7	VDD	Short this pin to the VDD pin.
B6	EN	Enable input.
C7	FSET	Float this pin or tie it to ground or VDD (LDO output only) to set the boost switching frequency in non-I²C mode. For details, see the Application Schematic on page 48.
C5	NC	Not connected internally. Can be connected to ground plane.

Functional Block Diagram

Figure 5 shows the ARC2C0608 functional block diagram.

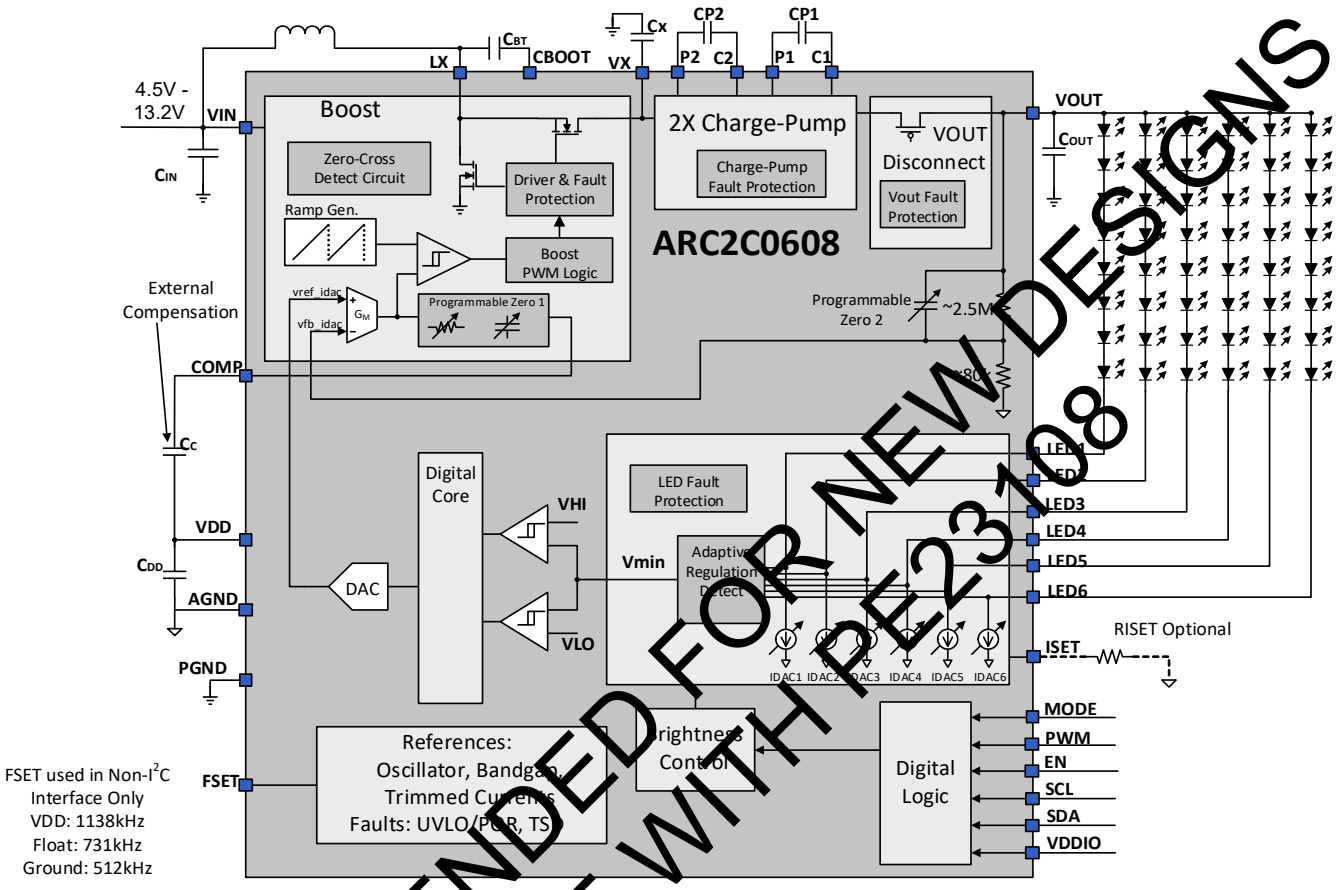

Figure 5. ARC2C0608 Functional Block Diagram

Application Circuit

Figure 6 shows the ARC2C0608 application circuit schematic.

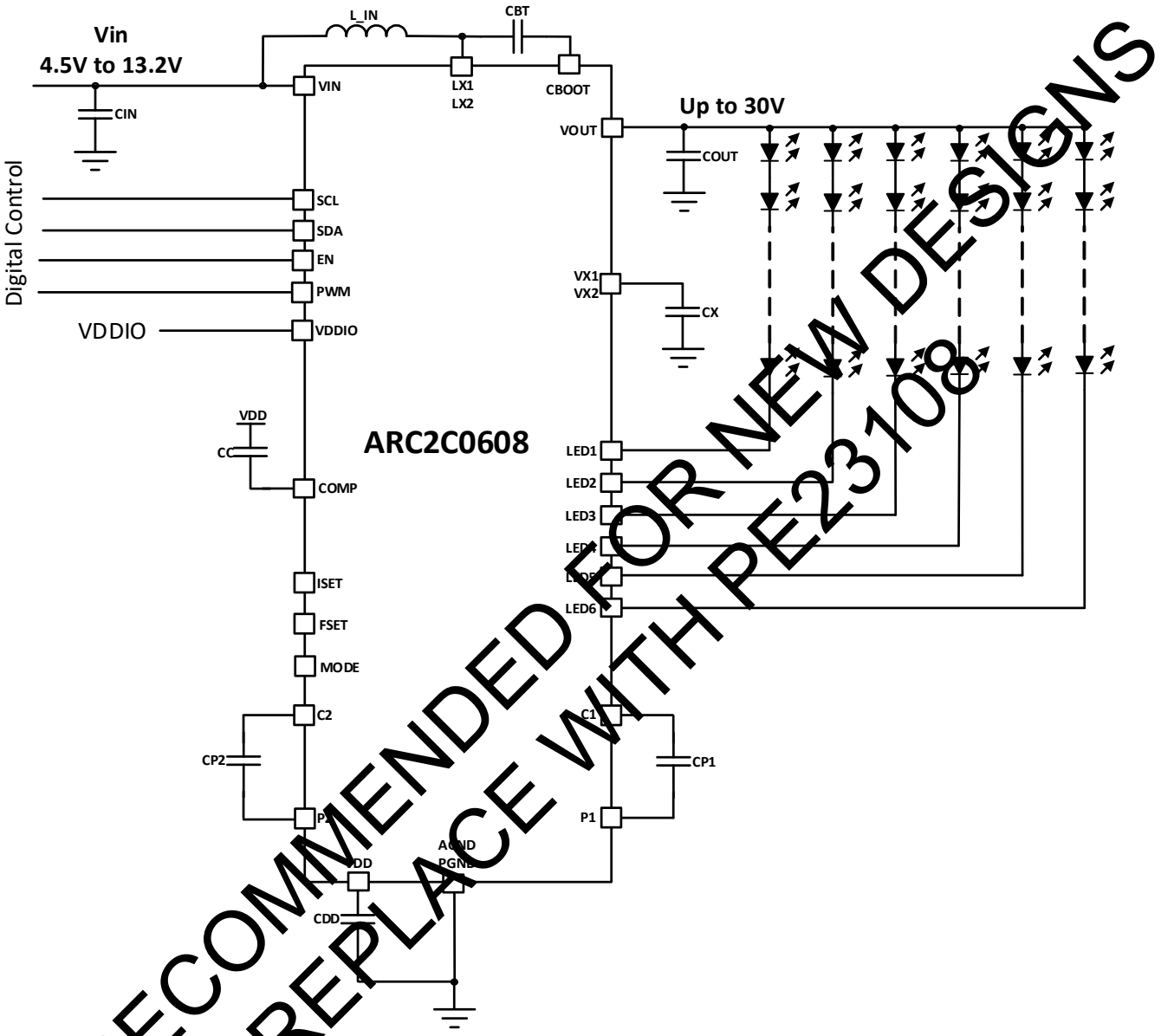

Figure 6. I²C Interface Application Schematic

Typical Performance Data

LED Efficiency

Figure 7–Figure 10 show the ARC2C0608 typical performance data under the following conditions, unless otherwise specified:

- VIN = 7.4V
- L = 15 µH TDK VLF504015-150M
- C_{OUT} = 4.7 µF
- LED V = 2.85V (typ)
- 512 kHz boost frequency

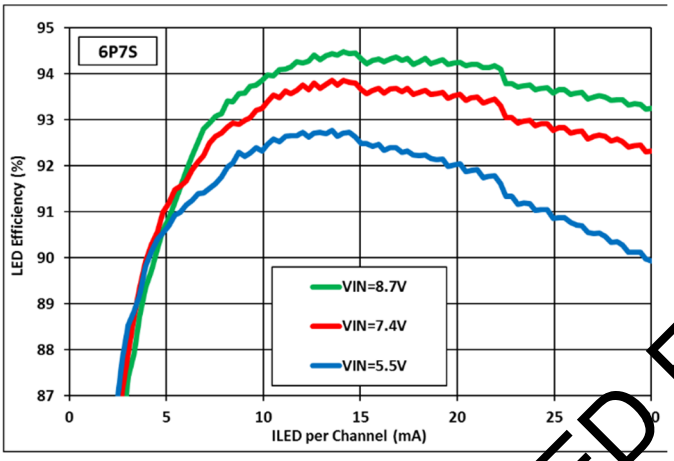

Figure 7. 6p7s LED Efficiency

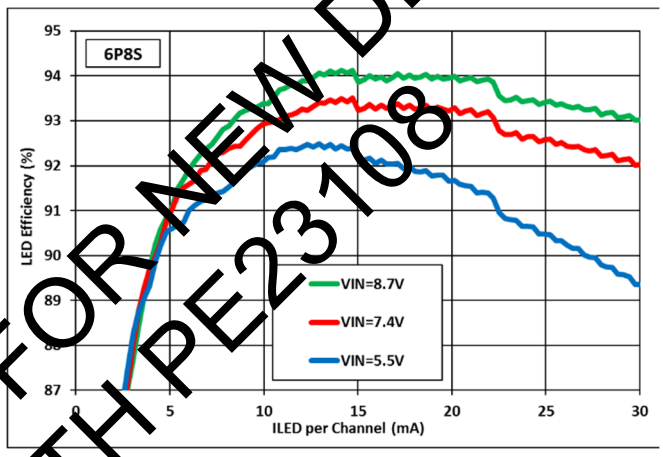

Figure 8. 6p8s LED Efficiency

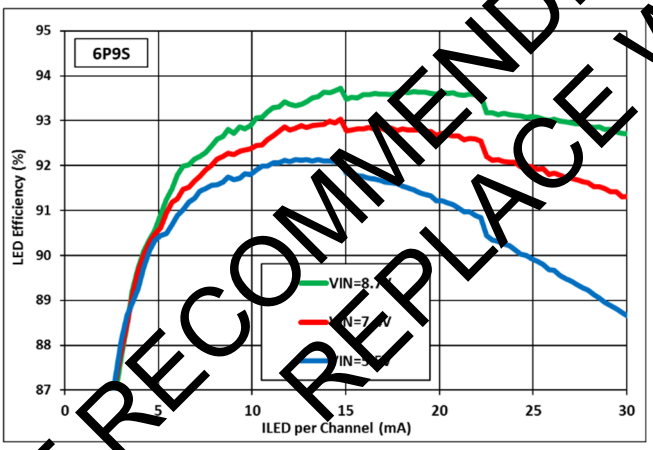

Figure 9. 6p9s LED Efficiency

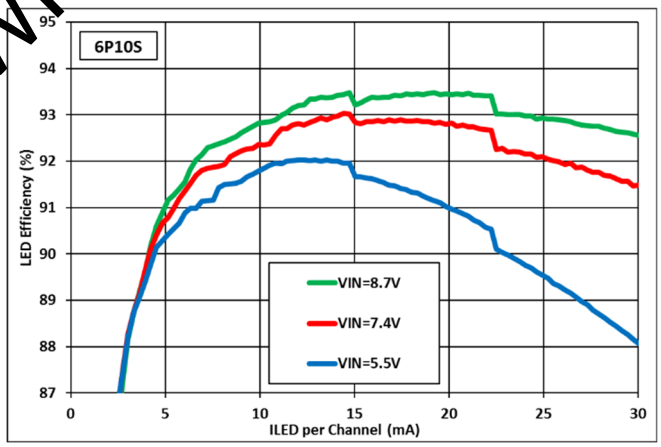

Figure 10. 6p10s LED Efficiency

LED Current Sinks

Figure 11 and Figure 12 show the ARC2C0608 typical performance data under the following conditions, unless otherwise specified:

- VIN = 7.4V
- L = 15 µH TDK VLF504015-150M
- C_{OUT} = 4.7 µF
- LED V = 2.85V (typ)
- 512 kHz boost frequency

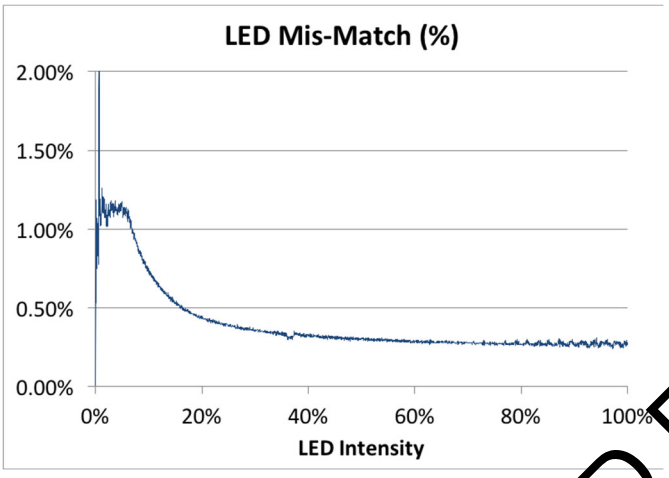

Figure 11. LED Mismatch in Linear Mode

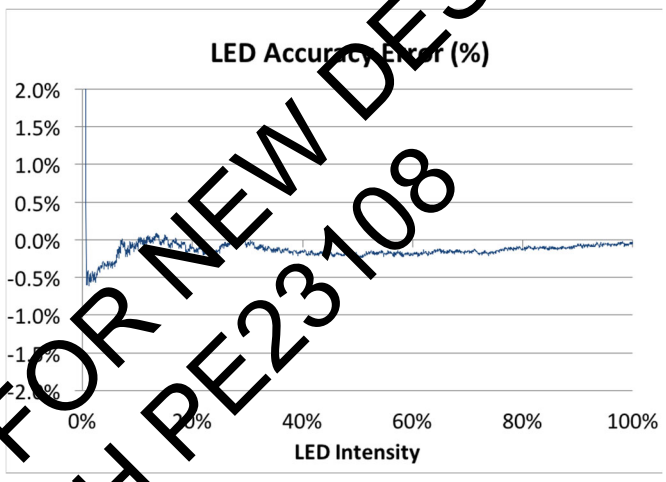

Figure 12. LED Accuracy in Linear Mode

Startup Characteristics

Startup Waveforms in Non-I2C Mode

Figure 13–Figure 15 show the ARC2C0608 startup characteristics under the following conditions, unless otherwise specified:

- VIN = 7.4V
- L = 15 µH TDK VLF504015-150M
- C_{OUT} = 4.7 µF
- LED V = 2.85V (typ)
- 512 kHz boost frequency

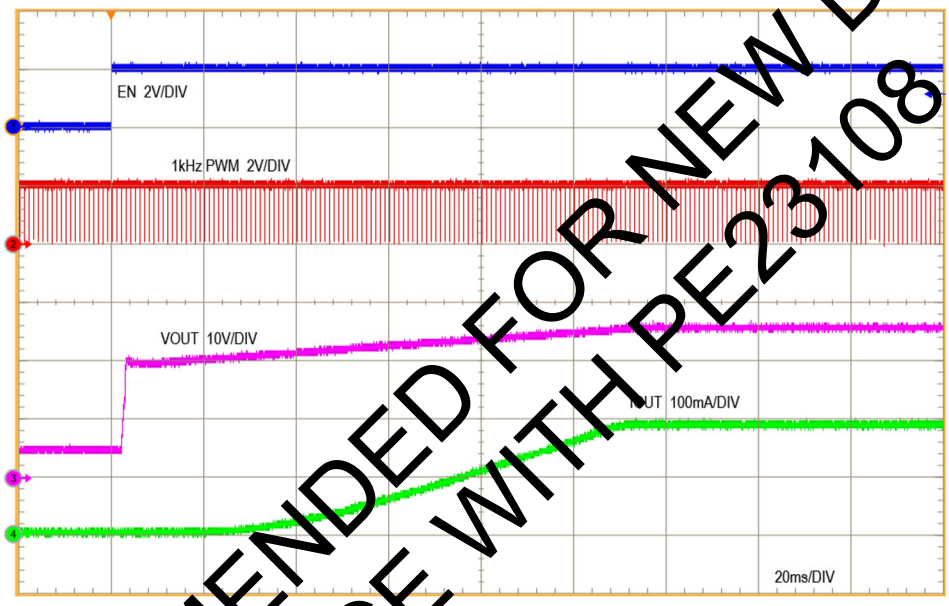

Figure 13. Startup Under 99% PWM Condition, 6p8s Configuration

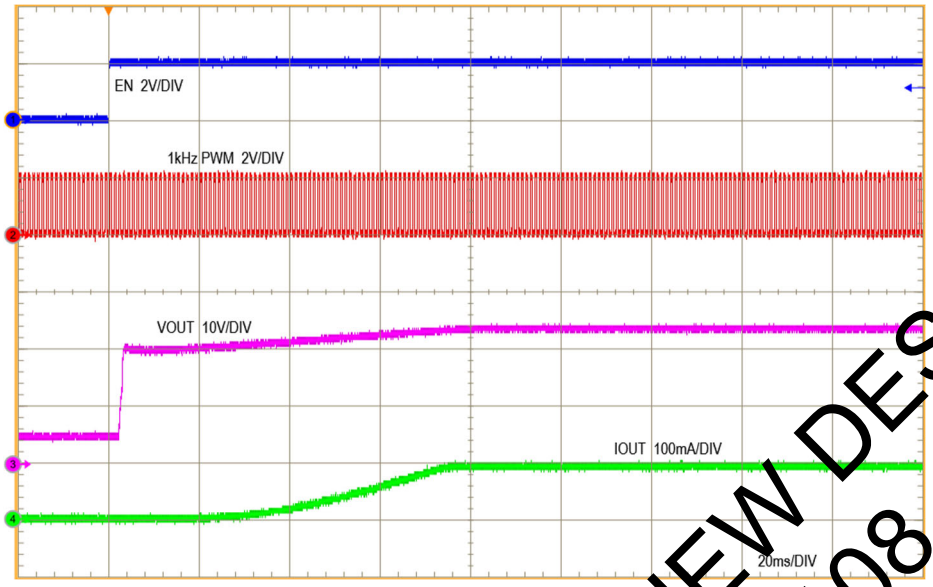

Figure 14. Startup Under 50% PWM Condition, 6p8s Configuration

Figure 15. Startup Under 1% PWM Condition, 6p8s Configuration

Thermal Performance

Figure 16 shows the ARC2C0608 thermal performance under the following conditions:

- 6p9s configuration
- 180 mA
- 7.4V VIN
- 1.5 mm, 15-µH inductor (TDK VLF504015-150M)
- The board temperature is 24.5 °C.
- The ambient temperature (T_A) is 22.3 °C.
- The maximum temperature is 40.5 °C close to the center of the ARC2C0608 die.

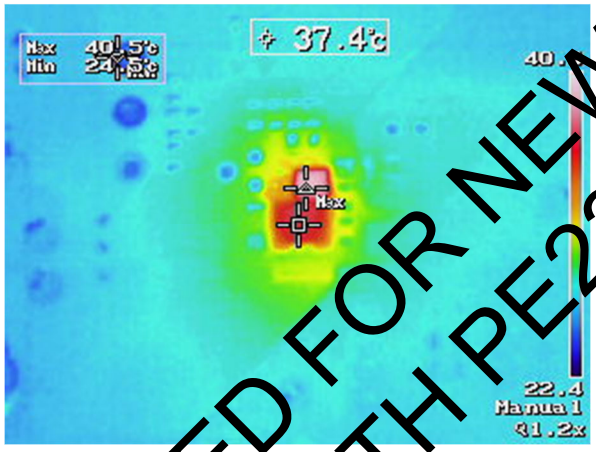

Figure 16. ARC2C0608 Thermal Performance

Detailed Description

The ARC2C0608 uses a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve high peak efficiencies and superior efficiency over the dual-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the LED selection.

The ARC2C0608 supports 1–6 LED strings. Tie unused LEDx pins to ground. This provides maximum design flexibility for a wide variety of LCD screens.

The ARC2C0608 supports I²C and non-I²C operation. It can be configured through I²C interface or external settings and allows combined I²C command settings with the PWM signal to adjust the LED brightness.

The ARC2C0608 provides a full set of protection features to ensure robust system operation that includes the following:

- Input voltage under-voltage lockout (UVLO)
- Thermal shutdown (TSD)
- Boost and charge pump over-current protection (OCP)
- Boost and charge pump output over-voltage and under-voltage protection (OVP and UVP)
- LED open and short detection

Input Sequencing Requirements

VDDIO determines if the device starts up in I²C or non-I²C mode. This input can be applied before or after VIN or EN, but it must be taken high (for I²C mode) or low (for non-I²C mode) before both VIN and EN are asserted. Do not leave VDDIO floating. With VDDIO already established, both VIN and EN must be asserted high before VDD comes up and the ARC2C0608 becomes operational. In I²C mode, the first command can be given 1 ms after both VIN and EN are asserted.

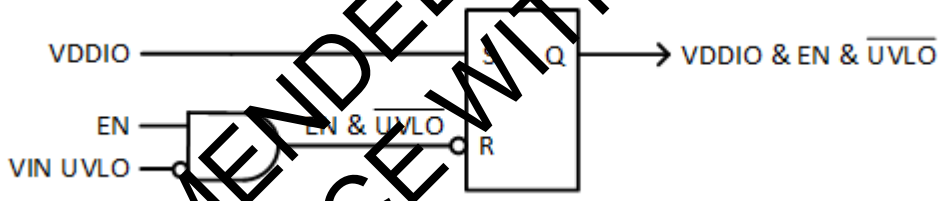

Figure 17. Input Sequencing Logic Diagram

If the part is enabled in non-I²C mode, VDDIO must be connected to the ground plane with a low inductance trace. In I²C mode, VDDIO can vary within its allowable voltage range. If this voltage drops too low, I²C communication stops. However, the device retains all its register values. I²C communication can resume 5 µs after VDDIO becomes stable within its allowable voltage range.

In I²C mode, SCL and SDA serve as the clock and data lines. In non-I²C mode, SCL and SDA can be used to select between the four IMAXTUNE settings, depending on whether the pins are logic low or high.

The sequence for the PWM pin does not matter. It can be switched according to the application requirements while all other signals are being turned on and off. Table 6 lists the various ARC2C0608 input conditions.

Table 6. Input Conditions

VIN	EN	VDDIO	SCL	SDA	PWM	Device Status
Low	–(*)	–	–	–	Switching	Non-operational
High	Low	–	–	–	Switching	Non-operational
High	High	Low	IMAXTUNE setting	IMAXTUNE setting	Switching	Non-I²C operation
High	High	High	Clock	Data	Switching	I²C operation

Note: * A dash (–) in this table denotes that the level can be either high or low and does not affect operation.

Under-voltage Lockout (UVLO)

The ARC2C0608 continuously monitors the VIN input. If the VIN voltage drops below approximately 4.3V, the ARC2C0608 immediately shuts down.

Output Over-voltage and Under-voltage Protection

The ARC2C0608 protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when VOUT rises above the over-voltage threshold V_{OUT_OVP}. When a VOUT OVP occurs, the VOUT_OVP bit of the STATUS1 register is set to 1, and the ARC2C0608 turns off the boost converter. The boost converter automatically restarts after an OVP event when VOUT decreases below the threshold plus 0.5V typical hysteresis.

The over-voltage threshold can be configured through the OVP_TH[1:0] bits in the COMMAND register. The accuracy of each over-voltage threshold is ±5%.

Table 7. Over-voltage Threshold

OVP_TH[1:0]	VOUT Over-voltage Threshold (V)
00	31.4
01	24
10	20

In non-I²C mode, the OVP threshold is fixed at 31.4V.

Select the output over-voltage threshold with enough voltage margin above the highest expected operating VOUT voltage in the application to ensure proper LED open or grounded string fault detection. The highest expected operating VOUT voltage is a function of the number of series LEDs used, the highest LED forward voltage expected, and the regulation voltage at the LED pins during the maximum LED current used in the application per channel.

Reset and Standby Functions

Table 8 lists the RESET and Standby states when the ARC2C0608 uses the I²C interface. For all modes, UVLO high = POR IC (entire chip shutdown).

Table 8. RESET and Standby States in I²C Mode

EN Pin Logic Level	PC_STANDBY Bit	LEDEN[6:1] Bits	Reset Bit	Device Status	Device Circuit Block Status	PC register
0	–*	–	–	OFF	None	Cleared
1	0	0	0	Ready	References ON Boost/CP off LED drivers on standby	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	–	–	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	–	1 (self-clearing)	Reset → Ready (self-clearing)	Ready state after self-clearing reset	Cleared

Note: * A dash (–) in this table denotes that the level can be either high or low and does not affect operation.

The STATUS1 and STATUS2 register bits are all cleared upon read, so the repeated read-back of a logic-high fault bit indicates that the fault event remains persistent. The LED_OPEN and LED_SHORT bits of the STATUS2 register require the faulted string's LEDEN[n] or all enabled LEDEN[n] to be reset low, and then the bits to be read, for them to be cleared.

Boost Output Over-voltage and Under-voltage Protection

The ARC2C0608 monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above a typical over-voltage threshold of 17V. When a VX OVP occurs, the VX_OVP bit of the STATUS1 register is set to 1, and the ARC2C0608 turns off the boost converter. The boost converter automatically restarts after a VX_OV event when VX decreases below the VX_OV threshold.

If the boost output voltage (VX) falls below VIN-1.0V after the LED current sinks have turned on, the ARC2C0608 shuts down the switching converter and the LED current sinks immediately and the VX_UV register bit in the STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and do not start unless the part is shutdown or reset as listed in Table 8.

Soft-Start Timeout

The ARC2C0608 implements a soft-start timeout fault. If the output voltage does not rise above 2x the input voltage within 10 ms, the switching converter and the LED current sinks are disabled. The SS_TIMEOUT bit in the STATUS1 register is set to 1. This is a latched fault. The ARC2C0608 does not start up until a reset event occurs, such as by toggling EN low or setting the RESET bit in the CONFIG4 register (which clears itself).

Charge Pump Flying Capacitor Over-voltage

The ARC2C0608 monitors the flying capacitor voltage relative to the VOUT voltage. When the voltage between the flying capacitor pins C1, C2, and VOUT exceed 18V typical, the switching converter and the LED current sinks are disabled immediately. The CAP_OVP bit of the STATUS1 register is set to 1. The ARC2C0608 does not start up until a reset event occurs, such as by toggling EN low or setting the RESET bit in the COMMAND register (which resets itself).

LED Short Protection

The ARC2C0608 includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator enables when at least one LED pin is in regulation and the shorted LED fault is triggered when an LEDx voltage rises above the shorted LED voltage threshold. The shorted LED voltage threshold can be programmed to 4.35V, 4.85V, 5.25V, and 5.75V by using the CONFIG3 register LED_SHORT_VTH[1:0] bits. This fault condition can occur when some LEDs in a string are electrically bypassed, making that LED string shorter than the other LED strings. The threshold level is referenced to ground.

The reduced forward voltage causes the current sink attached to that string to have a higher voltage than other current sinks, which could cause overheating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED short fault is recorded in the STATUS1 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the LED strings is open, the output rises until it crosses the VOUT_OVP threshold. Any string under regulation at that moment is blocked from controlling VOUT, resulting in the output decreasing to a level needed to regulate the remaining non-open LED strings. An LED open fault is recorded in the STATUS2 register.

If the open LED string is reconnected, the LED current sink re-establishes the current to the level based on the output voltage, but it is not allowed to control the VOUT voltage. To re-enable the output control for any faulted strings, turn off all LEDs or reset the part.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit of 2.3A typically but starts up initially with a derated over-current limit of 1.0A typically for soft-start. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults in which the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds 3.9A, the converter and the LED current sinks are disabled immediately. The BST_ILIM_SEC bit in the STATUS1 register is set and is cleared upon read. The switching converter and LED current sinks remain latched off and do not restart unless the part is shutdown or reset.

A separate short circuit detection is implemented if the current drawn from the VOUT pin exceeds more than 250 mA, the LED current sinks are disabled, and the output is disconnected from the charge pump. The DISC_OCP bit in the STATUS1 register is set. The LED current sinks are enabled again when the VOUT pin fault is removed.

Current Setting

In I²C mode, the maximum current of the LED outputs is set by the MAX_I[1:0] register bits in the ILED_CONFIG register. The default maximum current is 30 mA per LED string with three further settings available: 25 mA, 20 mA, and 15 mA.

Fine tuning of the maximum current of the LED outputs can be set in I²C mode by the IMAXTUNE[5:0] register bits in the ILED_CONFIG register. This allows incremental increases in the maximum output current from the MAX_I[1:0] setting mentioned above, in 6-bit resolution (64 steps) over a range from 0% to 41.5%, and at an average increase of 0.55% per step.

In non-I²C mode, you can use the SDA and SCL pins to select the four trim levels from the IMAXTUNE[5:0] register as listed in Table 9.

Table 9. Four IMAXTUNE[5:0] Trim Levels

SDL	SCL	IMAX Per String Increase	Corresponding IMAXTUNE[5:0] Register Value
0	0	MAX_I + 0%	0x00
0	1	MAX_I + 2.41%	0x05
1	0	MAX_I + 4.96%	0x0A
1	1	MAX_I + 7.64%	0x0F

In addition, the maximum current can be adjusted by an external resistor, R_{ISET}, connected between the ISET pin and ground, when the ISET bit in the LEDEN register is set to 1. R_{ISET} controls the full-scale LED current along with the current determined by the MAX_I register bits as follows:

$$I_{LED\_FULL} = \frac{0.4}{R_{ISET}} * K_{ISET}$$

The R_{ISET} range is 24.9–250 KΩ. In PWM mode, the output current of the LED can be calculated from the duty cycle of the PWM input as follows:

$$I_{LED} = \frac{0.4}{R_{ISET}} * K_{ISET} * PWM\ Duty\ Cycle$$

In non-I²C mode, the above formula applies with K_{ISET} = 1875. This value is factory trimmed. For other options, contact pSemi.

Boost Converter Switching Frequency

In I²C mode, the ARC2C0608 boost converter provides a wide frequency selection to meet your requirements. The FSW_BOOST[4:0] bits in the CONFIG register set the boost switching frequency, as listed in Table 10.

In non-I²C mode, the boost switching frequency is set by the FSET pin, which is sampled once at startup. Changing the FSET pin bias after boost switching has started does not change the boost switching frequency. Table 10 shows the boost switching frequency settings through the I²C register value. Table 11 shows how FSET determines the boost frequency in non-I²C mode.

The choice of inductor, charge pump fly capacitors, and compensation components depends on the selected boost switching frequency for proper part operation. For the recommended component types and values, contact pSemi.

Table 10. FSW_BOOST[4:0] Bits in the CONFIG Register

Division of Master	Frequency (kHz)	FSW_BOOST[4:0] Hex Code	FSW_BOOST[4:0] Binary Code	Non-I²C
3	3413.33	2	00010	–
4	2560.00	3	00011	–
5	2048.00	4	00100	–
6	1706.67	5	00101	–
7	1462.86	6	00110	–
8	1280.00	7	00111	–
9	1137.78	8	01000	Tie to VDD
10	1024.00	9	01001	–
11	930.91	A	01010	–
12	853.33	B	01011	–
13	787.69	C	01100	–
14	731.43	D	01101	Floating
15	682.67	E	01110	–
16	640.00	F	01111	–
17	602.35	10	10000	–
18	568.89	11	10001	–
19	538.95	12	10010	–
20	512.00	13	10011	Tie to GND
21	487.62	14	10100	–
22	465.45	15	10101	–
23	445.22	16	10110	–
24	426.67	17	10111	–
25	409.60	18	11000	–
26	393.85	19	11001	–
27	379.26	1A	11010	–
28	365.71	1B	11011	–
29	353.10	1C	11100	–
30	341.33	1D	11101	–
31	330.32	1E	11110	–
32	320.00	1F	11111	–

Table 11. FSET Pin Bias and Boost Frequency in Non-I2C Mode

FSET Pin Bias	Boost Frequency (kHz)
Shorted to V	1138
Open	731
Shorted to ground	512

Charge Pump Switching Frequency

Table 12 lists the relationship between the LED brightness setting and the charge-pump frequency ratio from the boost switching frequency.

Table 12. LED Current Settings and Charge-Pump Frequency Ratio

LED Current Setting	Charge Pump Frequency Ratio
100% –75%	/2
75% –50%	/4
50% –0%	/8

Switching Converter Compensation

The switching converter operates in hybrid voltage-mode control and uses external compensation. pSemi recommends Type-II compensation, which requires the three external components shown in Figure 18.

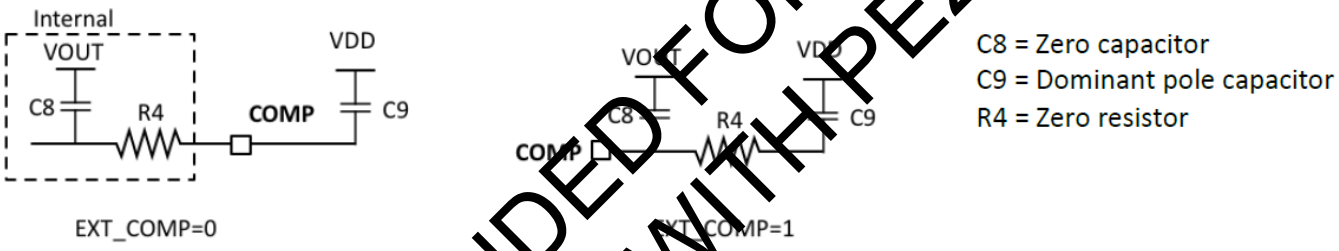

Figure 18. Compensation Components

When the I²C register bit EX_COMP=0, the ARC2C0608 has the C8 and R4 zero components populated internally and only requires dominant pole capacitor C9 to connect to the COMP pin. The SEL_ZERO2[1:0] and SEL_ZERO1[1:0] I²C register bits can internally adjust the values of C8 and R4 over a limited range.

For more compensation control, set the EXT_COMP register bit to 1, which requires all three components to be populated externally.

The default compensation mode when using a non-I²C interface is with internal zero components only (EXT_COMP=0). For compensation recommendations for your application, contact pSemi.

LED Current Output Dimming

The ARC2C0608 supports four LED current output dimming options for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency, and minimal WLED color shift at low brightness levels. These options are Analog, Phase Shift PWM, Hybrid PWM (Mixed-mode), and Direct PWM (DPWM) dimming.

Analog Dimming

In I²C mode, when ILED_CONFIG bit 6, DIM_MODE is set to 0, dimming is set to analog only. In analog dimming, the LED current sink output is always a DC current across the entire brightness range. As brightness is reduced, the LED current sink output DC level decreases, which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the VOUT voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with DC current output also minimizes noise in the system. When using a non-I²C interface, the full-scale output current per channel can be scaled using an external resistor, R_{ISET}, connected between the ISET pin and analog ground. The tolerance of the external resistor R_{ISET} directly affects the accuracy of the LED current sink output, so pSemi recommends using a precision resistor. The recommended R_{ISET} resistor range is 24.9–250 kΩ, with 25 kΩ corresponding to a 30-mA full-scale current output per channel when the register bits MAX_I[1:0]=11.

Phase Shift PWM Dimming

In I²C mode, when ILED_CONFIG register bit 6, DIM_MODE bit is set to 1, dimming is set to mixed dimming. In this mode, the mixed dimming block generates phase-shifted PWM signals to dim active LED strings when the required LED current is below the threshold set by the PWM_IX register bits. The phase difference between active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

Because the input code is a 12-bit value, the PWM generator uses the eight bits of the 0x08 register for the MSB portion mapped as bits WLED_ISET[11:4], and the upper nibble of register 0x07 for the LSB portion mapped as bits WLED_ISET[3:0]. Depending on the PWM frequency selected, the lower bits are truncated. Figure 19 shows how the register bits are used.

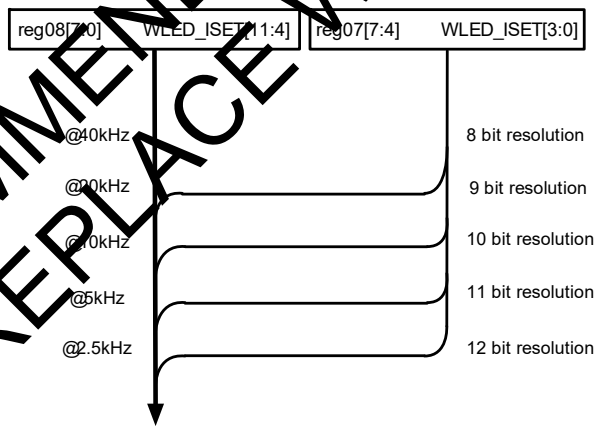

Figure 19. Relationship Between Frequency and Resolution in Phase Shift PWM Dimming

The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

If the PWM frequency is set at 40 kHz, only the WLED_ISET_MSB register at address 0x08 is considered. For a higher resolution and lower frequencies, write first to the upper four bits of the WLD_ISET_LSB register at address 0x07, and then the WLED_ISET_MSB register. The minimum PWM pulse width is typically 200 ns with a resolution of 97.66 ns.

In non-I2C mode, when the MODE pin is floating, the phase-shifted PWM scheme is enabled.

Hybrid PWM (Mixed-mode) Dimming

The ARC2C0608 allows a mixed dimming output scheme for better optical efficiency. The switch point from analog to PWM dimming is set by register bits DIM_MODE=1 and PWM_IX[1:0], and can be 0%, 12.5%, 25%, 50%, or 100% of the brightness range. 0% means that analog dimming is used across the whole brightness range and 100% means that PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted, and below the switch point PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved.

- PWM_IX[1:0]=11 results in a DC output current only when the LED brightness setting is at 100%, otherwise the LED current sink switches off and on to 100% of its full-scale output level.
- PWM_IX[1:0]=10 results in a DC output current only when the LED brightness setting is at 50% or greater, otherwise the LED current sink switches off and on to 50% of its full-scale output level.
- PWM_IX[1:0]=01 results in a DC output current only when the LED brightness setting is at 25% or greater, otherwise the LED current sink switches off and on to 25% of its full-scale output level.
- PWM_IX[1:0]=00 results in a DC output current only when the LED brightness setting is at 12.5% or greater, otherwise the LED current sink switches off and on to 12.5% of its full-scale output level.

Figure 20 shows an example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting.

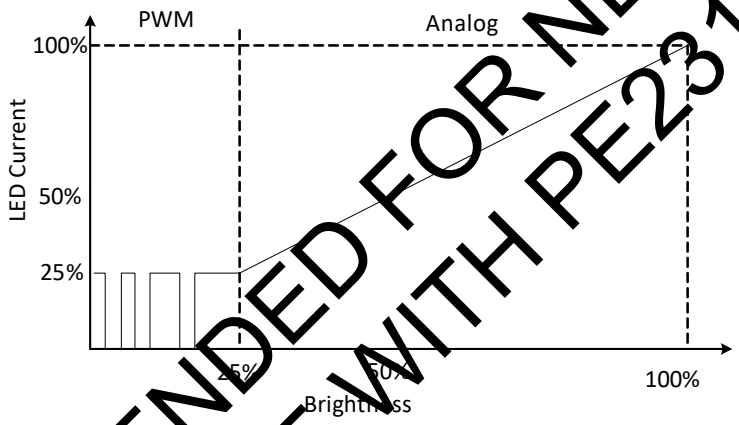

Figure 20. Mixed-Mode Dimming

The choice of four brightness transition points between analog dimming and PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Because the LED current output peak during PWM dimming scales proportionally with the brightness transition point, the LED current pulse width must also scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0] = 01 (25% transition point) is four times longer than at PWM_IX[1:0] = 11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is typically 200 ns.

When using a non-I^{2}C interface, the brightness transition point between analog dimming and PWM dimming is fixed at 25%. For alternative transition point options, contact pSemi.

When the LED current outputs are PWM dimming, their switching frequency can be selected from one of five frequency settings between 2.5–40kHz using the PWM_DIM_FREQ[2:0] register bits. When using a non-I^{2}C interface, the PWM dimming frequency of the LED current outputs is fixed at 2.5 kHz. For alternative frequency options, contact pSemi.

In general, the dimming resolution at the LED current output relates to the PWM dimming frequency and the hybrid transition point, with a higher resolution achieved with a lower PWM dimming frequency and lower transition point. For example, for a 25% transition point, a 12-bit resolution is possible at the 10 kHz PWM_DIM_FREQ[2:0] = 010 setting or lower, an 11-bit resolution is possible at the 20 kHz PWM_DIM_FREQ[2:0] = 011 setting, and so forth.

To help reduce audible noise, the LED current pulses during PWM dimming are always phase-shifted, which reduces the current and voltage ripple on the output capacitor. The equivalent PWM frequency seen by this output capacitor is increased by the number of enabled LED channels. The phase shift between each LED channel is equal to 360° divided by the number of enabled LED channels. This phase shift automatically adjusts as the number of enabled LED channels is changed during operation.

Direct PWM (DPWM) Dimming

The brightness is directly proportional to the duty cycle applied at the PWM pin. The LED current outputs are no longer phase-shifted but are synchronized with the timing edges at the PWM pin.

In I²C mode, when the DIMCODE register bits are set to 11, the direct PWM dimming mode is selected. In non-I²C mode, tying the MODE pin to the VDD pin selects direct PWM dimming.

In direct PWM dimming mode, the input PWM signal switches the LED strings on and off directly, with the LED current on when PWM is high. The mixed dimming block is bypassed, and there is no phase shift among the LED strings. The minimum PWM pulse width allowed under direct PWM dimming is 200ns. The PWM input frequency range is from 200 Hz–20 KHz in this mode.

LED Current Full-Scale or 100% Brightness

The maximum LED Current full-scale can be programmed using either I²C or an external resistor, both of which provide fine tuning. In non-I²C mode, the current set by the ISET resistor can be trimmed upwards by four set levels using the SDA and SCL pins. For more details on these options, see Current Setting on page 24.

LED Brightness Control

The LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET[11:0] bits written using the I²C interface, or both. The register bits DIMCODE[1:0] set up the four dimming schemes described in this section.

DIMCODE = 00

When DIMCODE=00, the LED current is controlled by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate the brightness code. The resulting code goes into the mixed dimming block to generate a DC current level or six phase-shifted PWM signals to control the LED strings.

In non- I²C mode, the LED dimming is controlled by the PWM input only, with the full-scale current set by the resistor on the ISET pin.

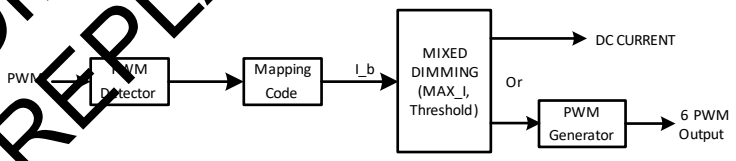

Figure 21. DIMCODE = 00

DIMCODE = 01

When DIMCODE=01, the LED current is controlled by the WLED_ISET[11:0] bits via I²C. The register codes go through a mapping first, then through the mixed dimming block to generate DC current or six phase-shifted PWM signals to control the LED strings.

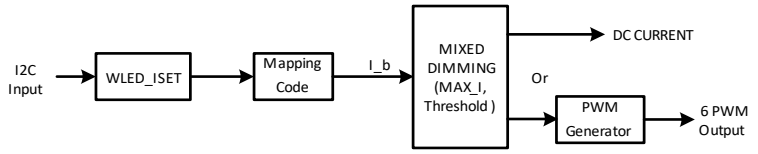

Figure 22. DIMCODE = 01

DIMCODE = 10

When DIMCODE=10, the LED current is controlled by both the PWM input duty cycle and the WLED_ISET[11:0] bits though I²C. The WLED_ISET[11:0] bits go through a mapping and are multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate DC current or six phase-shifted PWM signals to control the LED strings.

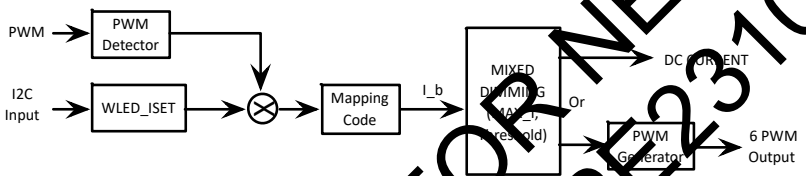

Figure 23. DIMCODE = 10

DIMCODE = 11

When DIMCODE=11, direct PWM dimming is enabled. Under this setting, the input PWM signal turns the active LED strings on and off directly and the internal decoding circuitry and mixed dimming block are bypassed. The minimum input PWM pulse width is limited to 200 ns under direct PWM dimming.

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either through the PWM input or the WLED_ISET[11:0] bits are translated linearly into the time-averaged LED current. This is the default setting.

For better visual experience, the ARC2C0608 can also translate the dimming settings through a logarithmic mapping to produce the LED current. To enable this feature, set the LOG_MODE bit to 1 in the ILED_CONFIG register. There are 1023 possible brightness states in this mode.

Operation with DIMCODE = 00 or 10

In these modes, the ARC2C0608 PWM input frequency range is from 200 Hz–40 KHz. The input frequency is independent of the PWM output frequency, which is the six-phase LED current switching frequency. In I²C mode, the PWM output frequency is set by the PWM_DIM_FREQ register. In non-I²C mode, the PWM output frequency is fixed at 2.5 kHz.

Because the on-chip clock is 10.24 MHz, the full 12-bit dimming resolution can only be implemented with a 2.5 kHz PWM input signal or lower (10.24 MHz/2^{12} = 2.5 kHz). Higher PWM input frequencies have reduced dimming resolution, with eight bits of dimming resolution available at 40 KHz.

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0] = 11). When using 25% PWM dimming, a 40 kHz PWM output frequency provides 10 bits of dimming resolution relative to the full-scale LED output current (10.24 MHz/2^{10}/25% = 40 kHz).

MODE Pin

In non-I²C mode, the MODE pin enables analog dimming, phase-shifted PWM dimming, or direct PWM dimming. This pin is sampled once at startup. Changing its bias after startup does not change the dimming scheme, as listed in Table 13.

Table 13. Mode Pin and Dimming Scheme

Mode Pin	Dimming Scheme
Tied to ground	Analog dimming
Floating	Mixed dimming with a phase-shifted 2.5 kHz internally generated PWM frequency. The transition point is 25%.
Tied to VDD pin	Direct PWM dimming

Fade In/Out Control

The fade in/out control makes a smooth transition from one brightness value to another for a better human eye experience. The ARC2C0608 provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED[7:0] bits in the WLED_FADING_CTRL register. This register can set the speed from a 50 µs/step (0x01) to a 12.75 ms/step (0xFF), or disabled (0x00), based on your preference. For details, see Register WLED_FADING_CTRL on page 11.

In non-I²C mode, FADING_SPEED[7:0] is set to 0x00 to provide full control through the PWM input.

Digital R-C Filter for Non-DPWM Mode Brightness Change

Due to the variability in the rate of consecutive discrete input brightness changes, it is not possible to pick a single fading speed and still produce a visibly smooth output brightness change for all use cases. To resolve this issue, an RC filter is used to filter the output brightness change response to each input brightness change.

The two RCFILTER[1:0] register bits control the coefficient of this RC time constant as shown in Table 14 for a specific case of brightness changes between 1% and 99%. The RC filter coefficient is independent of the PWM_DIM_FREQ[2:0] frequency settings. The RCFILTER[1:0] bits are available in I²C mode through register 0Bh bits[3:2]. This setting can only be changed when the LED strings are off.

Table 14. RC Filter and Time to Reach Steady State Output

RCFILTER[1:0]	Filter/Transition Level	Time to Reach New Steady-State Output Given a Brightness Change Between 1% and 99%
00	Disabled	0s or one PWM_DIM_FREQ[2:0] period(*)
01	Low	~3.7s
10	Medium	~1.7s
11	High	~0.8s

Note: * Depending on how the brightness change command lines up with the internal PWM clock edge.

Input PWM Filter for Non-DPWM Mode

When a duty cycle is applied at the PWM pin to control brightness in non-DPWM mode, the on-time and period are sampled by the internal 10.24 MHz master clock to translate the time-domain information into binary values. As inherent with any sampling of an asynchronous signal, the sampled binary values can jitter by ±1 LSB at steady-state, which translates into jitter on the final brightness result, and this can be visible as flicker. Adding some basic filtering to this sampled system can help to eliminate this flicker at steady state.

The two PWMFILTER[1:0] register bits enable and disable this filter and control the amount of filtering. Furthermore, the filtering is dependent on the direction of the sampled PWM time-step as follows:

- If the PWM time-step has been decreasing, the sampled binary value is allowed to decrement regardless of the delta time-step size but prevented from incrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.
- If the PWM time-step has been increasing, the sampled binary value is allowed to increment regardless of the delta time-step size but prevented from decrementing unless the delta time-step size is greater than or equal to the programmed filter threshold.

Table 15. PWM Filter and Time Step Settings

PWMFILTER[1:0]	Minimum PWM Time-Step Size
00	Disabled
01	2 steps
10	4 steps
11	8 steps

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both the SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through the open drain I/O pins, SDA, and SCL. A master device—such as a microcontroller or a digital signal processor—controls the bus. The master is responsible for generating the SCL signal and managing the device slave addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives or transmits data on the bus under the control of the master device.

The ARC2C0608 operates as a slave and supports the following data transfer modes, as defined in the I²C-Bus specification:

- Standard mode (100 Kbps)
- Fast mode (400 Kbps)
- Fast mode plus (1 Mbps)

The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. The register contents remain intact if the following occur:

- The VIN voltage remains above 4.45V,
- The EN pin remains a logic high, and
- The VDD regulator output voltage remains above 3.0V.

Because the data transfer protocol for standard and fast modes is the same, this document refers to them as F/S-mode. The ARC2C0608 supports 7-bit addressing; 10-bit addressing and general call addressing are not supported. The device 7-bit address is defined as 0110000, and the lower three bits are programmable as described below.

Programming the I²C Slave Address for Multiple Parts on One I²C Bus

To enable multiple ARC2C0608 devices to be addressed on one I²C bus, the lower three bits of the I²C slave address are I²C-accessible registers and allow the I²C slave address for each part to be customized during startup. This is done by enabling each ARC2C0608 in sequence. A special code equal to 6Ch must first be written to register 1Ah before the lower three bits of the I²C slave address can be written to a non-zero code in register 1Bh.

Standard Mode, Fast Mode, and Fast Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 24. All I²C-compatible devices must recognize a start condition.

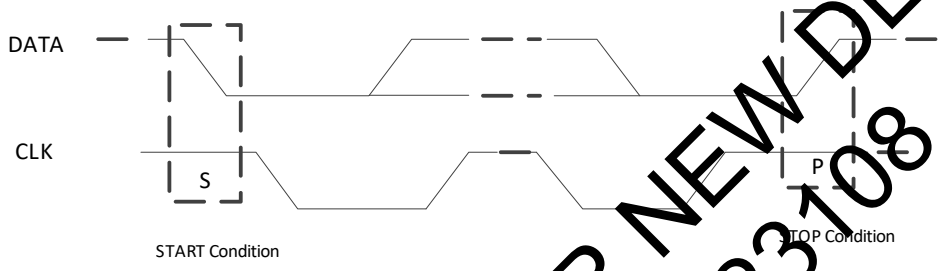

Figure 24. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that the data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 25. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge, as shown in Figure 26, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge signal, the master knows that a communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by transmitter. So, the master or the slave can generate an acknowledge signal, depending on which one is the receiver. The 9-bit valid data sequences consist of eight data bits and one acknowledge bit and can continue as long as needed.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, as shown in Figure 27. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

ARC2C0608 I²C Update Sequence

The ARC2C0608 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the ARC2C0608 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the ARC2C0608. The ARC2C0608 performs an update on the falling edge of the acknowledge signal that follows the LSB.

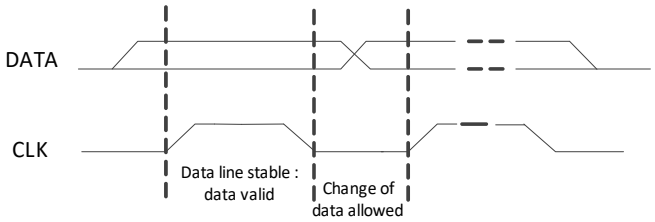

Figure 25. Bit Transfer on the Serial Interface

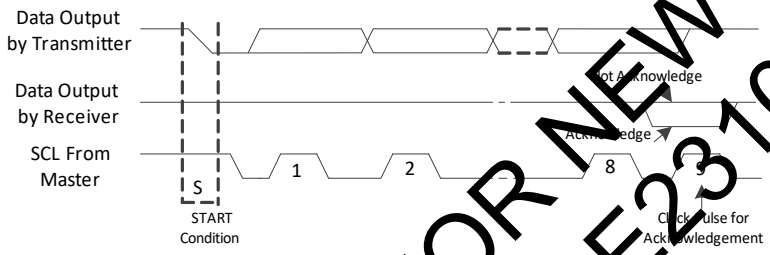

Figure 26. Acknowledge on the I²C Bus

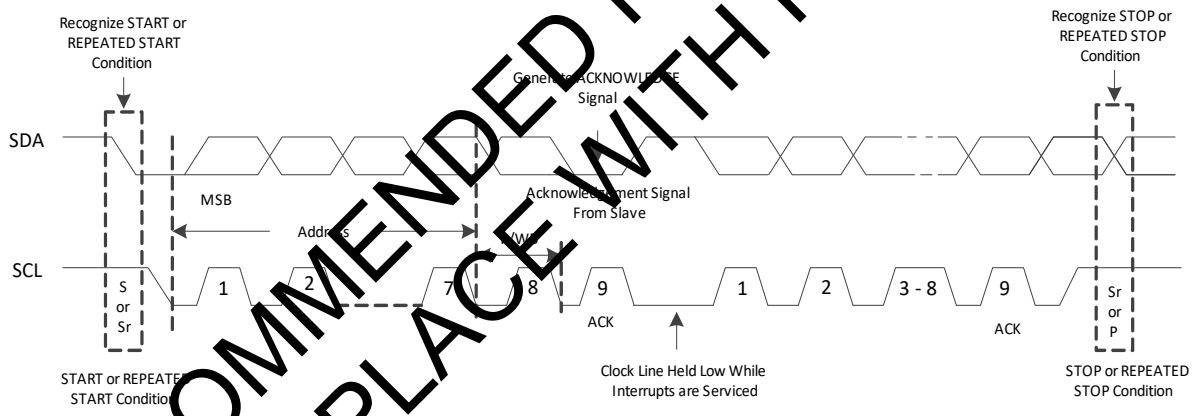

Figure 27. Bus Protocol

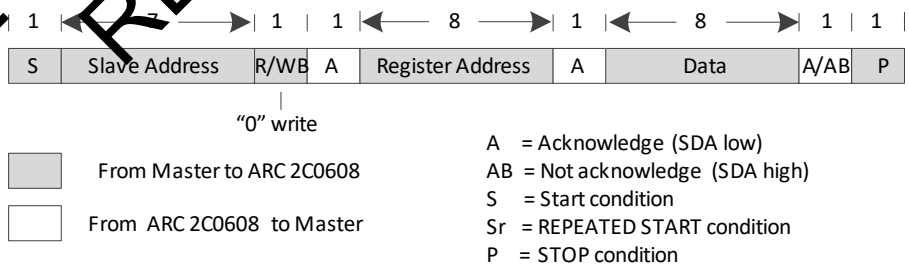

Figure 28. Write Data Transfer Format in Standard, Fast, Fast Plus Modes

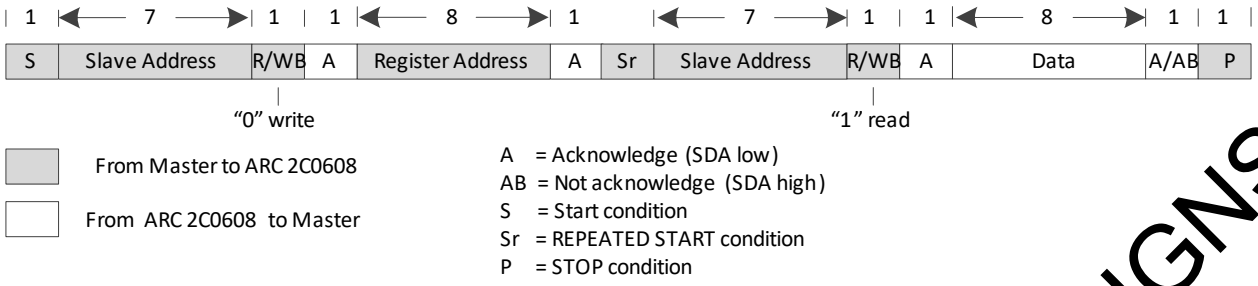

Figure 29. Read Data Transfer Format in Standard, Fast, Fast Plus Modes

Register Map

Slave address: 0110000 (0x30)(*)

Register Configuration Parameters

Register	ADDR	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	I2C_ STANDBY	RESET	Reserved	BOOST_ MODE	OVP_TH[1:0]		Reserved	EXT_COMP
CONFIG	0x01	Reserved[7:5]			FSW_BOOST[4:0]				
STATUS1	0x02	BST_ILIM_ SEC	VOUT_OVP	VX_OV	VX_UV	CAP_OVP	DISC_OCP	TSD	SS_ TIMEOUT
STATUS2	0x03	Reserved[7:2]						LED_OPEN	LED_SHORT
WLED_ FADING_CTRL	0x04	FADING_SPEED[7:0]							
ILED_CONFIG	0x05	LOG_MODE	DIM_MODE	PWM_IX[1:0]		DIM_CODE[1:0]		MAX_I[1:0]	
LEDEN	0x06	ISET_EXT	Reserved	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]
WLED_ISET_ LSB	0x07	WLED_ISET[3:0]				Reserved[3:0]			
WLED_ISET_ MSB	0x08	WLED_ISET[11:4]							
PWM_DIM_ FREQ	0x09	Reserved[7:3]					PWM_DIM_FREQ[2:0]		
CONFIG_ COMP	0x0A	LEDVREGCNTINIT[7:4]				SEL_ZERO2[1:0]		SEL_ZERO1[1:0]	
FILTER_ SETTINGS	0x0B	Reserved[7:4]				RCFILTER [1]	RCFILTER[0]	PWMFILTER [1]	PWMFILTER [0]
IMAXTUNE	0x0C	Reserved[7:6]		IMAXTUNE [5]	IMAXTUNE [4]	IMAXTUNE [3]	IMAXTUNE [2]	IMAXTUNE [1]	IMAXTUNE [0]
I2C_ PASSWORD	0x1A	I2CPASS[7]	I2CPASS[6]	I2CPASS[5]	I2CPASS [4]	I2CPASS [3]	I2CPASS [2]	I2CPASS[1]	I2CPASS[0]
I2C_LOWER_ 3_BITS	0x1B	Reserved[7:3]					I2CADDR [2]	I2CADDR[1]	I2CADDR[0]

Note: * Excluding the read and write bits. The slave address is 01100000 (0x60) if you include the read and write bits.

Detailed Register Descriptions

Register COMMAND

Address	Name	POR Value
0x00	COMMAND	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2C standby	RESET	Reserved	BOOST_MODE	OVP_TH[1:0]		Reserved	EXT_COMP

Bit Description

Field Name	Bits	Type	POR	Description
I2C standby	[7]	R/W	0x0	Standby low-power mode with I²C interface and registers accessible.
RESET	[6]	R/W	0x0	Write 1 to reset the device. This bit is self-clearing.
Reserved	[5]	R/W	0x0	Reserved
BOOST_MODE	[4]	R/W	0x0	Boost converter operating mode: • 0 = Discontinuous conduction mode (DCM) (default) • 1 = Continuous conduction mode (CCM)
OVP_TH[1:0]	[3:2]	R/W	0x0	Output over-voltage protection threshold • 00 = 31.4V (default) • 01 = 24V • 10 = 20V • 11 = Reserved
Reserved	[1]	R/W	0x0	Reserved
EXT_COMP	[0]	R/W	0x0	• 0 = Use partially external compensation network • 1 = Use 100% external compensation network

Register CONFIG

Address	Name	POR Value
0x01	CONFIG1	0x29

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:5]			FSW_BOOST[4:0]				

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:5]	R/W	0x1	Reserved
FSW_BOOST[4:0]	[4:0]	R/W	0x09	Boost switching frequency. For the full frequency chart, see Boost Converter Switching Frequency, on page 25. • 13h = 512 kHz • 09h = 1.024 MHz (default) • 04h = 2.048 MHz • 03h = 2.56 MHz

Register STATUS1

Address	Name	POR Value
0x02	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_OVP	VX_OV	VX_UV	CAP_OVP	DISC_OCP	TSD	SS_TIMEOUT

Bit Description

Field Name	Bits	Type	POR	Description
BST_ILIM_SEC	[7]	R	0b	Status bit to flag a secondary boost current limit condition: • 0 = No secondary current limit • 1 = Boost current exceeds secondary current limit
VOUT_OVP	[6]	R	0b	Status bit to flag an output over-voltage condition: • 0 = No OVP condition • 1 = Output voltage is above OVP threshold
VX_OV	[5]	R	0b	Status bit to flag a VX node over-voltage condition: • 0 = No VX over-voltage condition • 1 = VX voltage is above OVP threshold
VX_UV	[4]	R	0b	Status bit to flag a VX node under-voltage condition: • 0 = No VX under-voltage condition • 1 = VX voltage is below UVP threshold
CAP_OVP	[3]	R	0b	Status bit to flag a charge pump capacitor over-voltage condition: • 0 = No charge pump capacitor over-voltage • 1 = Charge pump capacitor voltage is above OVP threshold
DISC_OCP	[2]	R	0b	Status bit to flag a disconnect switch over-current condition: • 0 = No disconnect switch over-current • 1 = Current through the disconnect switch is above over-current threshold
TSD	[1]	R	0b	Status bit to flag a thermal shutdown condition: • 0 = No thermal shutdown condition • 1 = part exceeds the thermal shutdown threshold
SS_TIMEOUT	[0]	R	0b	Status bit to flag a soft start timeout condition: • 0 = No soft start timeout condition • 1 = Soft start incomplete within the pre-defined time

Register STATUS2

Address	Name	POR Value
0x03	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:2]						LED_OPEN	LED_SHORT

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:2]	R	0b	Reserved
LED_OPEN	[1]	R	0x0	An LED OPEN condition was detected on one or more strings. Status bit to flag an LED OPEN condition: • 0 = No LED open • 1 = LED open condition detected on one or more strings. After it is set, this bit stays set until the STATUS2 register is read and the individual LEDEN[n] bit corresponding to the open string is reset low.
LED_SHORT	[0]	R	0x0	An LED SHORT condition was detected on one or more strings* Status bit to flag an LED SHORT condition: • 0 = No LED short • 1 = LED short condition detected on one or more strings. After it is set, this bit stays set until the STATUS2 register is read and all LEDEN[6:1] bits are reset low.

Register WLED_FADING_CTRL

Address	Name	POR Value
0x04	WLED_FADING_CTRL	0x00

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED[7:0]							

Bit Description

Field Name	Bits	Type	POR	Description
FADING_SPEED	[7:0]	R/W	0x00	Sets the fading counter from 50 µs to 12.75 ms in 50 µs steps. This is the period between each intensity step. • 0x00 = Fading disabled 0x01 = 50 µs/step … 0xFF = 12.75 ms/step

Register ILED_CONFIG

Address	Name	POR Value
0x05	ILED_CONFIG	0x53

Bit Assignment

7	6	5	4	3	2	1	0
LOG_MODE	DIM_MODE	PWM_IX[1:0]		DIMCODE[1:0]		MAX_I[1:0]	

Bit Description

Field Name	Bits	Type	POR	Description
LOG_MODE	[7]	R/W	0b	LED brightness control profile: • 0 = linear (default) • 1 = logarithmic
DIM_MODE	[6]	R/W	1b	LED current output dimming mode: • 0 = Analog dimming only • 1 = Hybrid PWM dimming mode (default)
PWM_IX[1:0]	[5:4]	R/W	01b	Hybrid PWM dimming transition point between PWM dimming and analog dimming: • 00 = 12.5% of full-scale current • 01 = 25% of full-scale current (default) • 10 = 50% of full-scale current • 11 = 100% of full-scale current or PWM dimming only
DIMCODE[1:0]	[3:2]	R/W	00b	LED brightness control: • 00 = PWM input duty cycle dimming (default) • 01 = WLED_ISET[11:0] • 10 = Both PWM duty cycle and WLED_ISET[11:0] • 11 = Direct PWM dimming
MAX_I[1:0]	[1:0]	R/W	11b	WLED full scale current (100% brightness): • 00 = 15 mA • 01 = 20 mA • 10 = 25 mA • 11 = 30 mA (default)

Register LEDEN

Address	Name	POR Value
0x06	LEDEN	0x00

Bit Assignment

7	6	5	4	3	2	1	0
ISET_EXT	Reserved	LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]

Bit Description

Field Name	Bits	Type	POR	Description
ISET_EXT	[7]	R/W	0b	LED full-scale current setting pin: • 0 = MAX_I bits in the LED_CONFIG register set the full-scale LED current • 1 = External resistor R_{ISET} and current multiplier KISET program the full-scale LED current
Reserved	[6]	R/W	0b	Reserved
LEDEN[6]–LEDEN[1]	[5:0]	R/W	0x0	LED string enables: • 0 = String is disabled • 1 = String is enabled

Register WLED_ISET_LSB

Address	Name	POR Value
0x07	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				Reserved[3:0]			

Bit Description

Field Name	Bits	Type	POR	Description
WLED_ISET[3:0]	[7:4]	R/W	0x00	LED output current setting bits [3:0]. For details, see Current Setting on page 24. If you change the LSBs, write these before you write the MSBs. Changes to these bits are only implemented when the next register is written, which are typically the MSBs, but could be any register.
Reserved	[3:0]	R	0x00	Reserved

Register WLED_ISET_MSB

Address	Name	POR Value
0x08	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[11:4]							

Bit Description

Field Name	Bits	Type	POR	Description
WLED_ISET[11:4]	[7:0]	R/W	0x00	The MSB bits of the WLED_ISET[11:0] brightness code. For details, see LED Brightness Control on page 29.

Register PWM_DIM_FREQ

Address	Name	POR Value
0x09	PWM_DIM_FREQ	0x01

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:3]					PWM_DIM_FREQ[2:0]		

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:3]	R/W	0x00	Reserved
PWM_DIM_FREQ	[2:0]	R/W	001b	PWM_DIM_FREQ in kHz: • 000 = 2.5 • 001 = 5 (default) • 010 = 10 • 011 = 20 • 100 = 40 • 101, …, 111= Reserved

Register CONFIG_COMP

Address	Name	POR Value
0x0A	CONFIG_COMP	0x70

Bit Assignment

7	6	5	4	3	2	1	0
LEDVREGCNTINIT[7:4]				SEL_ZERO2[1:0]		SEL_ZERO1[1:0]	

Bit Description

Field Name	Bits	Type	POR	Description
LEDVREGCNTINIT[7:4]	[7:4]	R/W	0x07	Initial count for setting VOUT target voltage at startup: • 0x00 = 8.9V • … • 0x07 = 19.1V • … • 0x0F = 30.8V
SEL_ZERO2[1:0]*	[3:2]	R/W	00b	Selects internal feed forward zero frequency: • 00 = 11.6 kHz • 01 = 8.4 kHz • 10 = 7.1 kHz • 11 = 6.1 kHz
SEL_ZERO1[1:0]*	[1:0]	R/W	00b	Selects internal zero resistance: • 00 = 0Ω • 01 = 4.2 kΩ • 10 = 8.4 kΩ • 11 = 16.8 kΩ
Note: * The SEL_ZERO2[1:0] and SEL_ZERO1[1:0] bits are active only when the EXT_COMP bit from register 00h is 0. When EXT_COMP = 1, the SEL_ZERO2[1:0] and SEL_ZERO1[1:0] bits are ignored.				

Register FILTER_SETTINGS

Address	Name	POR Value
0x0B	FILTER_SETTINGS	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:4]				RCFILTER[1]	RCFILTER[0]	PWMFILTER[1]	PWMFILTER[0]

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:4]	R	0x00	Reserved
RCFILTER[1:0]	[3:2]	R/W	00b	Status 00 = RC filter OFF (default) 01 = LOW 10 = MEDIUM 11 = HIGH
PWMFILTER[1:0]	[1:0]	R/W	00b	Status 00 = OFF (default) 01 = 2 STEPS 10 = 4 STEPS 11 = 8 STEPS

Register IMAXTUNE

Address	Name	POR Value
0x0C	IMAXTUNE	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:6]		IMAXTUNE[5]	IMAXTUNE[4]	IMAXTUNE[3]	IMAXTUNE[2]	IMAXTUNE[1]	IMAXTUNE[0]

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:6]	R	0x00	Reserved
IMAXTUNE[5:0]	[5:0]	R/W	00b	Sets the percentage increase of the maximum LED current MAX_I[0:1] (non-linear but monotonic increase vs. code): • 0x00 = 0% increase • …. • 0x20 = 20.2% increase • …. • 0x3F = 41.5% increase

Register I2C_PASSWORD

Address	Name	POR Value
0x1A	I2C_PASSWORD	0x00

Bit Assignment

7	6	5	4	3	2	1	0
I2CPASS[7]	I2CPASS[6]	I2CPASS[5]	I2CPASS[4]	I2CPASS[3]	I2CPASS[2]	I2CPASS[1]	I2CPASS[0]

Bit Description

Field Name	Bits	Type	POR	Description
I2CPASS[7:0]	[7:0]	R/W	00b	I^2C password setting for lower three bits = 0x6C

Register I2C_LOWER_3_BITS

Address	Name	POR Value
0x1B	I2C_LOWER_3_BITS	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved[7:3]					I2CADDR[3]	I2CADDR[2]	I2CADDR[1]

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:3]	R	0x00	Reserved
I2CADDR[3:1]	[2:0]	R/W	00b	These lower three bits enable the assignment of unique I^2C addresses in multi-part applications.

Application Schematic

Figure 30 shows the ARC2C0608 detailed application schematic.

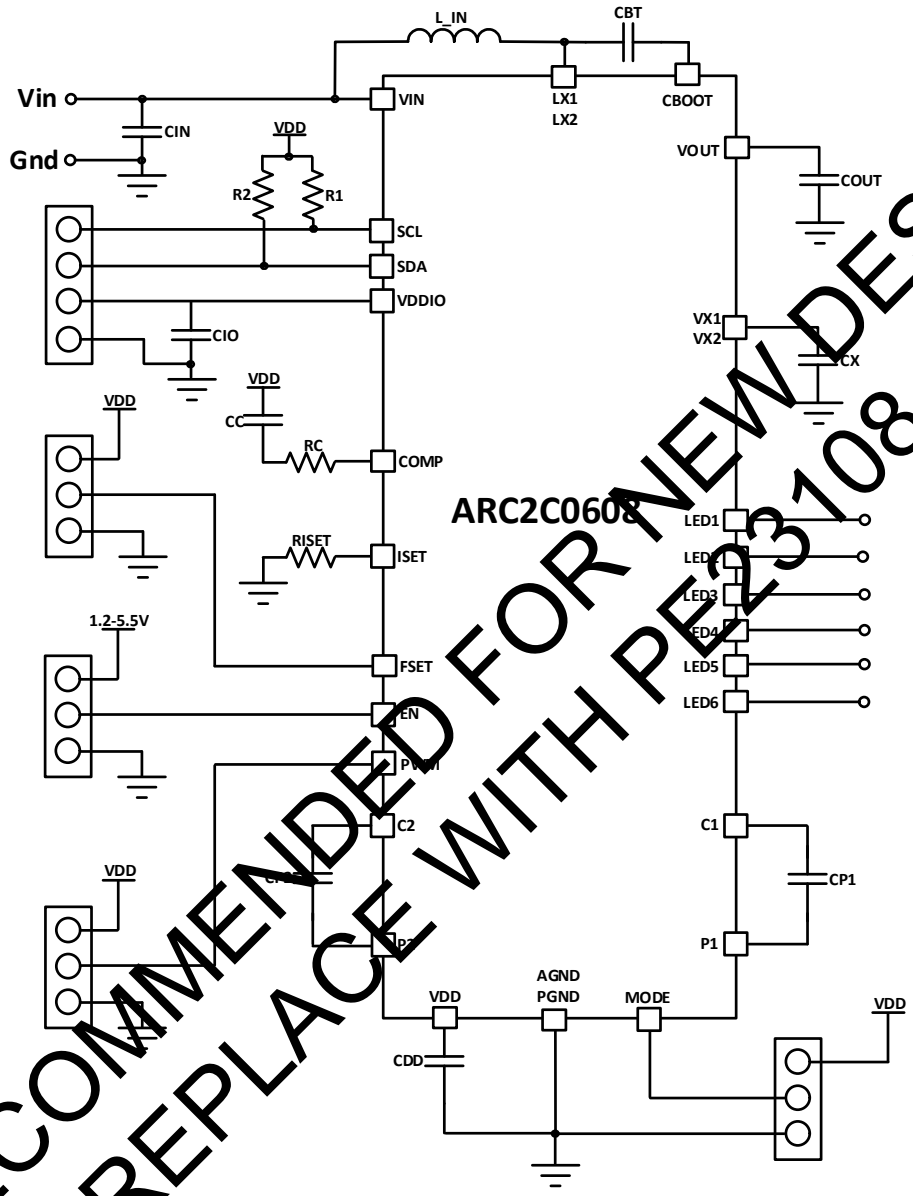

Figure 30. ARC2C0608 Detailed Application Schematic

Application Circuit Part List

Table 16 lists the recommended part numbers for the components shown in Figure 30.

Table 16. Recommended Parts

Component	Value	Part Size	Mfg. Part Number
CBT	22 nF 50V X7R	C0402	GRM155R71H223KA12D
CX	470 nF 25V X5R	C0402	GRM155R61E474KE01
CP1, CP2	2.2 µF 25V X7R	C0805	GRM21BR71E225KA73
CIN(*)	1.0 µF 16V X5R	C0603	GRM188R61C105KA12D
CC	5.6 nF X5R	C0201	GRM033R61E562KA12D
COUT	4.7 µF 35V X7S	C0805	GRM21BC7YA475KE11
CDD	1 µF 10V X5R	C0402	GRM155R61A105KE15D
CIO	1 µF 10V X5R	C0402	GRM155R61A105KE15D
L_IN	6.8 µH	3.2 × 2.5 × 1.2 mm	DFE322512F-6R8M
RISET	24.9 kΩ	R0402	Use tighter than 1% tolerance
RC	0 Ω	R0201	Generic
R1, R2	1 kΩ	R0201	Generic
U1	High-efficiency LED backlight driver	35-lead WLCSP	ARC2C0608

Note: * This value might require an adjustment based on the proximity of the input source to eliminate input voltage ringing.

Component Selection

pSemi recommends that ARC2C0608 customers adhere closely to the recommended parts list in Table 16. Component selection is a complex process and several important design parameters are not typically specified for passive components. If you want to deviate from these recommended components, contact pSemi for guidance.

Layout Example

Figure 31–Figure 35 show an example compact six WLED string converter layout. The solution size is ~56 mm^2.

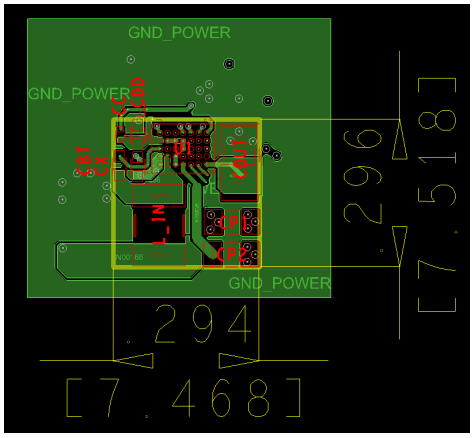

Figure 31. Layout Example

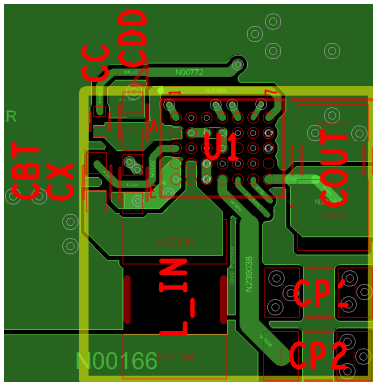

Figure 32. Top Layer

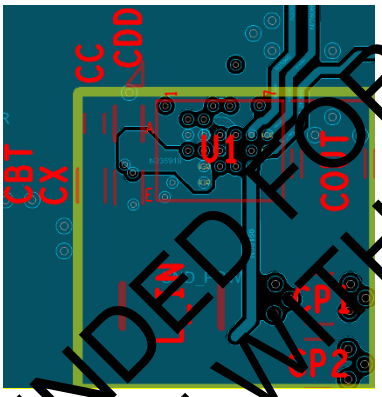

Figure 33. Layer 2

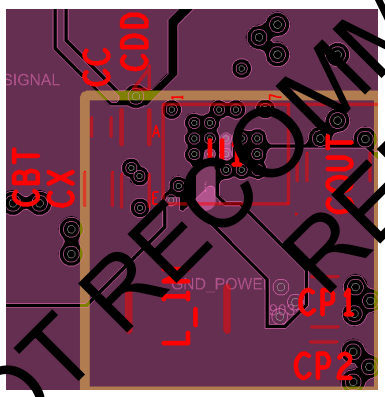

Figure 34. Layer 3

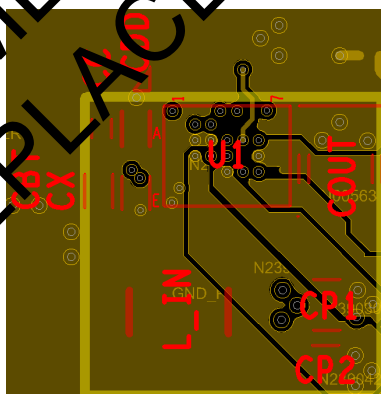

Figure 35. Bottom Layer

Packaging Information

This section includes the following packaging data:

- Package drawings
- PCB land design guidelines
- Tape-and-reel specification

Package Drawings

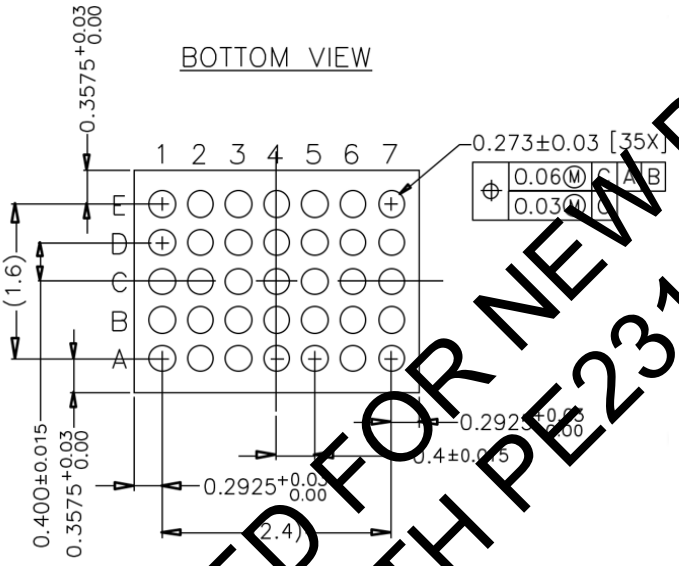

Figure 36. Bottom View and Dimensions

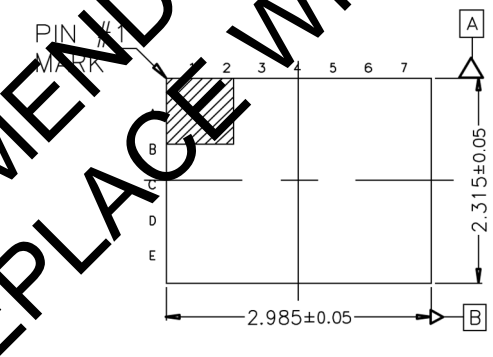

Figure 37. Top View and Dimensions

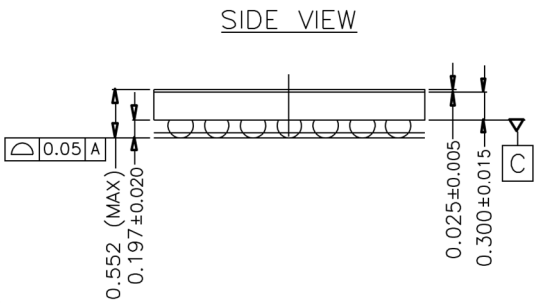

Figure 38. Side View and Dimensions

PCB Land Design Guidelines

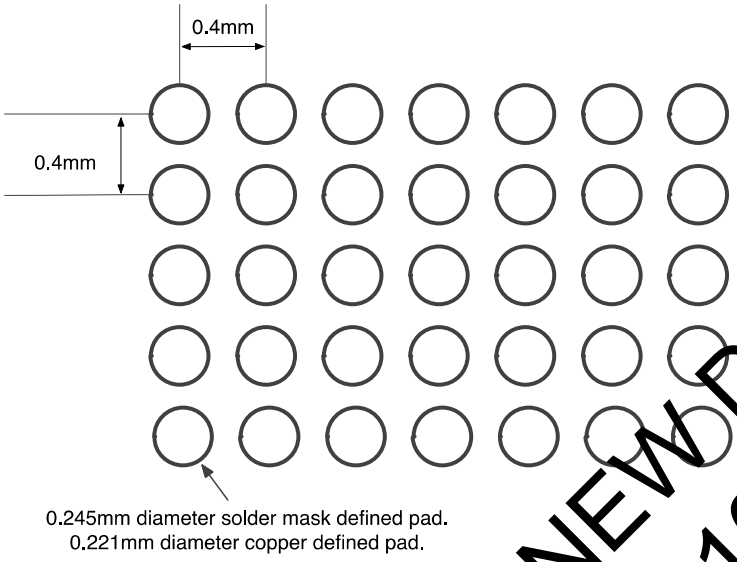

Figure 39. ARC2C0608 Bottom View and Pad Dimensions

Tape and Reel Specification

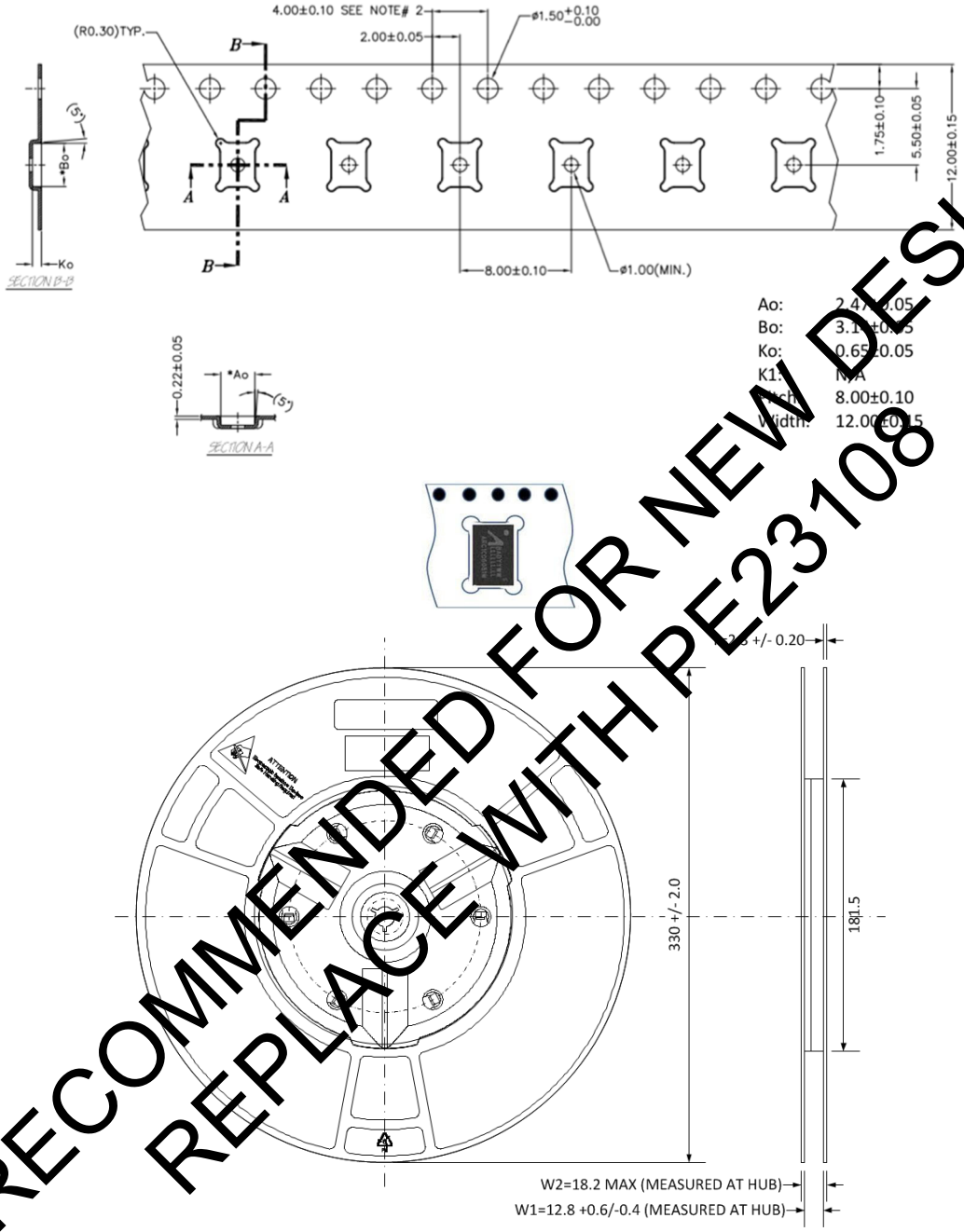

Figure 40. 2.985 mm × 2.315 mm WLCSP Tape and Reel Specification

Ordering Information

Table 17. ARC2C0608 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
ARC2C06081W-R	High-efficiency LED Backlight Driver	2.985 mm × 2.315 mm WLCSP on tape and reel	5000 units/large tape and reel
ARC2C06081W-V		2.985 mm × 2.315 mm WLCSP on tape and reel	250 units/small tape and reel
ARC2C06081W-G		2.985 mm × 2.315 mm WLCSP	10 units/sample waffle tray

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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