Product Specification

PE613010

UltraCMOS® SPST Tuning Control Switch, 100–3000 MHz

Features

- Open reflective architecture
- Very low on-resistance of 1.2Ω
- Low insertion loss
  - 0.20 dB @ 900 MHz
  - 0.40 dB @ 1900 MHz
- High power handling: 38 dBm (50Ω)
- Wide power supply range (2.3V to 4.8V)
- High ESD tolerance of 2 kV HBM on all pins
- Applications include:
  - Open and closed-loop tunable antennas for 2G/3G/4G
  - Tunable matching networks
  - Tunable filter networks
  - Bypassing applications
  - RFID readers

Product Description

The PE613010 is an SPST tuning control switch based on Peregrine's UltraCMOS® technology. This highly versatile switch supports a wide variety of tuning circuit topologies with emphasis on impedance matching and aperture tuning applications. PE613010 features low on-resistance and insertion loss from 100 to 3000 MHz.

PE613010 offers high RF power handling and ruggedness, while meeting challenging harmonic and linearity requirements enabled by Peregrine's HaRP™ technology. With single-pin low voltage CMOS control, all decoding and biasing is integrated on-chip and no external bypassing or filtering components are required.

UltraCMOS tuning devices feature ease of use while delivering superior RF performance. With built-in bias voltage generation and ESD protection, tuning control switches provide a monolithically integrated tuning solution for demanding RF applications.

Figure 1. Functional Block Diagram

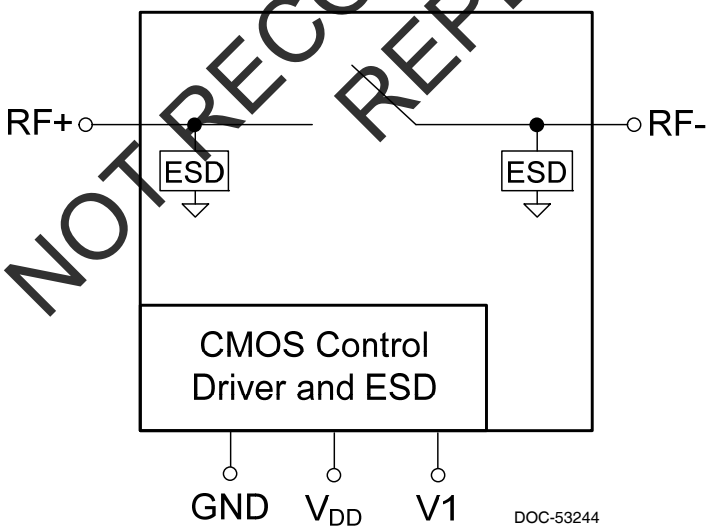


Figure 2. Package Type

10-lead 2 × 2 × 0.55 mm QFN

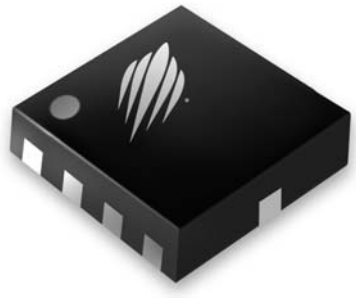


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.75V

Parameter	Condition	Min	Typ	Max	Unit
Operational Frequency		100		3000	MHz
R_{ON}	RF+ to RF–, SW_{ON}, DC measurement		1.20		Ω
C_{OFF}	RF+ to RF–, SW_{OFF}		0.40		pF
Insertion Loss[1]	100 to 960 MHz, (RF+ to RF–), SW_{ON}		0.20	0.30	dB
	960 to 1710 MHz, (RF+ to RF–), SW_{ON}		0.30	0.40	dB
	1710 to 2170 MHz, (RF+ to RF–), SW_{ON}		0.40	0.50	dB
	2170 to 2700 MHz, (RF+ to RF–), SW_{ON}		0.60	0.70	dB
	2700 to 3000 MHz, (RF+ to RF–), SW_{ON}		0.80	0.95	dB
Isolation[2]	100 to 960 MHz, (RF+ to RF–), SW_{OFF}	10	11		dB
	960 to 1710 MHz, (RF+ to RF–), SW_{OFF}	6	7		dB
	1710 to 2170 MHz, (RF+ to RF–), SW_{OFF}	4	5		dB
	2170 to 2700 MHz, (RF+ to RF–), SW_{OFF}	3	4		dB
	2700 to 3000 MHz, (RF+ to RF–), SW_{OFF}	3	4		dB
Harmonics[3,4]	2fo, 3fo: 698 to 915 MHz, P_{IN} +35 dBm (SW_{ON}), P_{IN} +31 dBm (SW_{OFF})		–60	–36	dBm
	2fo, 3fo: 1710 to 1910 MHz, P_{IN} +33 dBm, (SW_{ON}), P_{IN} +29 dBm (SW_{OFF})		–50	–36	dBm
Input IP3	100 to 3000 MHz		70		dBm
IMD3	Bands I,II,V,VIII, +20 dBm CW @ TX freq, –15 dBm CW @ 2TX–RX freq, 50Ω, SW_{ON}		–115	–105	dBm
Switching Time	50% VCTRL to 90% RF ON or 10% RF OFF		7	12	µs

Notes: 1. Assumes optimal matching with 1.5 nH inductor in series with each RF port.
2. Open reflective architecture for flexible configuration of switch in tuning application.
3. Pulsed RF input with 4620 µs period, 50% duty cycle, measured per 3GPP TS 45.005.
4. Power handling in the OFF state reduced due to highly reflective load condition.

Figure 3. Pin Configuration (Top View)

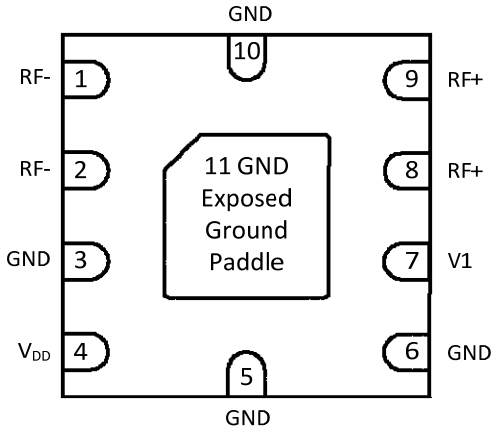


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RF–	Negative RF Port[1]
2	RF–	Negative RF Port[1]
3	GND	Ground[2]
4	V_{DD}	Power Supply Pin
5	GND	Ground[2]
6	GND	Ground[2]
7	V1	Switch control input, CMOS logic level
8	RF+	Positive RF Port[1]
9	RF+	Positive RF Port[1]
10	GND	Ground[2]
11	GND	Exposed Ground Paddle[2]

Notes: 1. Multiple RF pins are provided for flexibility. They can be tied together for optimal RF performance, or used individually (leave unused pin floating).
2. For optimal performance, recommend tying Pins 3, 5, 6, 10, 11 together on PCB.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE613010 in the 10-lead 2 × 2 × 0.55 mm QFN package is MSL1.

Table 3. Truth Table

State	V1
Switch OFF	0
Switch ON	1

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Supply Voltage	2.30	2.75	5.50	V
I_{DD} Power Supply Current (V_{DD} = 2.75V, 25°C)		140	200	µA
V_{IH} Control Voltage High	1.2	1.8	3.1	V
V_{IL} Control Voltage Low	0	0	0.57	V
Peak Operating RF Voltage[1,2] 100 MHz–3 GHz			25[3]	Vpk
T_{OP} Operating Temperature Range	–40	+25	+85	°C

Notes: 1. Between all RF ports, and from RF ports to GND.
2. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
3. RF input power of 38 dBm (50Ω, SW_{ON}) and 32 dBm (50Ω, SW_{OFF}).

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V_{DD}	Supply Voltage	–0.3	5.5	V
V_{CTRL}	Digital Input Voltage (V1)	–0.3	3.6	V
T_{ST}	Storage Temperature Range	–65	+150	°C
$V_{ESD,HBM}$	HBM ESD Voltage, All Pins*		2000	V

Note: * Human Body Model (MIL_STD 883 Method 3015.7).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Equivalent Circuit Model Description

The Equivalent Circuit Model includes all parasitic elements and is accurate in switch on and switch off states, reflecting physical circuit behavior accurately and providing very close correlation to measured data. It can easily be used in circuit simulation programs.

C_S represents switch core capacitance between RF+ and RF– ports in the SW_{OFF} state. The parameter R_S represents the Equivalent Series Resistance (ESR) of the switch core.

Parasitic inductance due to circuit and package is modeled as L_S. C_P represents the circuit and package parasitics from RF ports to GND.

Figure 4. Equivalent Circuit Model Schematic

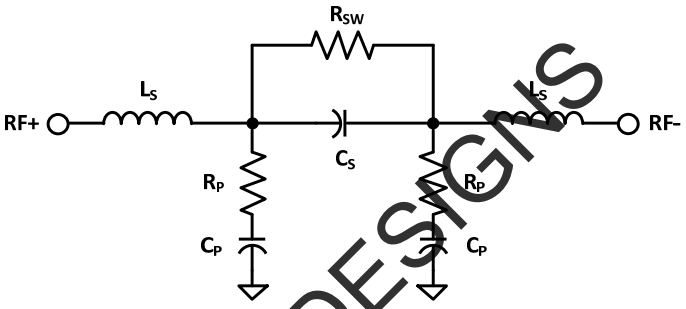


Table 6. Equivalent Circuit Model Parameters

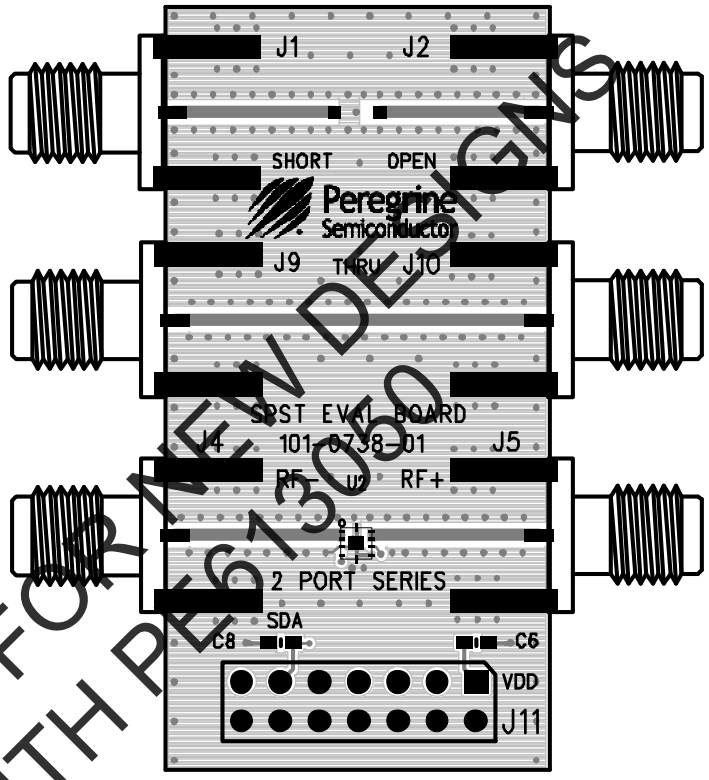
Parameter	Equation (SW=0 for OFF and SW=1 for ON)	Unit
C_S	0.40	pF
C_P	0.65	pF
R_{SW}	if SW == 1 then 1.2 else 100e3	Ω
R_P	6	Ω
L_S	0.35	nH

Evaluation Board

The 101-0738 Evaluation Board (EVB) was designed for accurate measurement of the tuning switch impedance and loss using 2 Port Series (J4, J5) configuration. Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used for performing port extensions and accounting for electrical length and transmission line loss. The Thru (J8, J10) standard can be used to estimate PCB transmission line loss for scalar de-embedding.

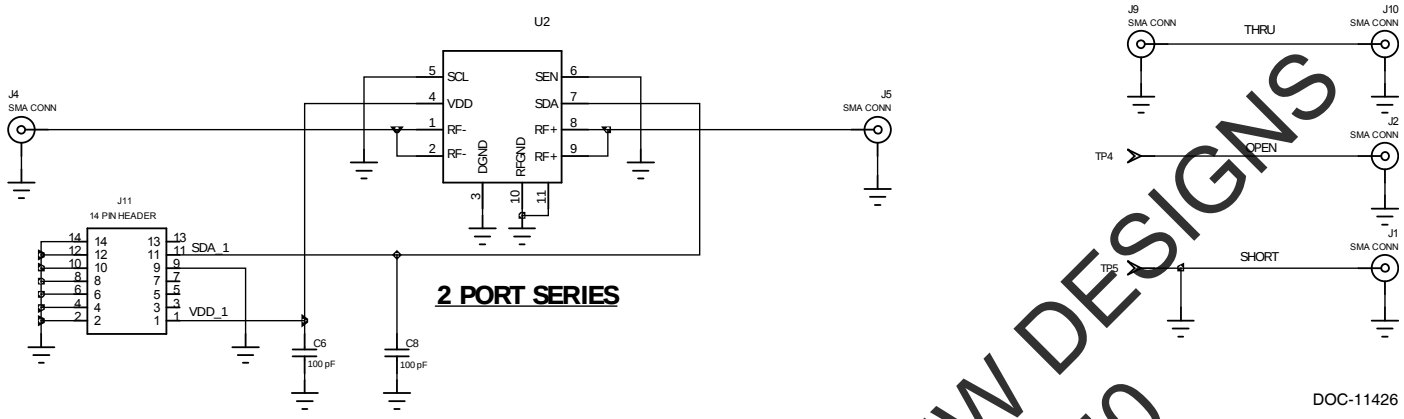
The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B (ε_r = 3.48) and 2 inner layers of FR4 (ε_r = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.051 mm).

Figure 5. Evaluation Board



PRT-08405

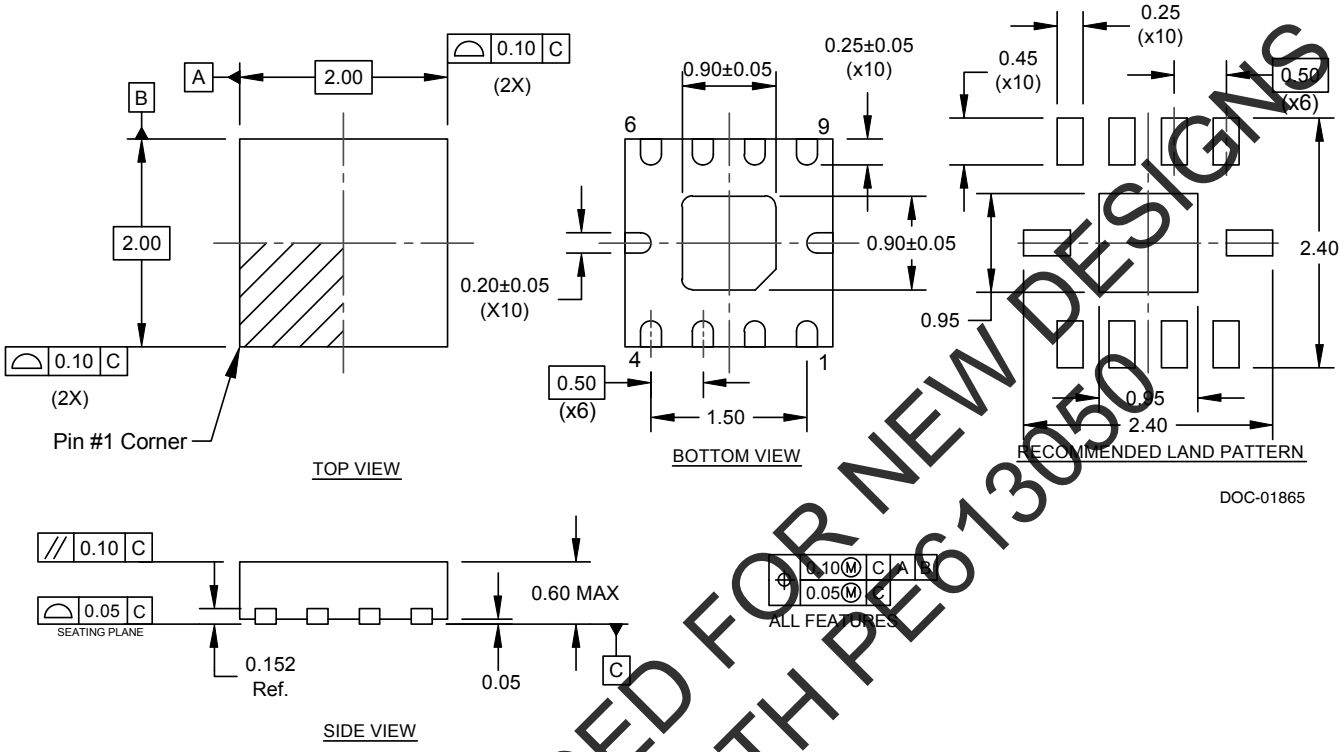
Figure 6. Evaluation Board Schematic



Note: Use PRT-08405 PCB part number.

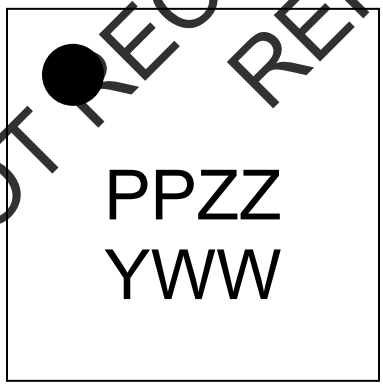
Figure 6. Package Drawing

10-lead 2 × 2 × 0.55 mm



Notes: 1. Dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M, 1994.

Figure 7. Top Marking Specifications

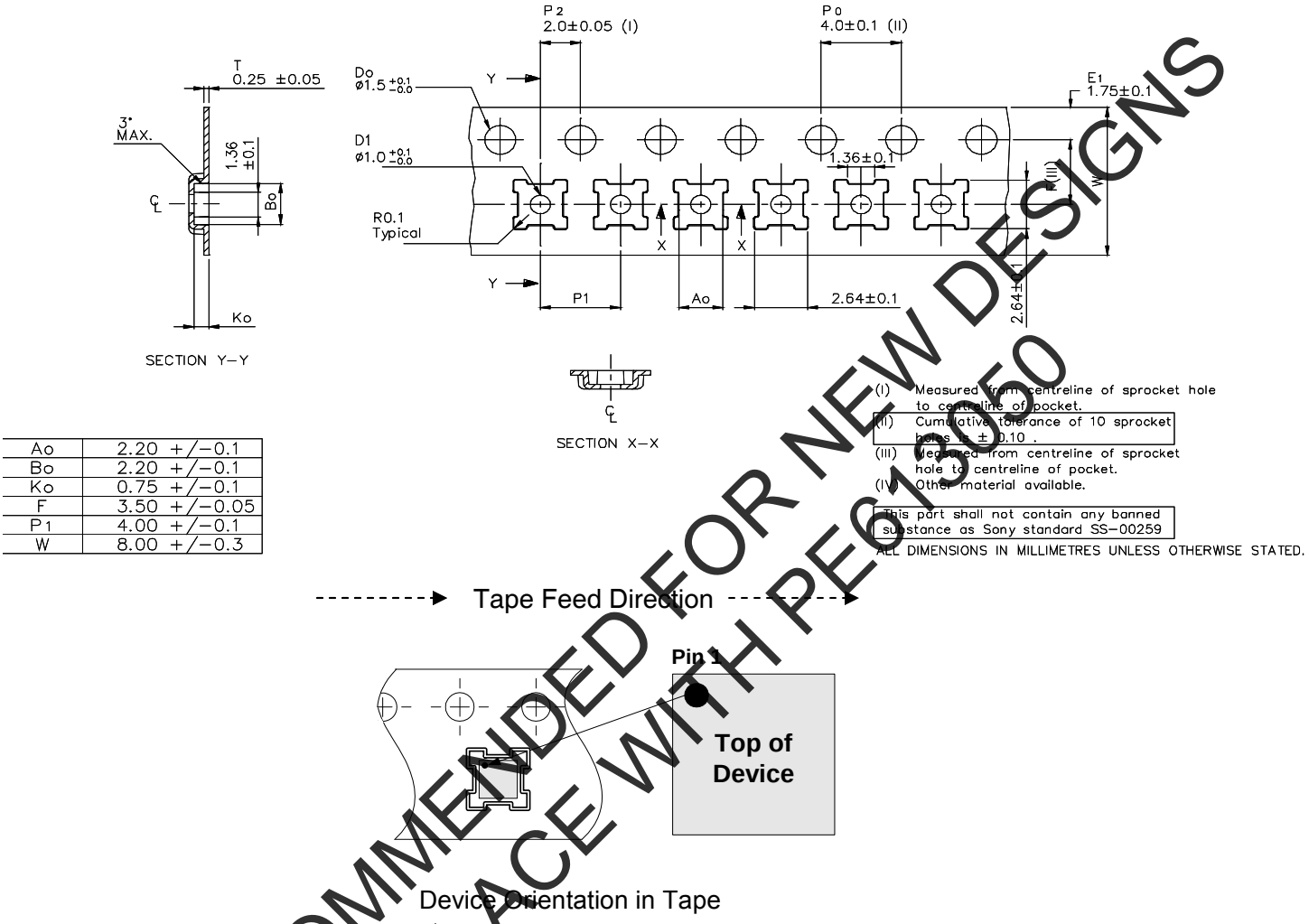


DOC-51207

Marking Spec Symbol	Package Marking	Definition
PP	DP	Part number marking for PE613010
ZZ	00–99	Last two digits of lot code
Y	0–9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc.)
WW	01–53	Work week

Note: (PP), the package marking specific to the PE613010, is shown in the figure instead of the standard Peregrine package marking symbol (P).

Figure 8. Tape and Reel Specifications



Ao	2.20 +/−0.1
Bo	2.20 +/−0.1
Ko	0.75 +/−0.1
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +/−0.3

Table 7. Ordering Information

Order Code	Package	Description	Shipping Method
PE613010MLAA-Z	10-lead QFN 2 × 2 × 0.55 mm	Package Part in Tape and Reel	3,000 units / T&R
EK613010-01	Evaluation Kit	Evaluation Kit	1 set / box

Sales and Contact Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).
The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
The Peregrine name, logo, UTSi and UltraCMOS are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com.