PCB Land Pattern and Segmented Exposed Pad Design Guidelines for Soldering Land Grid Array Packages

Scope

The objective of this application note is to provide guidelines for exposed pad land pattern and stencil design for land grid array (LGA) packages with solder mask segmented exposed pads (E-pads). Process confirmation or additional development might be necessary to optimize specific applications or performance.

Introduction

LGAs are grid array packages with terminal pads on the bottom surface. Although the lead positions on an LGA can resemble those on a quad flat no-lead (QFN) package, an LGA is typically made with organic laminate or PC board as substrate and has pads with nickel-gold (NiAu)- or nickel, palladium and gold (NiPdAu)-plated terminations. An LGA package with a segmented E-pad has a solid center ground (GND) pin for the E-pad but is divided by narrow webs of solder mask as shown in Figure 1. The solder mask web serves many purposes which help ensure the quality and reliability of the end assembly.

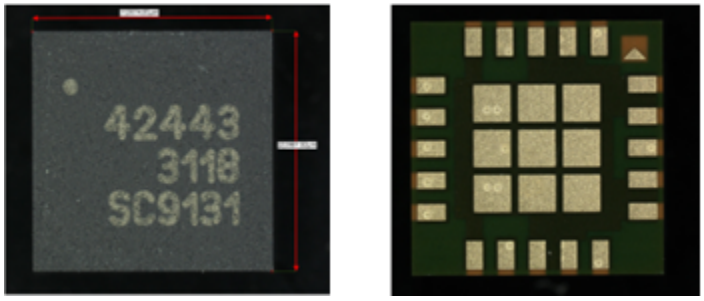

Figure 1. LGA with solder mask top side (left) and bottom side (right)

PC board land and paste patterns

A land pattern is the arrangement of pads designed on the target application board. All land patterns should be designed to follow board design requirements in IPC-351, Revision B, *Generic Requirements for Surface Mount Design and Land Pattern Standard* [1] and the PCB acceptance criteria based in IPC-A-600, *Acceptability of Printed Circuit Boards* [2] and IPC 6012, Revision F, *Qualification and Performance of Rigid Printed Boards* [3].

A land pattern design for an LGA with a segmented E-pad can follow two approaches, mirrored solder mask web or standard E-pad, as shown in Figure 2.

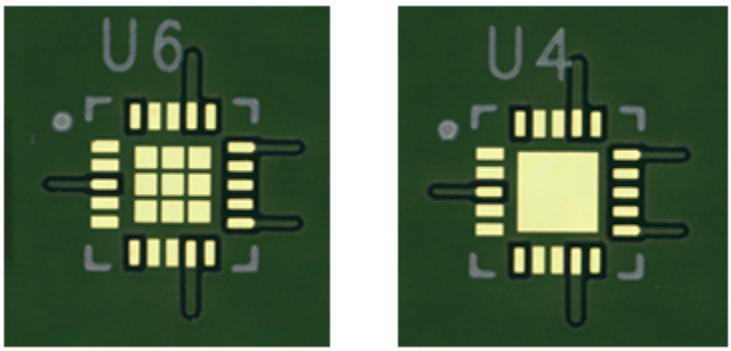

Figure 2. Land pattern with solder mask web (left) and standard land pattern (right)

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While a mirrored solder mask web GND pad is ideal and the most forgiving for circuit board assembly, a standard open E-pad can also be produced with very good success provided that the solder paste stencil is designed with the solder mask web pattern in mind. IPC-7525, *Stencil Design Guidelines* [4], refers to this solder paste design as "window pane."

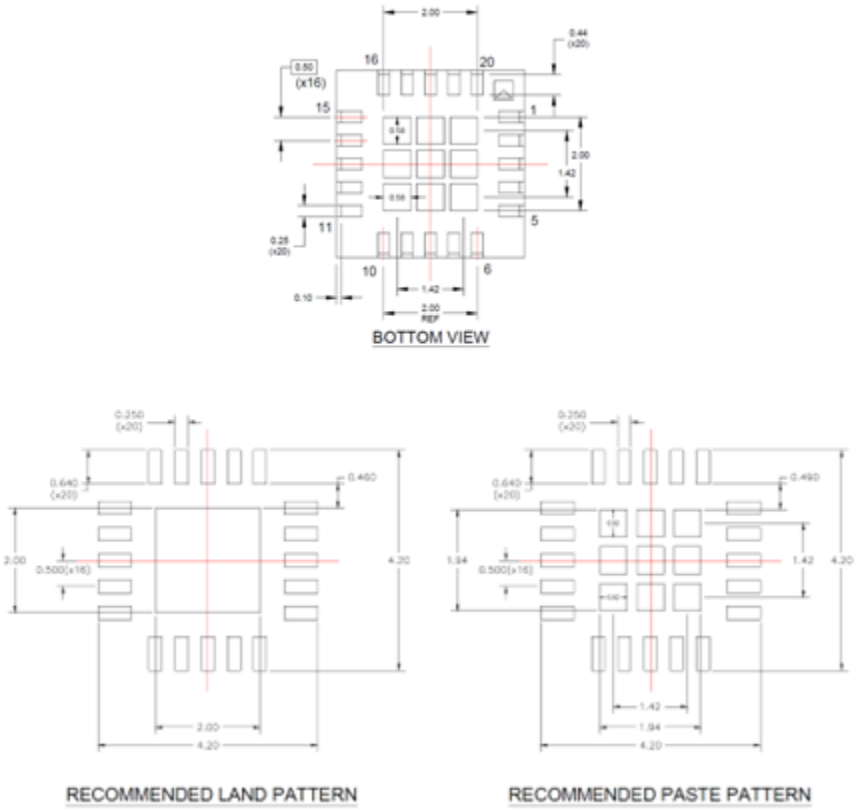

Figure 3. pSemi-recommended standard land pattern (lower left) with recommended paste pattern (lower right) to accommodate an LGA with solder mask web on E-pad (above)

pSemi offers a recommended land pattern. For parts containing a segmented E-pad, we also recommend a paste pattern. (See example in Figure 3.) Please refer to the pSemi data sheet for the part to see the recommended land pattern for the package terminal pads and the exposed pad.

Solder paste printing

Solder stencils

The formation of consistent solder joints is a requirement for good assembly yields. The contrast between a large, exposed pad and the small lead fingers of the QFN package can present a challenge in producing an even standoff height, so careful consideration should be given to an optimized stencil design.

The stencil thickness, as well as the stencil opening geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer are critical for uniform reflow soldering.

pSemi recommends inspecting the printed solder paste before parts placement. A repeatable brick-shaped solder deposit is the most important factor for robust reflow yields. Refer to IPC-7525, *Stencil Design Guidelines*. [4]

Exposed pad stencil design

Typically, the PCB board assembly house designs the solder paste stencil. The PCB assembly house receives the PCB CAD design data which sometimes only includes the data for the PCB and not the details of the parts being placed other than the BOM. Best practice is to provide the PCB assembly house with as much information as possible to increase its chances of first-time success.

Common practice within PCB design is to make the paste data layer 1:1 with the exposed pads on the PCB land pattern. This is the starting data that the PCB assembly house uses for paste stencil design. However, in the case of parts with a solder mask web, it is helpful for the PCB designer to design the paste data layer according to solder mask web on the part. The most important aspect of this is for the locations of the paste window panes to be aligned with the LGA package as shown in Figure 4.

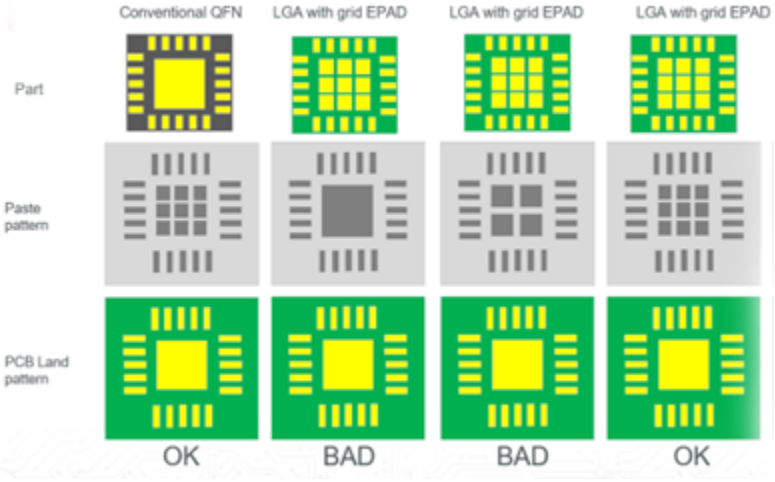

Figure 4. Package, solder paste, and PCB land pattern

The LGA package can be thermally and electrically enhanced when it has the exposed die attach pad on the underside of the package. The exposed pad should be soldered down to the PCB.

It is good practice to minimize voids within the exposed pad interconnection, so the design of the exposed pad stencil is crucial. The segmented stencil design enables outgassing of the solder flux during reflow and regulates the finished solder thickness. Typically, the stencil apertures are reduced such that the solder paste coverage is 1:1 with the exposed pad. However, this results in excessive paste volume that will "float" or "skate" the part, causing electrical opens and other manufacturing defects. The amount of voiding post-reflow in the exposed pad should not exceed 30% according to IPC-A-610, *Acceptability for Electronic Assemblies* [5]. pSemi recommends checking presence and number of voids using X-rays post-reflow. Destructive tests, such as X-sectioning the package, should be done for further analysis if needed.

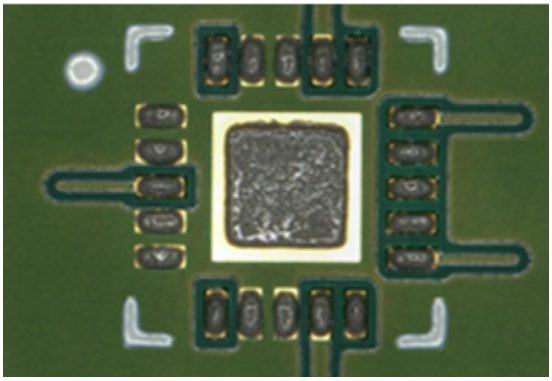

Figure 5. Standard exposed pad

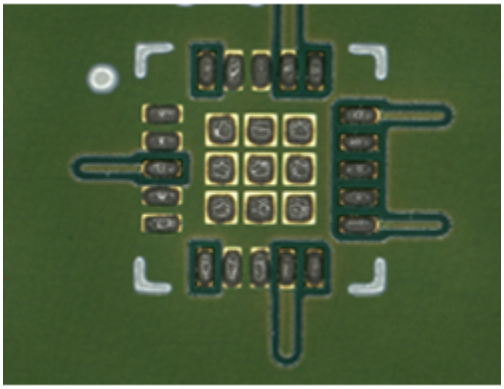

Figure 6. Segmented land pattern with paste

Exposed pad segmentation done using stencil aperture reduction is also an option for users. Figure 7 shows the solder paste print on a substrate with 30%–35% reduction in solder paste volume. By optimizing volume using stencil aperture reduction, costly board design changes and added cycle times to procure new boards are eliminated.

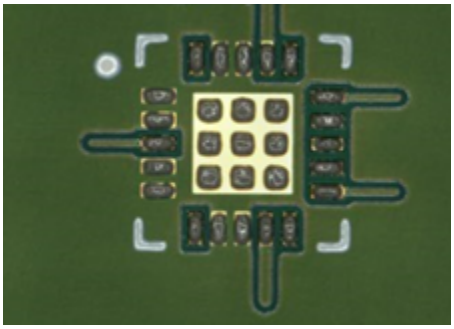

Figure 7. Segmented using stencil aperture reduction

pSemi recommends using stencil aperture reduction for optimized solder volume as shown in Figure 6 and Figure 7.

X-ray inspection shows the standard exposed pad has a large void (> 30%) as shown in Figure 8. In Figure 9, the segmented exposed pad shows smaller voids that are within the 30% void specification of IPC-A-610. This is one of the advantages of segmentation.

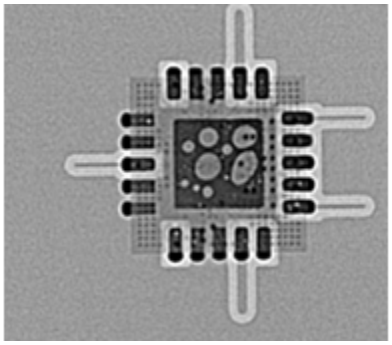

Figure 8. Large voids in the exposed pad

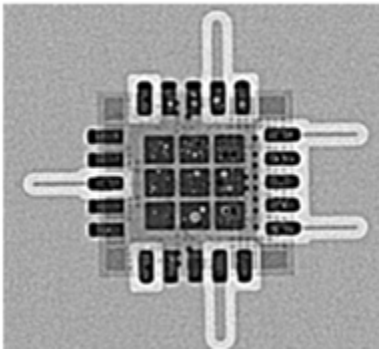

Figure 9. Reduced voids in the segmented pad

Termination pad stencil design

The stencil aperture for the terminal fingers is typically designed to match the PCB/substrate pad size 1:1. For fine pitch components of 0.5 mm pitch and below, it may be necessary to reduce the stencil aperture by 20%–30% to prevent shorting beneath the LGA.

Conclusion

Based on the above evaluations, pSemi requires customers to use a segmented land pattern on PCB exposed pad or use stencil aperture reduction to optimize solder volume on the standard exposed pad. This results in controlled reflow and robust solder joints.

References

1. IPC-7351, Revision B—*Generic Requirements for Surface Mount Design and Land Pattern Standard*
2. IPC-A-600—*Acceptability of Printed Circuit Boards*
3. IPC-6012, Revision F—*Qualification and Performance for Rigid Printed Boards*
4. IPC-7525—*Stencil Design Guidelines*
5. IPC-A-610—*Acceptability of Electronic Assemblies*

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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