ARC1C0608/ARC1C0605

Document Category: Product Specification

High-efficiency LED Backlight Driver

General Description

The ARC1C0608/ARC1C0605 is an ultra-high efficiency DC-DC converter solution with integrated programmable current sinks that drive up to six strings of LEDs. The ARC1C0608/ARC1C0605 integrates all MOSFETs and their control and driver circuitry. With a proprietary architecture, the ARC1C0608 provides the highest efficiency (>93%) possible in a compact WLCSP-35 package. The 0.4 mm pitch and high switching frequency enables a small solution size aligned to the needs of the newest mobile products.

Features

- Synchronous DC-DC converter with integrated FETs
- Single-cell Li-Ion battery input voltage: 2.7V to 5.5V
- Patented architecture for ultra-high LED efficiency, above 90% over most of the operating range
- Integrated output disconnect switch
- Up to 30V output for maximum flexibility in assignment of LEDs to strings and selection of LED forward voltage
- 12 bits hybrid (mixed) linear dimming mode and 10 bits logarithmic mapping
- Up to 12 bits resolution with DC or PWM dimming
- LED brightness ramp up/down control with programmable ramp rate and linear/logarithmic ramp profiles
- Phase-shifted PWM dimming among active strings to minimize audible noise
- 1 MHz I²C 6.0-compatible serial interface to program the brightness, or an external resistor on ISET to set the maximum brightness
- External PWM input for fine dimming resolution
- Six independently enabled current sinks, up to 25 mA per current sink
- +/-0.8% max/min current sink matching accuracy at 25 mA
- Wide range of input and output voltages with 3x/2x charge pump ratio
- Selectable boost switching frequency from 320 KHz to 3.4 MHz
- Extensive fault protection including boost over-current protection, output short circuit protection, output over-voltage protection, LED open and short protection, and thermal shutdown

Typical Applications

- Low-profile point-of-load (POL) regulators
- Optical modules
- Core supplies
- ASICs
- FPGA

Efficiency

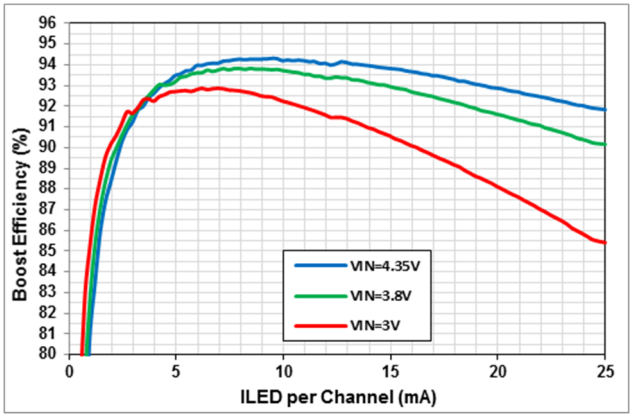

Figure 1. Efficiency Plot of Single Device

Simplified Application

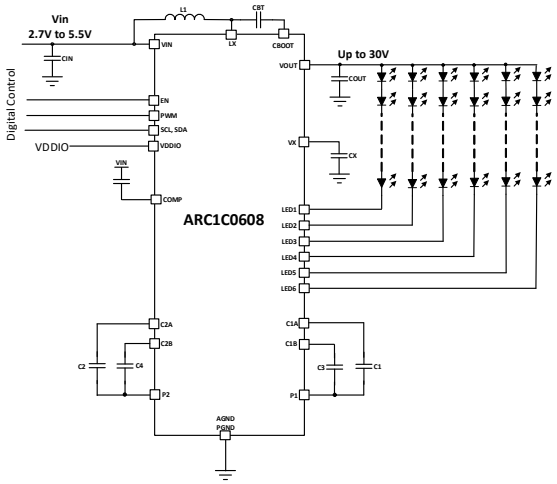

Figure 2. Typical Applications Circuit

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Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1

Table 1. ARC1C0608/ARC1C0605 Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{IN}, VDDIO to AGND	-0.3	6	V
SCL, SDA to AGND	-0.3	6	V
V_{OUT} to AGND	-0.3	36	V
LEDx to AGND	-0.3	26.4	V
AGND to PGND	-0.3	0.3	V
LX, VX, P1, P2 to PGND	-0.3	13.2	V
VX to LX, P1, P2	-0.3	13.2	V
C1A, C2A to VX	-0.3	13.2	V
C2B to C1A, C1B to C2A	-0.3	26.4	V
CBOOT to V_{IN}	-0.3	13.2	V
CBOOT to LX	-0.3	6	V
COMP, ISET, FSET, PWM, EN, to AGND	-0.3	6	V
Storage Temperature	-65ºC	150 º C	º C
Junction Temperature	-40ºC	150 º C	º C
Parameter	**Value**		
Operating Bump or Lead Temperature (soldering, reflow)	260 º C		
ESD Tolerance, HBM(3)	1kV		
ESD Tolerance, CDM(4)	1kV		

Notes:

1. The application of any stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device, and exposure at any of these ratings for extended periods may reduce the reliability of the device.
2. The above Absolute Maximum Ratings are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.
3. Human body model, per the JEDEC standard JS-001-2012.
4. Field-induced charge device model, per the JEDEC standard JESD22-C101.

Recommended Operating Conditions

Table 2 lists the ARC1C0608/ARC1C0605 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. ARC1C0608/ARC1C0605 Recommended Operating Conditions

Parameter	Min	Max	Units
V_{IN} Input Voltage Range	2.7	5.5	V
V_{OUT} Output Voltage Range (*)	12	30	V
VX Boost Output Voltage Range	$1.2 \times V_{IN}$	11	V
VDDIO Voltage Range	1.8	5.5	V
Junction Temperature Range, T_J	-40	125	°C

Note: * Output voltage operating range is also subject to an integer multiple of the boost output voltage range, as set by the programmable charge pump ratio of 2 or 3.

Package Thermal Characteristics(1),(2)

Table 3 lists the package thermal characteristics for the ARC1C0608/ARC1C0605.

Table 3. Package Thermal Characteristics

Parameter	WLCSP-35	Units
Junction-to-Ambient Thermal Resistance (Θ_{JA}), soldered thermal pad, connected to ground plane	44.5	°C/W
Junction-to-Board Thermal Characterization (Ψ_{JB})	10.8	°C/W
Junction-to-Top Case Characterization (Ψ_{JC})	6.5	°C/W

Notes:

1. Package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.
2. Junction-to-Ambient Thermal Resistance (ΘJA) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.

Electrical Characteristics

V_{IN} = 3.8V, V_{AGND} = V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 4. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply						
Input voltage range	V_{VIN}	Full parametric performance	2.7		5.5	V
Under-voltage lockout (UVLO) threshold low	V_{UVLO_L}	V_{VIN} falling	2.3			V
Under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{VIN} rising			2.69	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}			75		mV
Shutdown supply current	I_{VIN_STDBY}	I_{VIN} with VEN = 0V			1	µA
No switching supply current	$I_{VIN\_NO\_SW}$	LEDs disabled, no powertrain switching VEN = V_{VIN}, fSW_BOOST = 1.024 MHz		2.75		mA
Thermal shutdown threshold (3)	T_{TSD}			150		°C
Thermal shutdown hysteresis (3)	T_{TSD_HYST}			20		°C
Soft start time-out duration				10		ms
Step-Up Converter – Boost						
Boost switching frequency range	f_{SW_BOOST}	I^2C interface only; FSW_BOOST[4:0]=02h to 1Fh	0.32		3.41	MHz
		Non-I^2C interface only: FSET = V_{IN}		2.56		
		Non-I^2C interface only: FSET = Open		1.024		
		Non-I^2C interface only: FSET = AGND		0.512		
Boost switching frequency accuracy			-6		+6	%
Boost minimum off-time	$T_{OFF\_BOOST\_MIN}$			50		ns
Boost minimum on-time	$T_{ON\_BOOST\_MIN}$	Boost_mode=1 only		50		ns
Boost low-side switch current limit, cycle-by-cycle	I_{BOOST_LIMIT}	I_{LX} rising		2.9		A
Boost low-side switch current limit, secondary	$I_{BOOST\_LIMIT\_SEC}$	I_{LX} rising		4.8		A
Step-Up Converter – Charge Pump						
Output over-current threshold	I_{OUT_OC}	I_{OUT} rising	450			mA
Output under-voltage threshold	V_{OUT_UVP}	V_{OUT} rising		11.2		V
	V_{OUT_OVP}	OVP_TH[1:0]=00		31.4		V

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Output over-voltage threshold		V_{OUT} rising, I^2C interface only	OVP_TH[1:0]=01		24		
			OVP_TH[1:0]=10		20		
			OVP_TH[1:0]=11		16		
		V_{OUT} rising, non-I^2C interface only, 3x charge pump ratio (ARC1C0608)			31.4		
		V_{OUT} rising, non-I^2C interface only, 2x charge pump ratio (ARC1C0605)			20		
Output over-voltage hysteresis	$V_{OUT\_OVP\_HYST}$	V_{OUT} rising - V_{OUT} falling			0.5		V
LED Current Sinks (LED1 To LED6)							
ISET voltage	V_{ISET}	Non-I^2C interface only		0.388	0.4	0.412	V
ISET internal current multiplier	K_{ISET}	Non-I^2C interface only. I_{LED_MAX} = V_{ISET}/R_{ISET} x K_{ISET}			1562.5		A/A
ISET recommended resistor range	R_{ISET}	Excluding resistor tolerance		24.9		250	kΩ
LED current full-scale output range	I_{LED_MAX}	I^2C interface only	MAX_I[1:0]=00		10		mA
			MAX_I[1:0]=01		15		
			MAX_I[1:0]=10		20		
			MAX_I[1:0]=11		25		
LED current matching (4)	$I_{LED\_MATCHING}$	I_{LEDX} programmed to 25 mA		-0.8		+0.8	%
LED current accuracy (4)	$I_{LED\_ACCURACY}$	I_{LEDX} programmed to 25 mA, V_{IN} = 2.7V to 4.5V		-2.5		+2.5	%
		I_{LEDX} programmed to 25 mA, V_{IN} > 4.5V		-3.25		+3.25	%
LED regulation voltage	$V_{LED\_REGULATION}$	I_{LEDX} programmed to 25 mA T_A = 25°C			350		mV
LED shorted string detection threshold		V_{LEDX} rising			6.2		V
LED PWM output frequency	f_{ILEDX}	I^2C interface program range with DIM_MODE = 1		2.5		40	KHz
LED current sink minimum controllable on-time or off-time					0.2		µs
PWM Dimming Control Interface							
PWM input frequency	F_{PWM}			2.65		40	KHz
PWM input minimum pulse on-time (2)					0.1		µs
PWM input minimum pulse off-time (2)					0.1		µs
PWM input high voltage	V_{IH_PWM}			1.1			V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PWM input low voltage	V_{IL_PWM}				0.4	V
PWM input current	I_{PWM}		-1.0		1.0	µA
Logic Interface (EN, FSET)						
EN input high voltage	V_{IH_EN}		1.1			V
EN input low voltage	V_{IL_EN}				0.4	V
EN input current	I_{EN}		-1.0		1.0	µA
EN input logic low width to shutdown			3.0			ms
FSET input resistance	$I_{\_FSET\_R}$	Non-I²C interface only		100		kΩ
FSET input low voltage	V_{IL_FSET}	Non-I²C interface only			0.4	V
FSET input high voltage	V_{IH_FSET}	Non-I²C interface only	V_{VIN} -0.4			V
I²c Serial Interface (SCL, SDA, VDDIO)						
VDDIO supply voltage range	V_{DDIO}		1.62		5.5	V
SDA, SCL input high voltage	V_{IH}		0.7 x V_{VDDIO}			V
SDA, SCL input low voltage	V_{IL}				0.3 x V_{VDDIO}	V
SDA, SCL input hysteresis	V_{HYS}		0.05 x V_{VDDIO}			V
SDA, SCL input current	I_{SCL}, I_{SDA}		-1		+1	µA
SDA output low level (2)	V_{OL}	I_{SDA} = 20 mA			0.4	V
I²C interface initial wait time		Initial wait time from EN logic high to first I²C command accepted	350			µs
SDA, SCL pin capacitance (2)	$C_{I/O}$				10	pF
Serial clock frequency	F_{SCL}	Standard mode			100	KHz
		Fast mode			400	KHz
		Fast mode plus			1	MHz
Clock low period	t_{LOW}	Standard mode	4.7			µs
		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
Clock high period	t_{HIGH}	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
	t_{BUF}	Standard mode	4.7			µs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
BUS free time between a STOP and a START condition		Fast mode	1.3			µs
		Fast mode plus	0.5			µs
Setup time for a repeated START condition	$t_{SU:STA}$	Standard mode	4.7			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Hold time for a repeated START condition	$t_{HD:STA}$	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Setup time of STOP condition	$t_{SU:STO}$	Standard mode	4			µs
		Fast mode	600			ns
		Fast mode plus	260			ns
Data setup time	$t_{SU:DAT}$	Standard mode	250			ns
		Fast mode	100			ns
		Fast mode plus	50			ns
Data hold time	t_{HD_DAT}	Standard mode	0		3.45	µs
		Fast mode	0		900	ns
		Fast mode plus	0		450	ns
Rise time of SCL signal	t_{RSCL}	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns
Fall time of SCL signal	t_{FSCL}	Standard mode			300	ns
		Fast mode			300	ns
		Fast mode plus			120	ns
Rise time of SDA signal	t_{RSDA}	Standard mode			1000	ns
		Fast mode	20		300	ns
		Fast mode plus			120	ns
Fall time of SDA signal (2)	t_{FSDA}`	Standard mode			300	`ns
		Fast mode	20 x VDDIO/ 5.5V		300	ns
		Fast mode plus	20 x VDDIO/ 5.5V		120	ns
Capacitive load for SDA and SCL	C_{BUS}	Standard mode			400	pF
		Fast mode			400	pF
		Fast mode plus			550	pF

Parameter	Symbol	Conditions	Min	Typ	Max	Units

Notes:

1. Min/max specifications are 100% production tested at TA=25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Guaranteed by design.
3. Thermal shutdown is guaranteed by design.
4. LED current accuracy is based on the average of all six LED current outputs, I_{LED_AVG}, compared to the LED current setting, $I_{LED\_SETTING}$. Accuracy = 100% x[(I_{LED_AVG}/$I_{LED\_SETTING}$)-1]. LED current matching is based on the highest (I_{LED_HIGH}) and lowest (I_{LED_LOW}) of all six LED current outputs compared to the average, at a given LED current setting. Matching = 100% x (I_{LED_HIGH} – I_{LED_LOW})/I_{LED_AVG}.

I²C Timing Diagram

The serial interface timing diagram for Standard Mode, Fast Mode, and Fast Mode Plus is given in Figure 3.

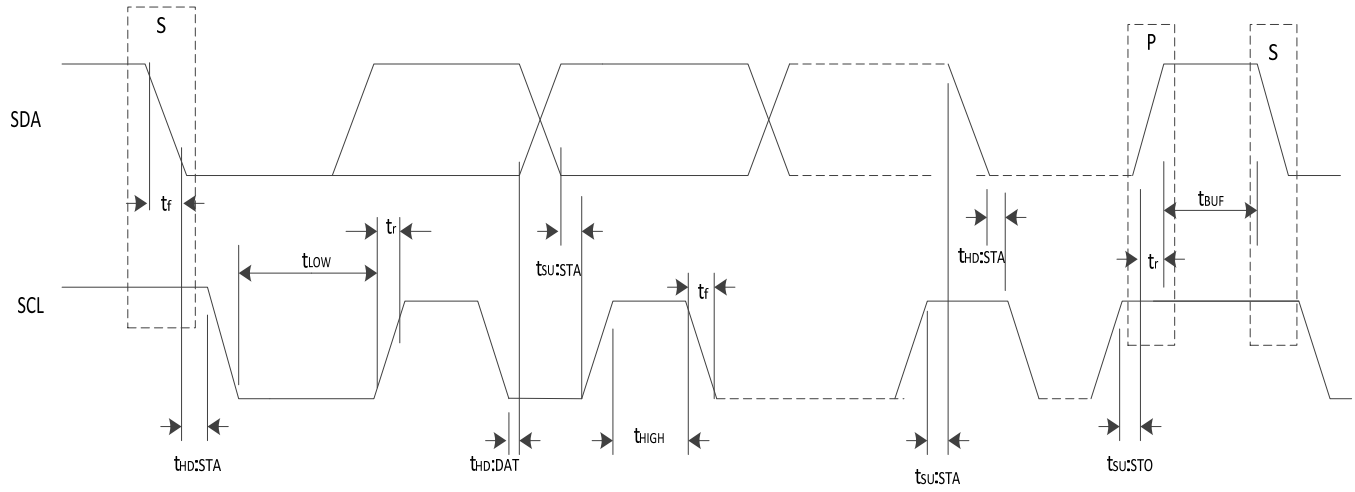


Figure 3. Serial Interface Timing Diagram for Standard, Fast, and Fast Mode Plus

Pin Functions and Configurations

The pin configuration for the ARC1C0608 / ARC1C0605 package is shown in Figure 4.

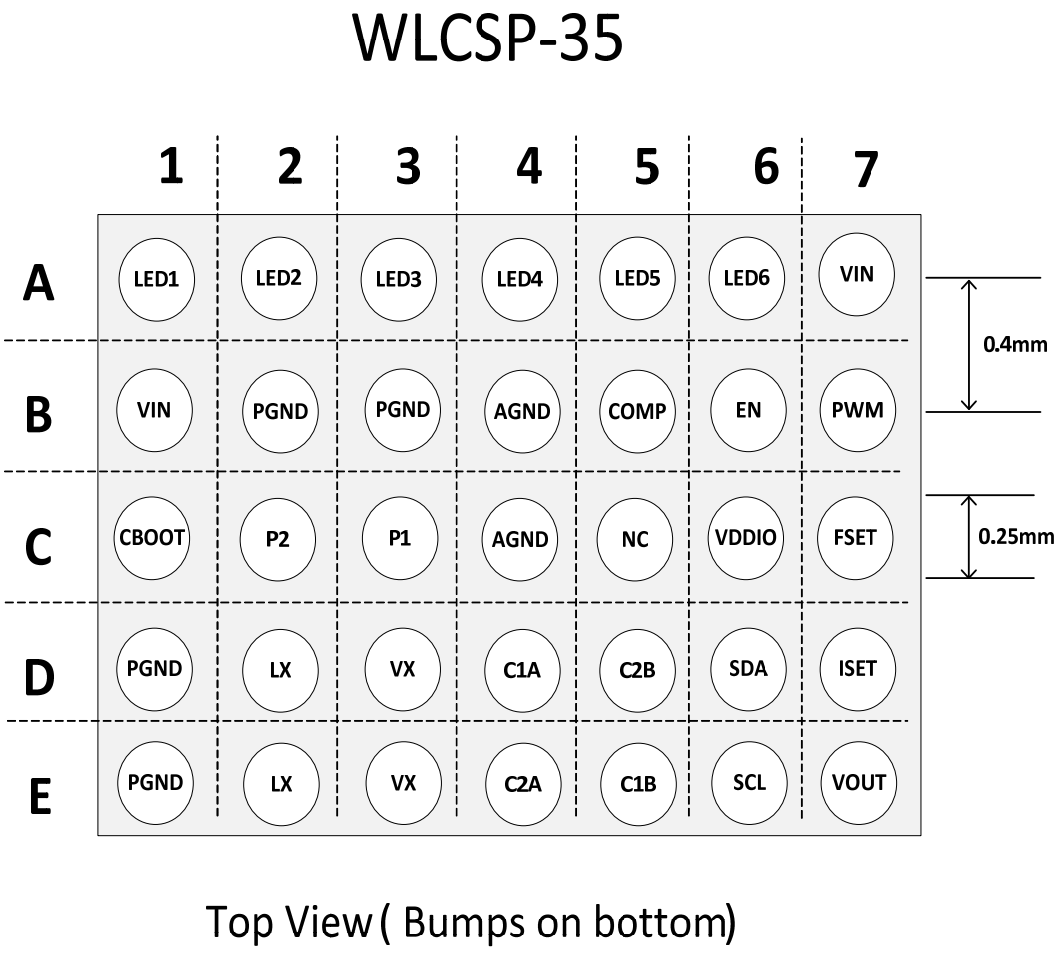


Figure 4. Package Drawing

Pin Descriptions

Pin descriptions for the ARC1C0608/ ARC1C0605 device are given in Table 6.

Table 5. Pin Descriptions

Pin Name	Pin No.	Description
VIN	B1, A7	Input voltage, battery power supply pin. Connect both pins together externally with a low-impedance trace.
LX	D2, E2	Fully synchronous switching node for the boost power inductor, which connects between LX and input voltage V_{IN}.
C1A	D4	Charge pump fly capacitor to be externally connected between C1A and P1.
C1B	E5	For 3x charge pump ratio, a charge pump fly capacitor is to be externally connected between C1B and P1 pins. For 2x charge pump ratio, short this pin to the C2A pin and do not connect an external capacitor between C1B and P1 pins.
C2A	E4	Charge pump fly capacitor to be externally connected between C2A and P2.
C2B	D5	For 3x charge pump ratio, a charge pump fly capacitor is to be externally connected between C2B and P2 pins. For 2x charge pump ratio, short this pin to the C1A pin and do not connect an external capacitor between C2B and P2 pins.
P1	C3	Phase node for charge pump fly capacitors at C1A and C1B
P2	C2	Phase node for charge pump fly capacitors at C2A and C2B
VX	D3, E3	Charge pump input node, internally driven by the output of the boost converter. Connect externally to a capacitor per Recommended BOM List on page 39.
VOUT	E7	Power converter output voltage, to be externally connected to the high side of all LED strings. Connect a 1MΩ resistor between V_{OUT} pin to GND.
PWM	B7	PWM dimming input for brightness control. Connect to V_{IN} if not used.
LED1 – LED6	A1-A6	Individual LED current sinks, to be externally connected to the low side of individual LED strings. Connect unused LED current sink(s) to AGND.
AGND	B4, C4	Analog ground; must tie externally to ground plane.
PGND	B2, B3, D1, E1	Power ground; must tie externally to ground plane. High current path.
SCL	E6	Serial clock for I^2C bus. When an I^2C interface is not used, connect this pin to AGND or leave open.
SDA	D6	Serial data for I^2C bus. When an I^2C interface is not used, connect this pin to AGND or leave open.
VDDIO	C6	Digital I/O supply voltage for I^2C interface. When an I^2C interface is used, connect this pin to the I^2C bus supply voltage. When an I^2C interface is not used, connect this pin to AGND.
COMP	B5	Compensation pin.
EN	B6	Enable input.
ISET	D7	LED current setting pin. Connect a resistor from this pin to AGND to set the full-scale LED current in non-I^2C mode. Leave this pin open in I^2C mode.
FSET	C7	Float this pin or tie it to ground or V_{IN} to set the boost switching frequency in non-I^2C mode. See application section for more detail.
CBOOT	C1	Bootstrap capacitor for boost stage high side FET.

Table 6. Pin Descriptions

Functional Block Diagram

The functional block diagram for ARC1C0608 is given in Figure 5.

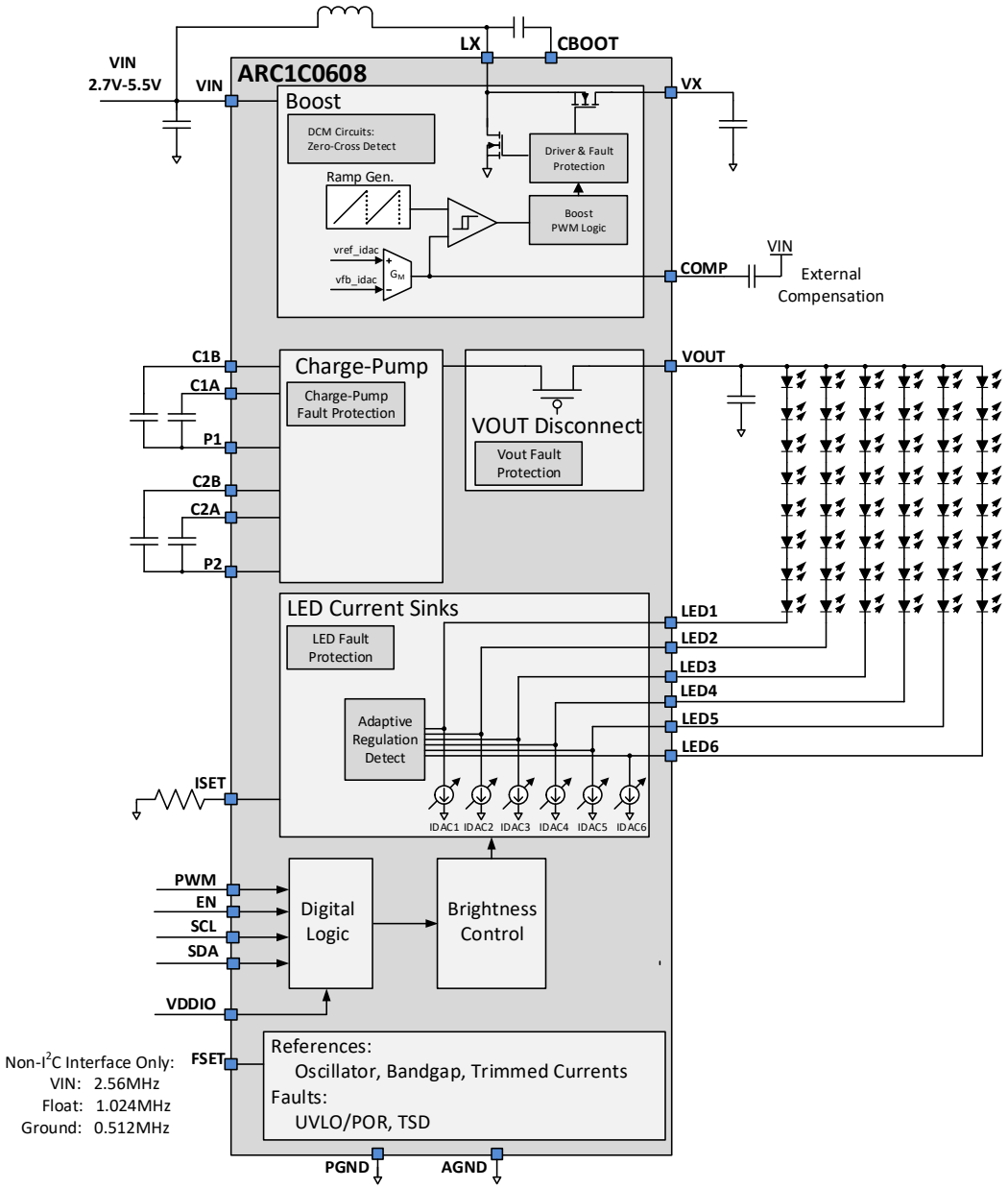


Figure 5. Block Diagram

Application Circuit

The application schematic for the 3x charge pump ratio is shown in Figure 6.

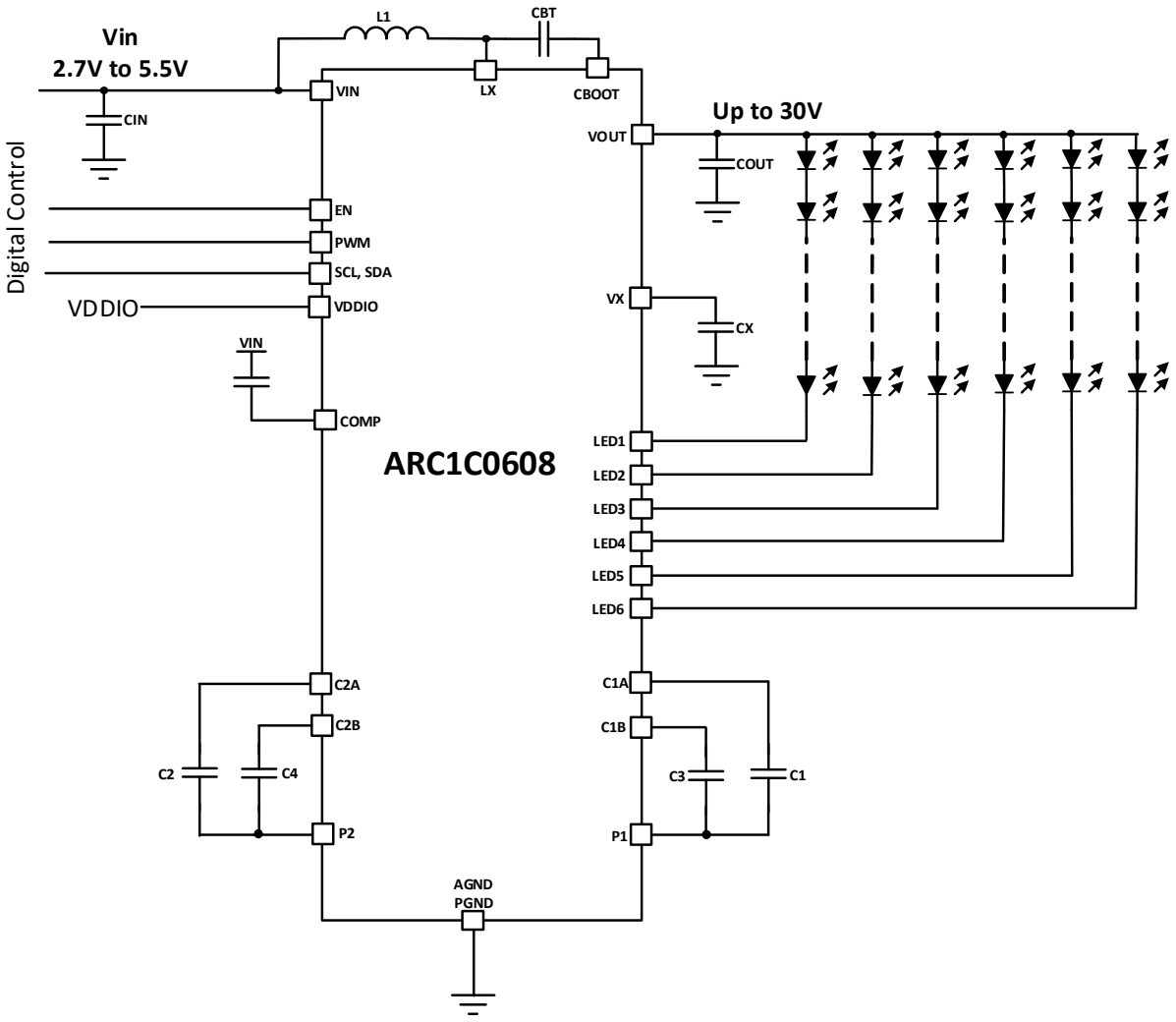


Figure 6. Application Schematic for 3x Charge Pump Ratio

The application schematic for the 2x charge pump ratio is shown in Figure 7.

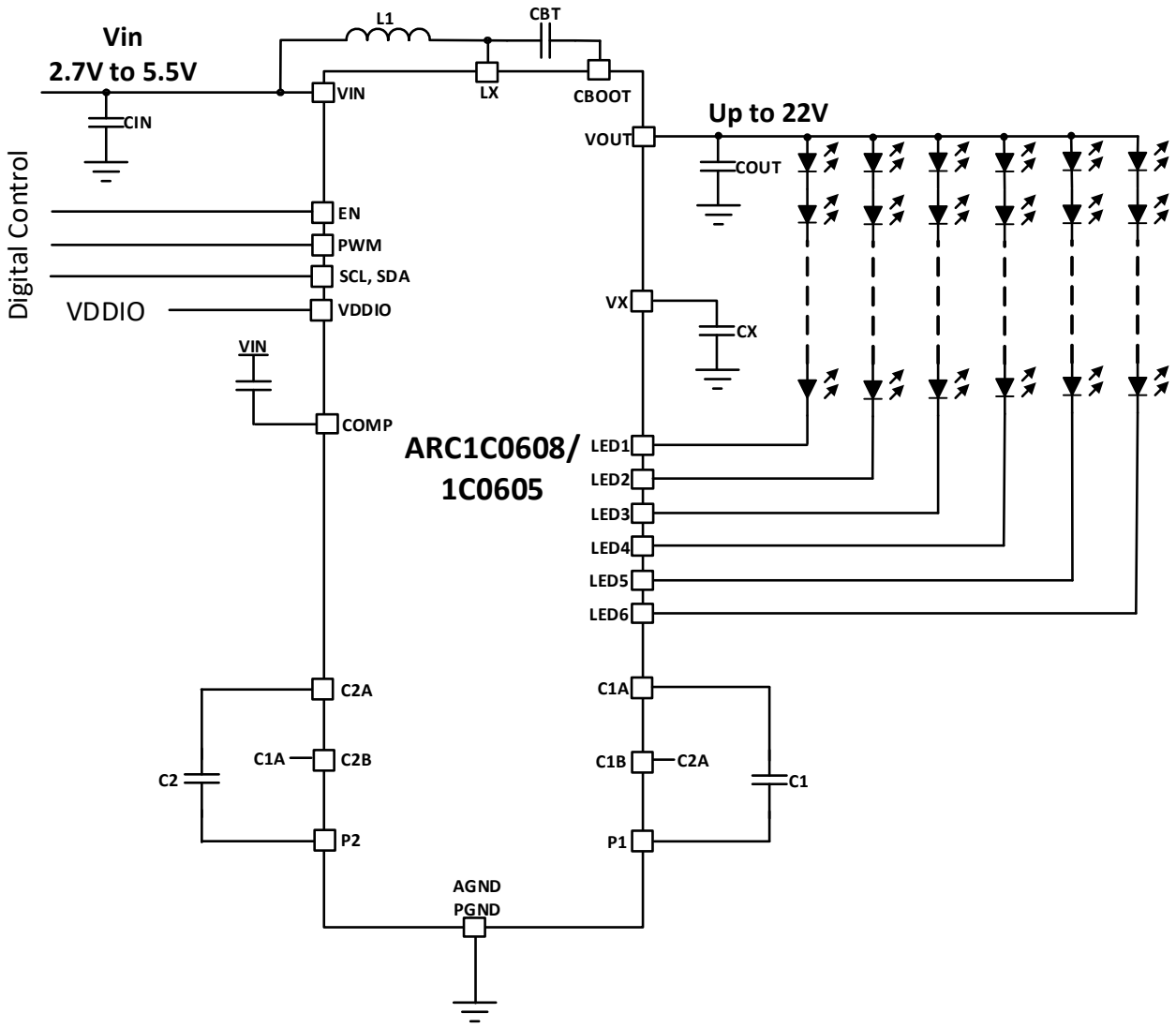


Figure 7. Application Schematic for 2x Charge Pump Ratio

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 3.8V, L = 6.8 µH Murata DFE322512F-6R8M, Cout = 1 µF, LED VF = 2.85V (typ), f_{SW_BOOST} = 512 KHz

LED Efficiency

The LED efficiency for 6p6s over V_{IN} range is shown in Figure 8, and the LED efficiency for 4p8s over V_{IN} range is shown in Figure 9.

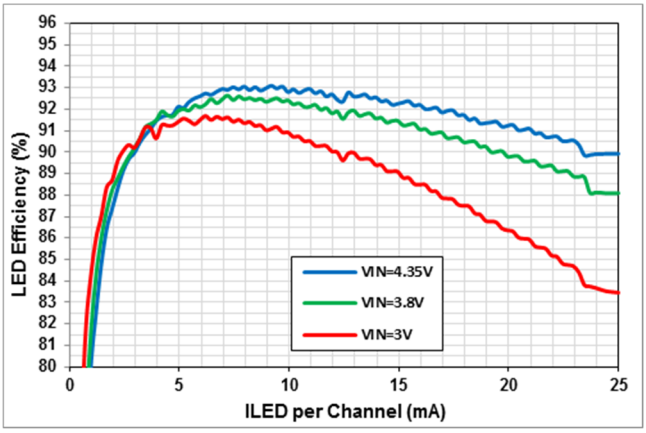


Figure 8. 6p6s LED Efficiency Over V_{IN} Range

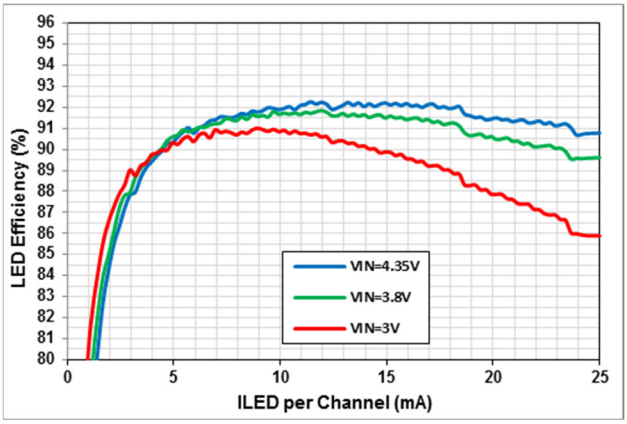


Figure 9. 4p8s LED Efficiency Over V_{IN} Range

LED Current Sinks

LED mismatch in linear mode is given in Figure 10 and LED accuracy in linear mode is shown in Figure 11.

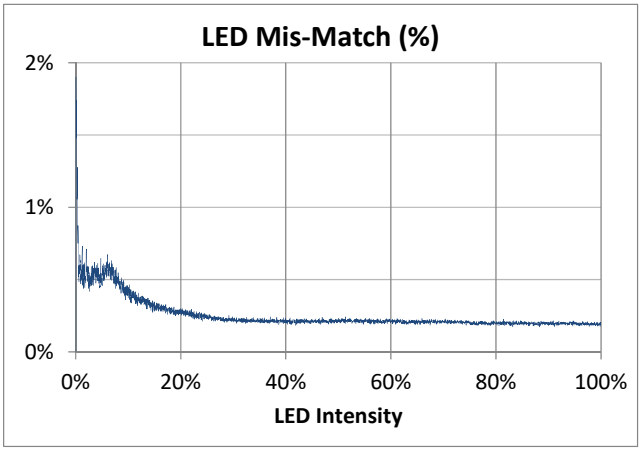


Figure 10. LED Mismatch – Linear Mode

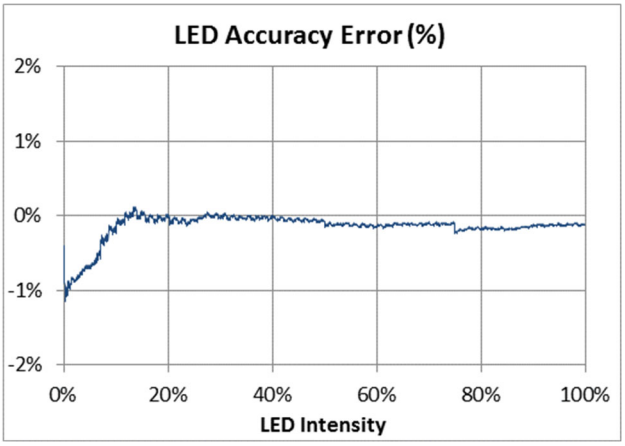


Figure 11. LED Accuracy – Linear Mode

Typical Performance Characteristics (contd.)

Unless otherwise specified: V_{IN} = 3.8V, L = 6.8 µH Murata DFE322512F-6R8M, Cout = 1 µF, LED VF = 2.85V (typ), fSW_BOOST = 512 KHz.

Startup Waveforms

Startup under 1% PWM duty cycle is depicted in Figure 12, and startup under 50% PWM duty cycle is depicted in Figure 13.

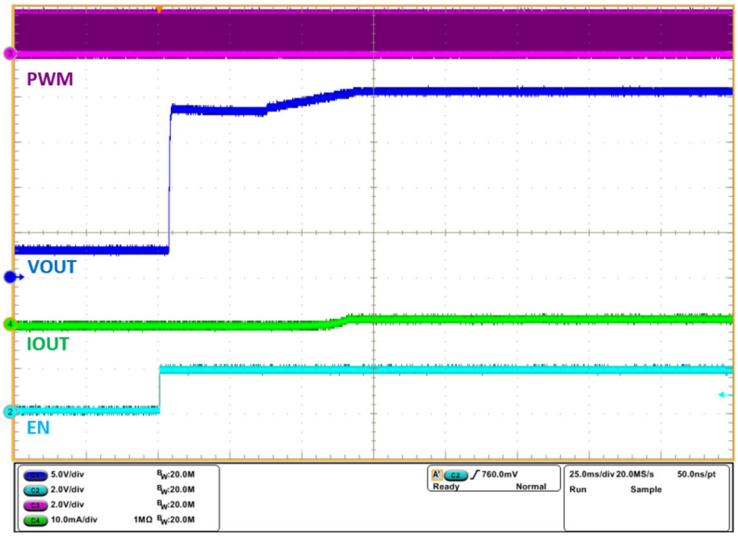


Figure 12. Startup Under 1% PWM Duty Cycle

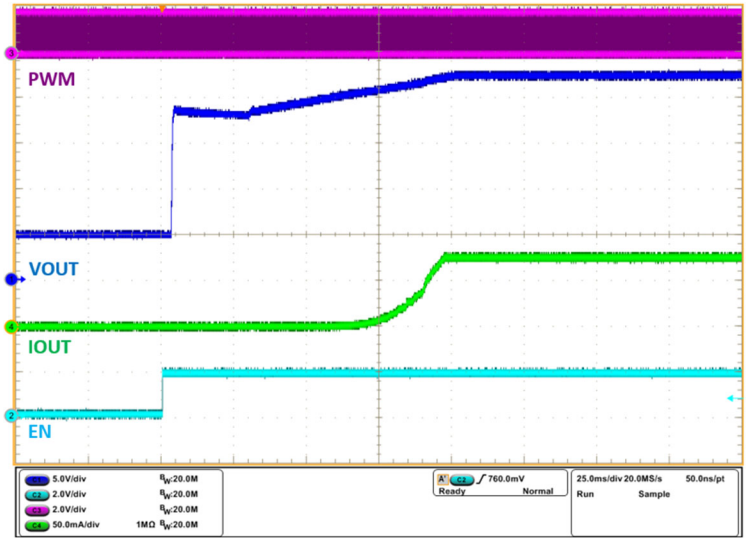


Figure 13. Startup Under 50% PWM Duty Cycle

Typical Performance Characteristics (contd.)

Unless otherwise specified: V_{IN} = 3.8V, L = 6.8 µH Murata DFE322512F-6R8M, Cout = 1 µF, LED VF = 2.85V (typ), fSW_BOOST = 512 KHz

Startup Waveforms

Startup under 99% PWM duty cycle is depicted in Figure 14.

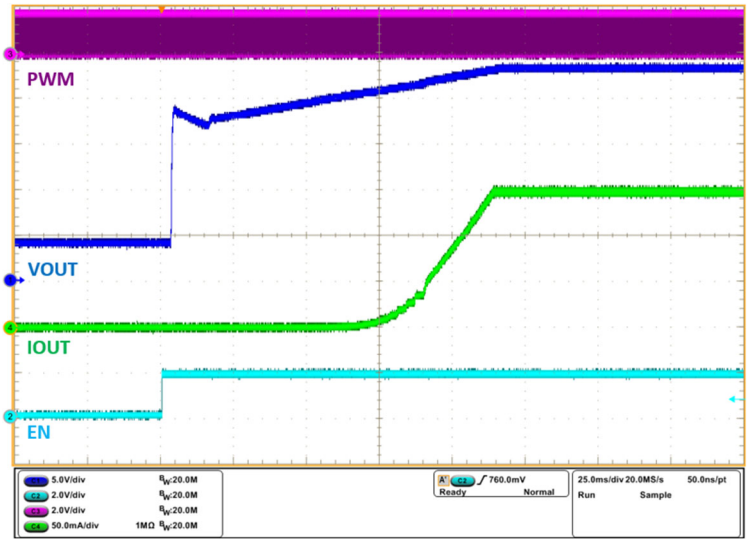


Figure 14. Startup Under 99% PWM Duty Cycle

Thermal Performance

The thermal performance of ARC1C0608 is shown in Figure 15.

Figure 15. ARC1C0608 Thermal Performance
6p6s configuration, V_{OUT}=17.5V, 150 mA, V_{IN}=3V, 0.3W power dissipation,
1.2 mm 6.8 µH inductor (DFE322512F-6R8M, ambient temperature 24°C
Maximum temperature is 38.3°C close to the LX and PGND pins of the package

Detailed Description

The ARC1C0608/ARC1C0605 uses a proprietary architecture with a charge pump driven by a synchronous boost converter to achieve very high peak efficiencies and superior efficiency over the single-cell lithium battery input voltage range. This architecture further realizes excellent performance across a range of LED forward voltages, allowing freedom in the selection of LEDs.

The ARC1C0608/ARC1C0605 supports 1 to 6 parallel LED strings. Unused LEDx pins should be tied to ground. This provides maximum design flexibility for wide variety of LCD screens.

The ARC1C0608/ARC1C0605 supports both I²C and non-I²C operation. It can be configured through I²C interface or external settings and allows combined I²C command settings with the PWM signal (CABC function) to adjust LED brightness.

The ARC1C0608/ARC1C0605 provides a full set of protection features to guarantee robust system operation, which include input battery voltage under-voltage lockout (UVLO), thermal shutdown (TSD), boost and charge pump over-current protection (OCP), boost and charge pump output over-voltage and under-voltage protection (OVP and UVP), and LED open and short detection.

Input Sequencing Requirements

VDDIO determines if the device starts up in I²C or non-I²C mode. This input can be applied before or after V_{IN} or EN, but it should be taken high (for I²C mode) or low (for non-I²C mode) before both V_{IN} and EN are asserted. VDDIO should not be left floating. In I²C mode the first command can be given at least 350 µs after both V_{IN} and EN are asserted.

If the part is enabled in non-I²C mode, VDDIO needs to be connected to the GND plane with a low inductance trace. In I²C mode, VDDIO can vary within its allowable voltage range. If this voltage drops too low, I²C communication will stop; however, the device will retain all its register values. I²C communication can resume 5 µs after VDDIO becomes stable within its allowable voltage range.

In I²C mode, SCL and SDA serve as clock and data lines. In non-I²C mode, connect SCL and SDA to AGND.

Charge Pump Ratio

The ARC1C0608/ARC1C0605 supports 1 to 6 parallel LED strings of 4-series to 9-series LEDs, depending on the LED forward voltages and the charge pump ratio selected. For most typical backlight applications, it is recommended that a 2x charge pump ratio is selected for LED strings with 4-series or 5-series LEDs. For 6-series LEDs and up to 9-series LEDs, a 3x charge pump ratio is recommended to achieve highest efficiency and to avoid VX over-voltage fault.

Selecting the charge pump ratio depends on whether the ARC1C0608/ARC1C0605 is operating with an I²C interface or not. When operating with an I²C interface, the charge pump ratio is set by the register bit MODE_2X. When MODE_2X = 0, the charge pump ratio is 3x and the output voltage of the boost converter is multiplied by 3 to the V_{OUT} output voltage. Conversely, when MODE_2X = 1, the charge pump ratio is 2x and the output voltage of the boost converter is multiplied by 2 to the V_{OUT} output voltage. Furthermore, the required external component and pin connections are different for each MODE_2X setting. Refer to application circuit Figure 6 where MODE_2X=0 and application circuit Figure 7 where MODE_2X=1.

The MODE_2X register bit is only read when LED channels enable, and the resulting charge pump ratio selection is locked in until all the LED channels disable. This means that changes to MODE_2X are ignored while the boost converter is in operation to prevent on-the-fly changes to the charge pump ratio.

In non-I²C mode, the ARC1C0608 is fixed at 3x charge pump ratio and ARC1C0605 is fixed at 2x charge pump ratio.

V_{IN} Under-Voltage Lockout (UVLO)

ARC1C0608/ARC1C0605 provides continuous monitoring of the V_{IN} input. When V_{IN} voltage drops below approximately 2.3V, the ARC1C0608/ARC1C0605 immediately shuts down.

Thermal Shutdown

The thermal shutdown protection circuit turns off the switching converter and LED current sinks when the IC junction temperature exceeds 150°C. The TSD bit in the STATUS1 register will be set. The switching converter and LED current sinks automatically restart when the IC junction temperature drops below the thermal hysteresis threshold.

Output Over-Voltage and Under-Voltage Protection

The ARC1C0608/ARC1C0605 protects against excessive output voltage by initiating over-voltage protection (VOUT_OVP) when V_{OUT} rises above the over-voltage threshold VOUT_OVP. When a V_{OUT} OVP occurs, the VOUT_OVP bit of the STATUS2 register is updated to a 1, and the ARC1C0608/ARC1C0605 turns off the boost converter. The boost converter automatically restarts after an OVP event when V_{OUT} decreases below the over-voltage threshold plus 0.5V typical hysteresis.

The over-voltage threshold can be configured through OVP_TH[1:0] bits in COMMAND register. The accuracy of each over-voltage threshold is +/-5%.

Table 7. Over-voltage Protection Thresholds

OVP_TH[1:0]	V_{OUT} Over-Voltage Threshold (V)
00	31.4
01	24
10	20
11	16

In non-I²C mode, the OVP threshold is fixed at 31.4V for ARC1C0608 and 20V for ARC1C0605.

The user should select the output over-voltage threshold with enough voltage margin above the highest expected operating V_{OUT} voltage in the application to guarantee proper LED open or grounded string fault detection. The highest expected operating V_{OUT} voltage is a function of the number of series LEDs used, the highest LED forward voltage expected and the regulation voltage at the LED pins during the maximum LED current used in the application per channel. When the MODE2X register bit is set or 2x charge pump ratio is selected, it is recommended that the user set the OVP_TH[1:0] = 10 for 20V over-voltage threshold to prevent exceeding the voltage rating on the VX pin.

Reset and Standby Functions

Details in Table 8 explain all RESET and standby states when the part uses the I²C interface.

For all modes: UVLO high = POR IC (entire chip shutdown).

Table 8. Reset and Standby States for UVLO High and PORC (Entire Chip Shutdown)

EN Pin Logic Level	Standby Bit	LEDEN[6:1] Bits	Reset Bit	Device Status	Device Circuit Block Status	I²C Registers
0	-	-	-	OFF	None	Cleared
1	0	0	0	Ready	References ON; boost/CP off; LED drivers on standby.	I²C accessible
1	0	>0	0	ON	All ON	I²C accessible
1	1	-	-	Standby	All off except UVLO + critical reference circuits	I²C accessible
1	0	-	1 (self-clearing)	Reset -> Ready (self-clearing)	Ready state after self-clearing reset	Cleared
Note: "-Denotes level can be either high or low and does not affect operation.						

Boost Output Over-voltage and Under-voltage Protection

The ARC1C0608/ARC1C0605 monitors the boost output (VX) voltage by initiating over-voltage protection (VX_OV) when VX rises above the VX over-voltage threshold. When a VX OV occurs, the VX_OV bit of the STATUS1 register is updated to a 1, and the ARC1C0608/ARC1C0605 turns off the boost converter. The boost converter automatically restarts after a VX_OV event when VX decreases below the VX_OV threshold.

If the boost output voltage (VX) falls below VX under-voltage (VX_UV) threshold, after the LED current sinks have turned on, the ARC1C0608/ARC1C0605 will shut down the switching converter and the LED current sinks immediately and register bit VX_UV in the STATUS1 register is set to 1. The switching converter and the LED current sinks remain latched off and will not start unless the part is shutdown or reset as explained in the table above.

The ARC1C0608/ARC1C0605 can detect a missing or unconnected inductor upon startup by monitoring the boost output prior to enabling the switching converter and LED strings. When an inductor open is detected, the VX_UV bit in the STATUS1 register will be set and is cleared upon read.

Soft-start Time-out

The ARC1C0608/ARC1C0605 implements a soft-start time-out fault. If the output voltage does not achieve regulation within 10 ms after startup, the switching converter and LED current sinks are disabled. The SS_TIMEOUT bits in the STATUS1 register will be set. The switching converter and LED current sinks remain latched off and will not restart unless the part is shutdown or reset.

Charge Pump Flying Capacitor Over-voltage

The ARC1C0608/ARC1C0605 monitors the flying capacitor voltage relative to the output voltage. In 2x charge pump ratio, when the voltage between the flying capacitor pins C1B (must be externally shorted to C2A), C2B (must be externally shorted to C1A) and V_{OUT} exceed 13.4V typical, the switching converter and the LED current sinks are disabled immediately. The CAP_OVP bit of STATUS1 register is set to 1. The ARC1C0608/ARC1C0605 will not restart until a reset event occurs, for example, by toggling EN low or setting the RESET bit in the COMMAND register.

In 3x charge pump ratio, when the voltage between the flying capacitor pins C1B, C2B and V_{OUT} exceeds 13.4V typical, the switching converter and the LED current sinks are disabled immediately. The CAP_OVP bit of STATUS1 register is set to 1. The ARC1C0608 will not restart until a reset event occurs, for example, by toggling EN low or setting the RESET bit in the COMMAND register.

LED Short Protection

The ARC1C0608/ARC1C0605 includes a fault comparator on each LEDx pin to detect a shorted LED condition. This comparator detects when the LEDx voltage rises above 6.2V typical, indicating a shorted LED fault. This fault condition may occur when some LEDs in a string are electrically bypassed making that LED string shorter than the other LED strings. The reduced forward voltage causes the current sink attached to that string to have a higher voltage on the LEDx pin than other current sinks, which could cause over-heating of that current sink. When this fault is detected, the faulty current sink is disabled, and an LED_SHORT fault is recorded in the STATUS2 register. The faulty current sink can only be re-enabled by turning off all LED current sinks first, or if a reset event occurs.

LED Open Circuit Protection

When one of the enabled LED strings is open, the output voltage V_{OUT} will rise until it crosses the VOUT_OVP threshold. Any string whose LED pin is below the regulation point is subsequently blocked from controlling V_{OUT}. This causes the output voltage V_{OUT} to decrease, and it is now controlled by the non-open string with the lowest LED pin voltage. An LED_OPEN fault is recorded in STATUS2 register.

If the open LED string is re-connected, the LED current sink will re-establish current to the level it is able based on the output voltage, but it will not be allowed to control the output voltage. The LEDEN[n] corresponding to the string with the LED_OPEN fault needs to toggled low first, and then re-enabled to re-establish output voltage control for that string.

Over-current and Short Circuit Protection

The boost converter has a cycle-by-cycle over-current limit of 2.9A typically but starts up initially with a derated over-current limit of 1.3A typically for soft-start. The boost low-side switch turns off when the inductor current reaches the current limit threshold and remains off until the beginning of the next switching cycle. This fault is not reported in the STATUS1 or STATUS2 registers.

For more severe over-current faults where the cycle-by-cycle over-current limit cannot prevent the inductor current from continuing to ratchet up, a secondary over-current protection is implemented. When the inductor current through the boost low-side switch exceeds 4.8A, the converter and the LED current sinks are disabled immediately. The BST_ILIM_SEC bit in the STATUS1 register will be set and is cleared upon read. The switching converter and LED current sinks remain latched off and will not restart unless the part is shutdown or reset.

A separate short-circuit detection is implemented where if the V_{OUT} pin is shorted to GND, the LED current sinks are disabled, and the output is disconnected from the charge-pump. The DISC_OCP bit in the STATUS1 register will be set.

STATUS1 and STATUS2 Registers

The STATUS1 and STATUS2 register bits are all cleared upon read, so repeated read-back of a logic-high fault bit indicates the fault event remains persistent. The LED_OPEN and LED_SHORT bits of the STATUS2 register require the faulted string's LEDEN[n] or all enabled LEDEN[n] to be reset low, and then the bits to be read for them to be cleared.

Current Setting

In I^2C mode, the maximum current of the LED outputs is set by the MAX_I[1:0] register bits in the ILED_CONFIG register. The default maximum current is 25 mA per LED string with 3 further settings available: 20 mA, 15 mA and 10 mA.

In non-I^2C mode, the maximum current can be adjusted by an external resistor, RISET connected between the ISET pin and GND. RISET controls the full scale per-channel LED current as follows:

$$I_{LED\_FULL} = \frac{0.4}{R_{ISET}} * K_{ISET},\ where\ K_{ISET} = 1562.5$$

The RISET range is between 24.9KΩ to 250 KΩ. In PWM mode, the per-channel LED current output can be calculated from the duty cycle of the PWM input as follows:

$$I_{LED} = \frac{0.4}{R_{ISET}} * K_{ISET} * PWM\ Duty\ Cycle$$

Boost Converter Switching Frequency

In I²C mode, the ARC1C0608/ARC1C0605 boost converter provides wide frequency selection to meet different users' requirements. Five bits are used to set the boost switching frequency, which are the FSW_BOOST[4:0] bits in the CONFIG register. See Table 9.

Table 9. Boost Converter and Boost Switching Frequency

Frequency (Khz)	FSW_BOOST[4:0]	Frequency (Khz)	FSW_BOOST[4:0]
Reserved	0x00	602	0x10
Reserved	0x01	569	0x11
3413	0x02	539	0x12
2560	0x03	512	0x13
2048	0x04	488	0x14
1707	0x05	465	0x15
1463	0x06	445	0x16
1280	0x07	427	0x17
1138	0x08	410	0x18
1024	0x09	394	0x19
931	0x0A	379	0x1A
853	0x0B	366	0x1B
788	0x0C	353	0x1C
731	0x0D	341	0x1D
683	0x0E	330	0x1E
640	0x0F	320	0x1F

In non-I²C mode, the boost switching frequency is set by the FSET pin, which is sampled once at startup. Changing the FSET pin bias after boost switching has started will not change the boost switching frequency. Table 10 shows the boost switching frequency settings through I²C register value. It also shows how FSET determines the boost frequency in non-I²C mode.

The choice of inductor, charge pump fly capacitors and compensation components is dependent on the selected boost switching frequency for proper part operation. Contact pSemi for recommended component types and values.

Table 10. Boost Frequency in non I²C Mode and Boost Switching Frequency through I²C Register Value

Non-I²C Interface: Fset Pin Bias	Boost Switching Frequency
FSET shorted to V_{IN}	2560 KHz
FSET open	1024 KHz
FSET shorted to GND	512 KHz

Charge Pump Switching Frequency

The charge pump switching frequency is set as a ratio of the boost switching frequency. The ratio is programmable to 1/8, 1/4 or 1/2 using register bits CP_FREQ[1:0] in CONFIG register via I²C. The 1/8 charge pump switching frequency ratio provides higher overall efficiency but the maximum total output current supported is limited to 75 mA, which translates to 18.75 mA maximum per-channel LED current for a 4-channel display. The 1/4 charge pump ratio supports a maximum total output current of 112.5 mA, and 1/2 charge pump ratio can support the maximum 150 mA or 25 mA maximum per-channel LED current for a 6-channel display.

For I²C operation, the charge pump switching frequency ratio default setting is 1/4. For non-I²C operation, the charge pump switching frequency ratio default setting is 1/8. Contact Murata for alternate factory configuration options.

Switching Converter Compensation

The switching converter operates in voltage-mode control and uses external compensation. Type-III compensation is recommended which requires three components as shown in Figure 16.

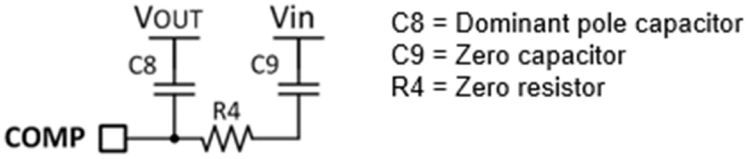


Figure 16. Compensation Components

Contact pSemi for compensation recommendations for your application.

LED Current Output Dimming

The ARC1C0608/ARC1C0605 supports three LED current output dimming options in I²C mode for maximum application flexibility in choosing among low noise, converter efficiency, optical efficiency and minimal WLED color shift at low brightness levels. These options are analog, phase shift PWM, and hybrid PWM (mixed-mode). In non-I²C mode, only the analog output dimming option is used.

Analog Dimming

In I²C mode, when ILED_CONFIG register bit 6, DIM_MODE, is set to 0, dimming is set to analog only. In analog dimming, the LED current sink output is always a dc current across the entire brightness range. As brightness is reduced, the LED current sink output dc level decreases which also decreases the LED forward voltage. The adaptive output voltage regulation loop decreases the V_{OUT} voltage at the top of the LED strings, which can also reduce power dissipation in the switching converter. Operating the LEDs with a dc current output also minimizes noise in the system. When using a non-I²C interface, the full-scale output current per channel can be scaled using an external resistor, R_{ISET}, connected between the ISET pin and GND. The tolerance of the external resistor R_{ISET} directly affects the accuracy of the LED current sink output, so using a precision resistor is recommended. The recommended R_{ISET} resistor range is 24.9kΩ to 250kΩ, with 24.9kΩ corresponding to a 25 mA full-scale current output per channel.

Phase Shift PWM Dimming

In I²C mode, when ILED_CONFIG register bit 6, DIM_MODE, is set to 1, dimming is set to mixed-mode dimming. Under this mode, the mixed-mode dimming block generates phase shifted PWM signals to dim active LED strings when the required LED current is below the threshold set by the PWM_IX[1:0] register bits. The phase difference between active strings is automatically adjusted to 360 degrees divided by the number of active strings. This phase shifting reduces noise in the audio band.

Since the input code is a 12-bit value, the PWM generator uses the 8 bits of the WLED_ISET_MSB register 0x08 for the msb portion mapped as bits WLED_ISET[11:4], and the upper nibble of WLED_ISET_LSB register 0x07 for the lsb portion mapped as bits WLED_ISET[3:0] in the 12-bit value.

Depending on the PWM frequency selected, the lower bits are truncated. Figure 17 shows how the register bits are used and the corresponding relationship between frequency and resolution during phase shift PWM dimming.

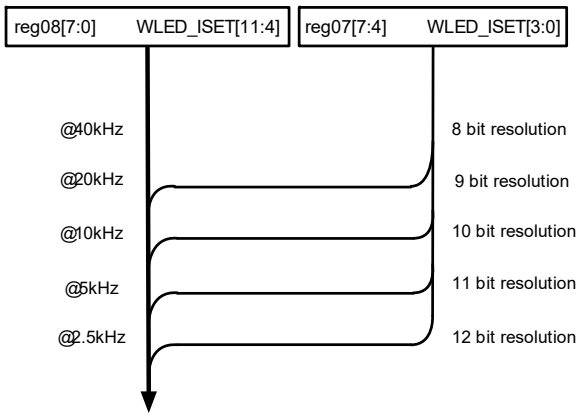


Figure 17. Relationship Between Frequency and Resolution in Phase Shift PWM Dimming

The LED intensity is updated at the start of every LED output PWM cycle with the frequency set by the PWM_DIM_FREQ[2:0] bits.

Note that since the on-chip clock is 10.24MHz, an 11-bit dimming resolution can only be implemented with a 5 KHz PWM input signal or lower (10.24MHz/211 = 5KHz). Higher PWM input frequencies will have reduced dimming resolution, with 8 bits of dimming resolution available at 40 KHz.

The same resolution limitation occurs with the PWM output frequency. This effect is most pronounced with 100% PWM dimming (PWM_IX[1:0]=11). When 25% PWM dimming (PWM_IX[1:0]=01) is used, a 40 KHz PWM output frequency provides 10 bits of dimming resolution relative to the full-scale LED output current (10.24MHz/210/25% = 40KHz).

If the PWM frequency is set at 40 KHz, only the WLED_ISET_MSB register at address 0x08 is considered.

Hybrid PWM (Mixed-Mode) Dimming

The ARC1C0608/ARC1C0605 allows a mixed-mode dimming scheme for better optical efficiency. The transition point from analog to phase shift PWM dimming is set by register bits DIM_MODE and PWM IX[1:0], and can be 12.5%, 25%, 50% or 100% of the brightness range. 100% means PWM dimming is used across the whole brightness range. In the brightness range above the switch point, analog dimming is adopted and below the transition point, phase shift PWM dimming is adopted. With this arrangement, good optical efficiency at low brightness levels is achieved.

PWM_IX[1:0]=11 results in a LED dc output current only when the LED brightness setting is at 100%; otherwise, each LED current sink switches off and on to 100% of its full-scale output level.

PWM_IX[1:0]=10 results in a LED dc output current only when the LED brightness setting is at 50% or greater; otherwise, each LED current sink switches off and on to 50% of its full-scale output level

.PWM_IX[1:0]=01 results in a LED dc output current only when the LED brightness setting is at 25% or greater; otherwise, each LED current sink switches off and on to 25% of its full-scale output level.

PWM_IX[1:0]=00 results in a LED dc output current only when the LED brightness setting is at 12.5% or greater; otherwise, each LED current sink switches off and on to 12.5% of its full-scale output level

An example of the LED current output for any one channel at the PWM_IX[1:0]=01 setting is shown in Figure 18.

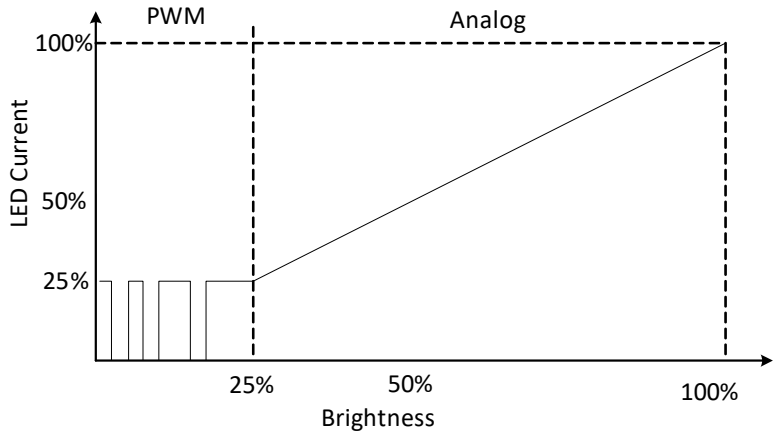


Figure 18. Mixed-Mode Dimming Control with PWM_IX[1:0]=01 for 25% Transition Point

The choice of four brightness transition points between analog dimming and phase shift PWM dimming at the LED current sink output provides flexibility in optimizing between good optical efficiency and good matching of the LED brightness and color shift. Since the LED current output peak during phase shift PWM dimming scales proportionally with the brightness transition point, the LED current pulse width also has to scale inversely for a given brightness setting. For example, at a 10% LED brightness setting, the LED current pulse width at PWM_IX[1:0]=01 (25% transition point) is four times longer than at PWM_IX[1:0]=11 (PWM-only dimming) to get an equivalent output brightness. The minimum controllable LED current on pulse or off pulse is 200 ns typically.

When the LED current outputs are operating in phase shift PWM dimming, their switching frequency can be selected from one of 5 frequency settings between 2.5 KHz and 40 KHz using the PWM_DIM_FREQ[2:0] register bits.

LED Current Full-Scale or 100% Brightness

The maximum LED current full-scale is programmed using MAX_I[1:0] bits in I²C mode or an external resistor in non-I²C mode, both of which provide for fine tuning.

LED Brightness Control

The LED brightness is controlled by the duty cycle of the PWM input signal, the WLED_ISET[11:0] bits written via the I²C interface, or both for CABC function. The register bits DIMCODE[1:0] select the following dimming schemes:

A. DIMCODE[1:0]=00

When DIMCODE[1:0]=00, the LED current is controlled by the PWM input duty cycle. The PWM detector block extracts the duty cycle of the PWM input signal. The duty cycle goes through a mapping to generate the brightness code. The resulting code goes into the mixed dimming block to generate a DC current level or six phase-shifted PWM signals at the LED strings. See Figure 19.

In non-I²C mode, the LED brightness is controlled by the PWM input duty cycle only, with the full-scale current set by the resistor on the ISET pin.

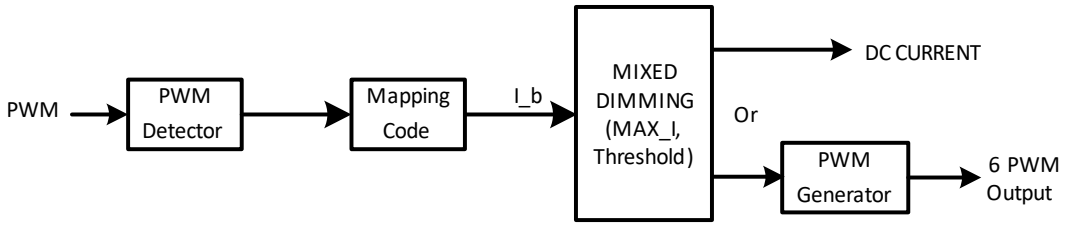


Figure 19. DIMCODE[1:0]=00

DIMCODE[1:0]=01

When DIMCODE[1:0]=01, the LED current is controlled by the WLED_ISET[11:0] register bits via I²C. The register codes go through a mapping first, then through the mixed dimming block to generate a DC current level or six phase-shifted PWM signals at the LED strings. See Figure 20.

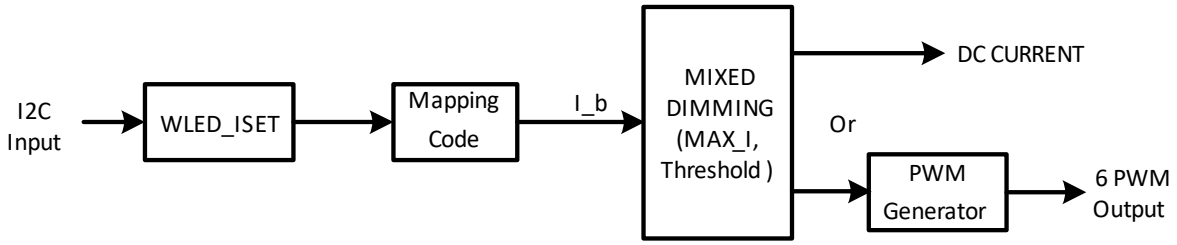


Figure 20. DIMCODE[1:0]=01

B. DIMCODE[1:0]=10 (CABC function)

When DIMCODE[1:0]=10, the LED current is controlled by both the PWM input duty cycle and the WLED_ISET[11:0] register bits via I²C. The WLED_ISET[11:0] bits are multiplied by the PWM-based brightness code. After multiplication, the resulting code goes into the dimming block to generate a DC current or six phase-shifted PWM signals at the LED strings. See Figure 21.

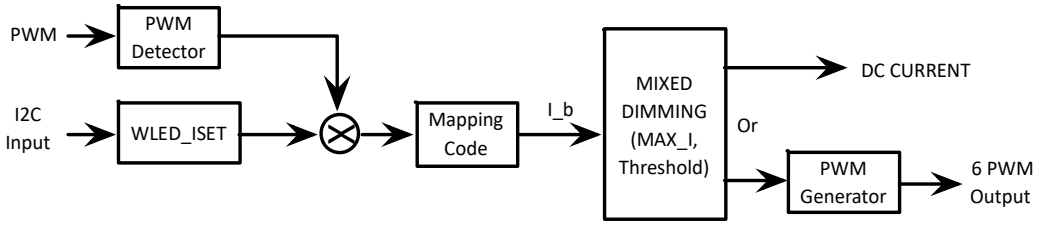


Figure 21. DIMCODE[1:0]=10

Linear and Logarithmic Mapping

In linear mapping mode, the dimming settings presented either via the PWM input duty cycle or WLED_ISET[11:0] bits are translated linearly into the LED current. This is the default setting.

For a better visual experience, ARC1C0608/ARC1C0605 can also translate the dimming settings via a logarithmic mapping to produce the LED current. The user can set the LOG_MODE bit to 1 in the ILED_CONFIG register to enable this feature. There are only 1023 possible brightness states in this mode.

Operation with DIMCODE=00 or 10

In these modes, the ARC1C0608/ARC1C0605's PWM input frequency range is from 2.65 KHz to 40 KHz. The input frequency is independent of the PWM output frequency which is the six-phase LED current switching frequency. In I²C mode, the PWM output frequency is set by the PWM_DIM_FREQ register.

Fade In/Out Control

The fade in/out control makes a smooth transition from one brightness value to another for a better human eye experience. ARC1C0608/ARC1C0605 provides extensive selection of the time for brightness changes from one level to another. The fading speed is selected by the FADING_SPEED[7:0] bits in the WLED_FADING_CTRL register. This register can set the speed from 50us/step (0x01) to 12.75ms/step (0xFF) or disabled (0x00) based on user preference. See the register WLED_FADING_CTRL section for detailed description.

In non-I²C mode, FADING_SPEED[7:0] is set to 0x00 to give users full control via the PWM input.

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and managing device slave addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The ARC1C0608/ARC1C0605 operates as a slave and supports the following data transfer modes, as defined in the I²C -Bus specification: Standard mode (100 Kbps), fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the V_{IN} voltage remains above UVLO and the EN pin remains logic high.

The data transfer protocol for standard and fast modes is the same; therefore, they are referred to as F/S-mode in this document. The ARC1C0608/ARC1C0605 supports 7-bit addressing; 10-bit addressing, and general call address are not supported. The device 7-bit address is defined as '0110000' or 0x30.

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 22. All I²C-compatible devices should recognize a start condition.

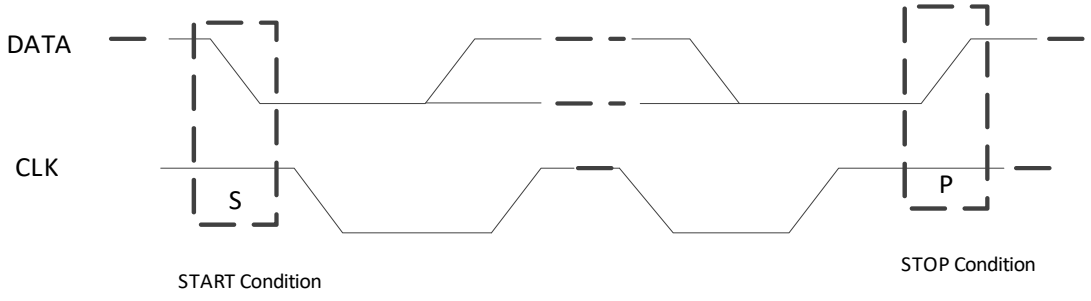


Figure 22. START and STOP Conditions

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse. See Figure 23. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that a communication link with a slave has been established. See Figure 24.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high. See Figure 25 on page 33. This releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in FFh being read out.

ARC1C0608/ARC1C0605 I²C Update Sequence

The ARC1C0608/ARC1C0605 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, ARC1C0608/ARC1C0605 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the ARC1C0608/ARC1C0605. The ARC1C0608/ARC1C0605 performs an update on the falling edge of the acknowledge signal that follows the LSB.

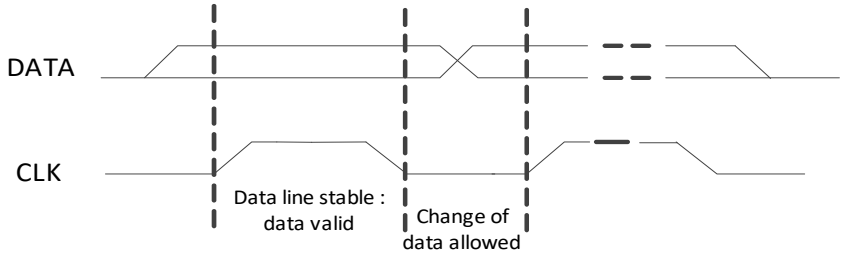


Figure 23. Bit Transfer on the Serial Interface

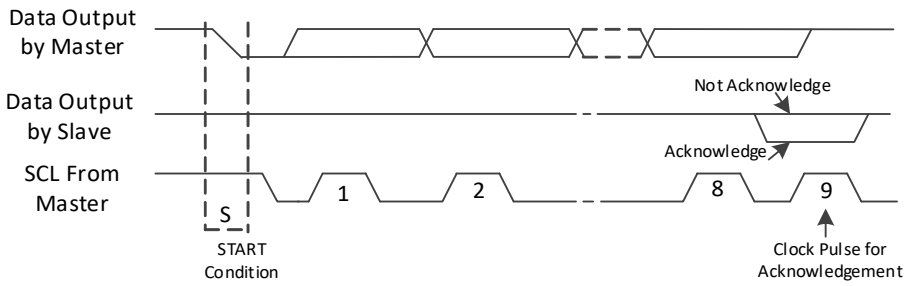


Figure 24. Acknowledge (ACK) on the I²C Bus

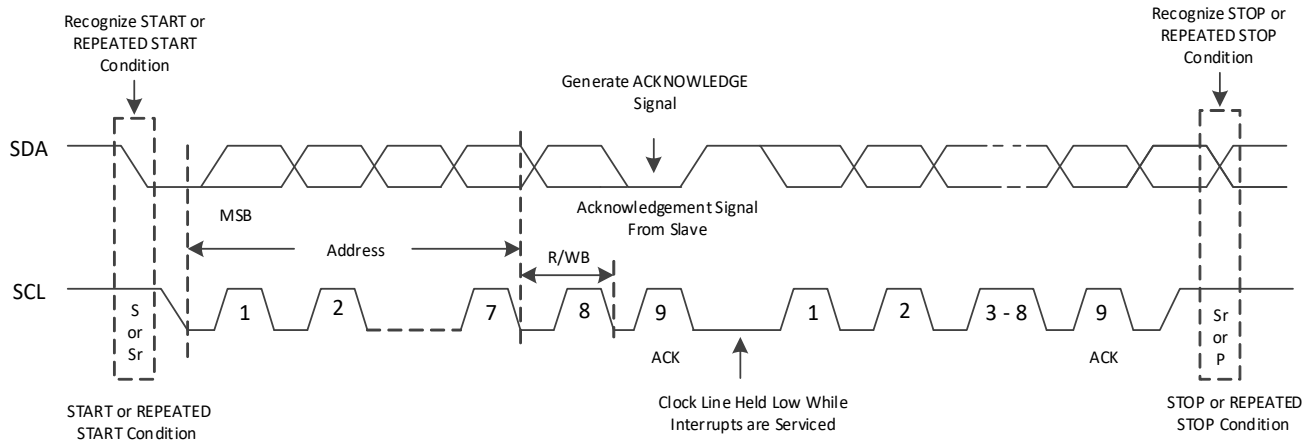


Figure 25. Bus Protocol

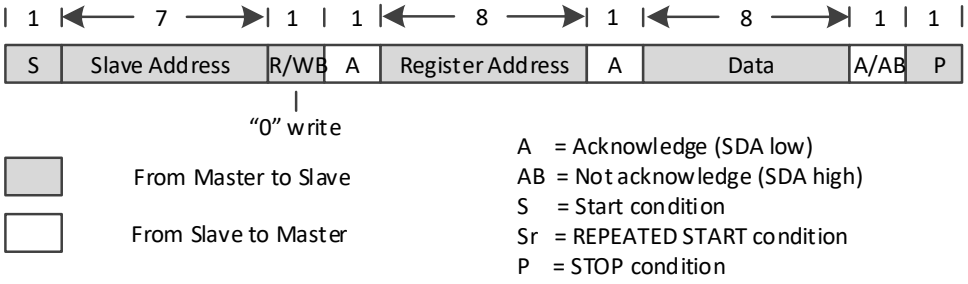


Figure 26. "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

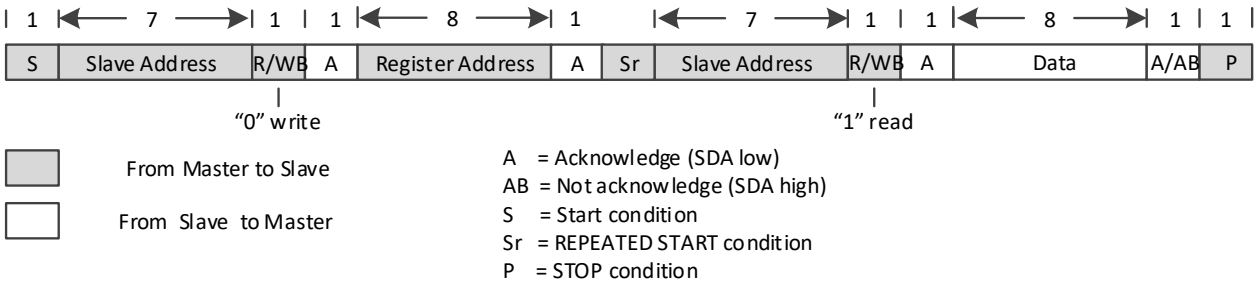


Figure 27. "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

Register Map

7-Bit Slave Address: 0x30

Register Configuration Parameters

Register	Addr	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	0x00	I2C_Standby	RESET	Reserved	Boost_ mode	OVP_TH[1:0]		MODE_2X	Reserved
CONFIG	0x01	Reserved	CP_FREQ[1:0]		FSW_BOOST[4:0]				
STATUS1	0x02	BST_ILIM_SEC	VOUT_UVP	VX_OV	VX_UV	CAP_ OVP	DISC_OCP	TSD	SS_TIMEOUT
STATUS2	0x03	VOUT_OVP	Reserved					LED_OPEN	LED_SHORT
WLED_ FADING_CTRL	0x04	FADING_SPEED [7:0]							
ILED_CONFIG	0x05	LOG_MODE	DIM_MODE	PWM_IX[1:0]		DIMCODE[1:0]		MAX_I[1:0]	
LEDEN	0x06	Reserved		LEDEN[6]	LEDEN[5]	LEDEN [4]	LEDEN[3]	LEDEN[2]	LEDEN[1]
WLED_ISET_ LSB	0x07	WLED_ISET[3:0]				Reserved			
WLED_ISET_ MSB	0x08	WLED_ISET[11:4]							
PWM_DIM_ FREQ	0x09	Reserved					PWM_DIM_FREQ[2:0]		

Detailed Register Description

Register COMMAND

Address	Name	POR Value
0x00	COMMAND	0x20

Bit Assignment

7	6	5	4	3	2	1	0
I2C_Standby	RESET	Reserved	Boost mode	OVP_TH[1]	OVP_TH[0]	MODE_2X	Reserved

Bit Description

Field Name	Bits	Type	POR	Description
I2C_Standby	[7]	R/W	0b	Low-power standby mode with I^2C interface and registers accessible.
RESET	[6]	R/W	0b	Write 1 to reset the device. This bit is self-clearing.
Reserved	[5]	R/W	1b	
Boost mode	[4]	R/W	0b	0 = DCM (discontinuous conduction mode) 1 = CCM (continuous conduction mode)
OVP_TH[1:0]	[3:2]	R/W	00b	00 = 31.4V; 01 = 24V; 10 = 20V; 11 = 16V
MODE_2X	[1]	R/W	0b	0 = 3x charge pump ratio 1 = 2x charge pump ratio
Reserved	[0]	R/W	0b	

Register CONFIG

Address	Name	POR Value
0x01	CONFIG	0x29

Bit Assignment

7	6	5	4	3	2	1	0
Reserved	CP_FREQ[1:0]		FSW_BOOST[4:0]				

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7]			
CP_FREQ[1:0]	[6:5]	R/W	01b	Charge pump frequency ratio 00 = 1/2 01 = 1/4 10 = 1/8 11 = Reserved
FSW_BOOST[4:0]	[4:0]	R/W	01001b	Boost switching frequency. See the Boost Converter Switching Frequency section for the full frequency chart. 11111 = 320 KHz 01111 = 640 KHz 01001 = 1.024 MHz (default) 00011 = 2.560 MHz 00010 = 3.413 MHz

Register STATUS1

Address	Name	POR Value
0x02	STATUS1	0x00

Bit Assignment

7	6	5	4	3	2	1	0
BST_ILIM_SEC	VOUT_UVP	VX_OV	VX_UV	CAP_OVP	DISC_OCP	TSD	SS_TIMEOUT

Bit Description

Field Name	Bits	Type	POR	Description
BST_ILIM_SEC	[7]	RO	0b	Boost secondary current limit
VOUT_UVP	[6]	RO	0b	V_{OUT} under-voltage
VX_OV	[5]	RO	0b	VX over-voltage
VX_UV	[4]	RO	0b	VX under-voltage
CAP_OVP	[3]	RO	0b	Charge pump over-voltage
DSC_OCP	[2]	RO	0b	Output over-current
TSD	[1]	RO	0b	Thermal shutdown
SS_TIMEOUT	[0]	RO	0b	Soft-start yimeout

Register STATUS2

Address	Name	POR Value
0x03	STATUS2	0x00

Bit Assignment

7	6	5	4	3	2	1	0
VOUT_OVP	Reserved					LED_OPEN	LED_SHORT

Bit Description

Field Name	Bits	Type	POR	Description
VOUT_OVP	[7]	RO	0b	V_{OUT} over-voltage
Reserved	[6:2]			
LED_OPEN	[1]	RO	0b	LED open or grounded
LED_SHORT	[0]	RO	0b	LED shorted string

Register WLED_FADING_CTRL

Address	Name	POR Value
0x04	WLED_FADING_CTRL	0x00

Bit Assignment

7	6	5	4	3	2	1	0
FADING_SPEED [7:0]							

Bit Description

Field Name	Bits	Type	POR	Description	Field Name
FADING_SPEED		[7:0]	R/W	0x00	Sets the fading counter from 50 µs to 12.75 ms in 50 µs steps. This is the period between each intensity step. 0x00 = Fading disabled 0x01 = 50 µs/step… 0xFF = 12.75 ms/step

Register ILED_CONFIGs

Address	Name	POR Value
0x05	ILED_CONFIG	0x53

Bit Assignment

7	6	5	4	3	2	1	0
LOG_MODE	DIM_MODE	PWM_IX[1]	PWM_IX[0]	DIMCODE[1]	DIMCODE[0]	MAX_I[1]	MAX_I[0]

Bit Description

Field Name	Bits	Type	POR	Description
LOG_MODE	[7]	R/W	0b	LED brightness control profile 0 = linear 1 = logarithmic
DIM_MODE	[6]	R/W	1b	LED current output dimming mode 0 = Analog dimming only 1 = Hybrid PWM dimming mode
PWM_IX[1:0]	[5:4]	R/W	01b	Hybrid PWM dimming transition point between PWM dimming and analog dimming 00 = 12.5% of full-scale current 01 = 25% of full-scale current (default) 10 = 50% of full-scale current 11 = 100% of full-scale current or PWM dimming only
DIMCODE[1:0]	[3:2]	R/W	00b	LED brightness control 00 = PWM input duty cycle dimming (default) 01 = WLED_ISET[11:0] 10 = Both PWM duty cycle and WLED_ISET[11:0] (CABC function) 11 = Reserved
MAX_I[1:0]	[1:0]	R/W	11b	WLED full-scale current (100% brightness). 00 = 10 mA 01 = 15 mA 10 = 20 mA 11 = 25 mA (default)

Register LEDEN

Address	Name	POR Value
0x06	LEDEN	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved		LEDEN[6]	LEDEN[5]	LEDEN[4]	LEDEN[3]	LEDEN[2]	LEDEN[1]

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:6]			
LEDENx	[5:0]	R/W	0x00	LED channel enable 0 = disable LED channel 1 = enable LED channel

Register WLED_ISET_LSB

Address	Name	POR Value
0x07	WLED_ISET_LSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[3:0]				Reserved			

Bit Description

Field Name	Bits	Type	POR	Description
WLED_ISET[3:0]	[7:4]	R/W	0x00	The LSB bits of the WLED_ISET[11:0] brightness code. If changing the LSB bits, these must be written before the MSB bits.
Reserved	[3:0]			

Register WLED_ISET_M SB

Address	Name	POR Value
0x08	WLED_ISET_MSB	0x00

Bit Assignment

7	6	5	4	3	2	1	0
WLED_ISET[11:4]							

Bit Description

Field Name	Bits	Type	POR	Description
WLED_ISET[11:4]	[7:0]	R/W	0x00	The MSB bits of the WLED_ISET[11:0] brightness code.

Register PWM_DIM_FREQ

Address	Name	POR Value
0x09	PWM_DIM_FREQ	0x09

Bit Assignment

7	6	5	4	3	2	1	0
Reserved					PWM_DIM_FREQ[2:0]		

Bit Description

Field Name	Bits	Type	POR	Description
Reserved	[7:3]			
PWM_DIM_FREQ[2:0]	[2:0]	R/W	001b	Hybrid dimming frequency 000 = 2.5 KHz 001 = 5 KHz(default) 010 = 10 KHz 011 = 20 KHz 100 = 40 KHz 101, …, 111 = reserved

Application Schematic

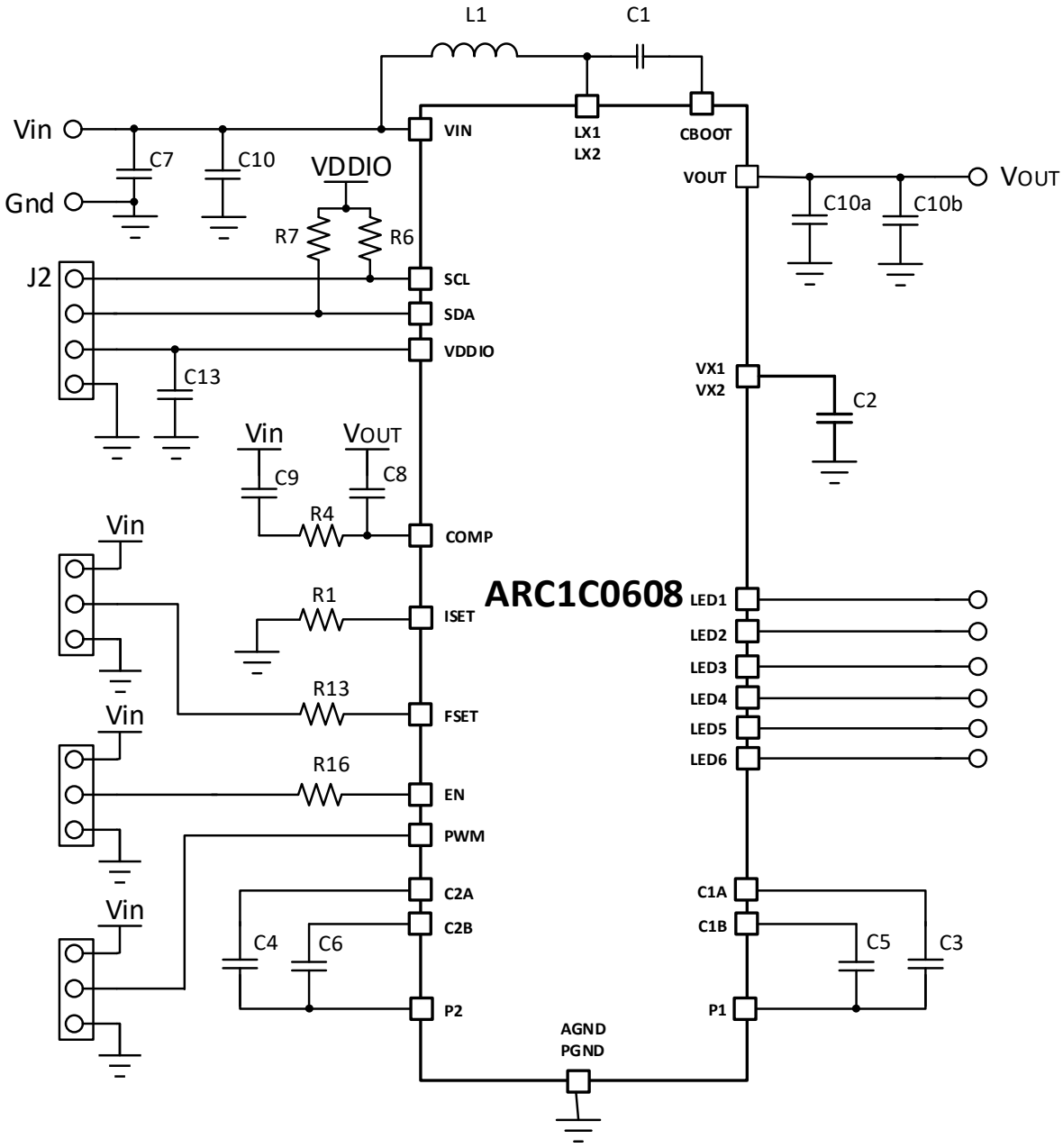


Figure 28. Detailed Application Schematic for 3x Charge Pump Ratio

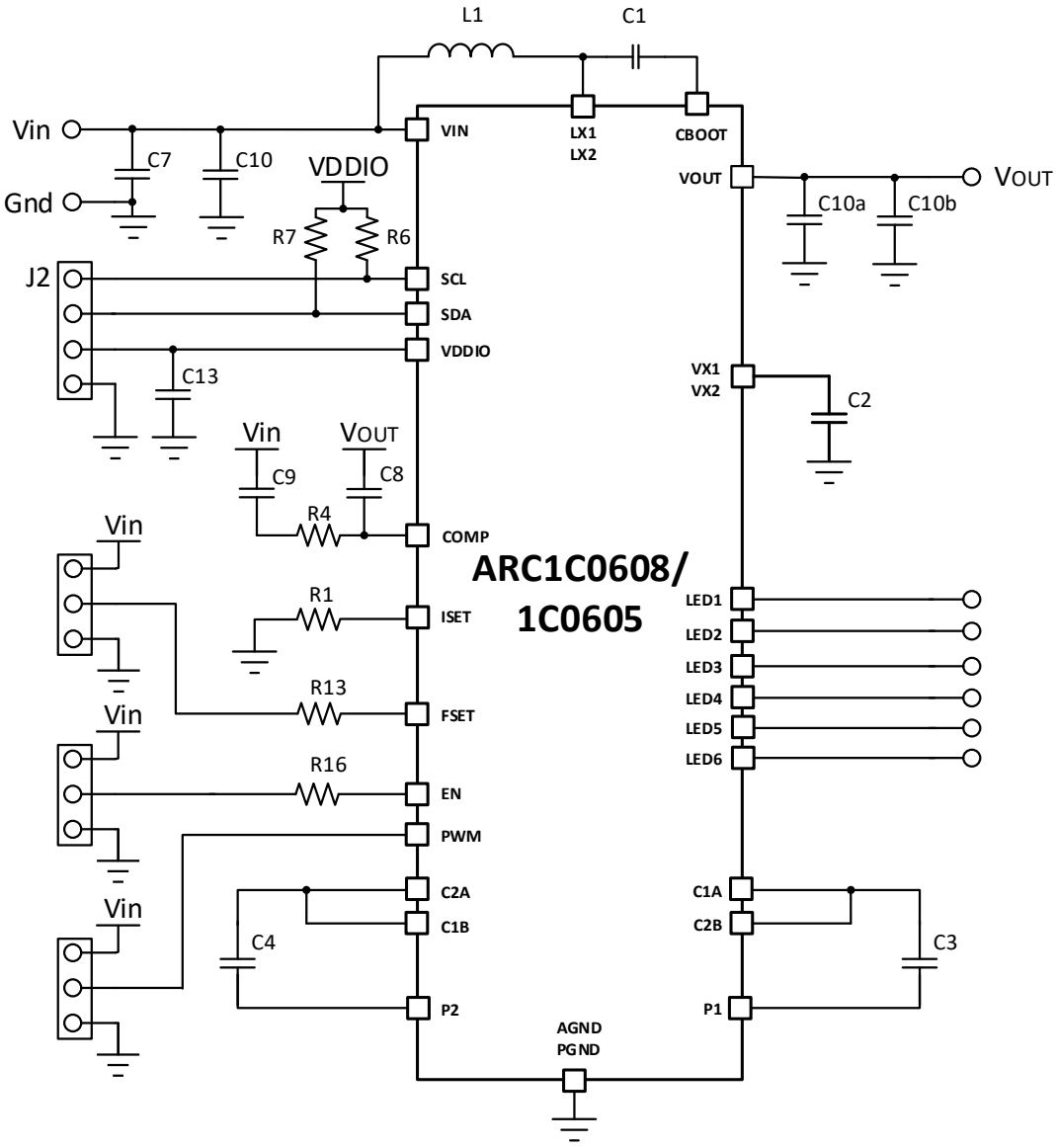


Figure 29. Detailed Application Schematic for 2x Charge Pump Ratio

Recommended BOM Lists

Table 11. Recommended BOM List for 3x Charge Pump Ratio (Figure 28)

Component Name	Value	Part Size (Imperial Unless Otherwise Specified)	Manufacturer's Part Number
C1	22 nF 50V X7R	0402	GRM155R71H223KA12D
C2	470 nF 25V X5R	0402	GRM155R61E474KE01
C3	2.2 µF 16V X5R	0603	GRM188R61C225KAAD
C4	2.2 µF 16V X5R	0603	GRM188R61C225KAAD
C5	4.7 µF 35V X5R	0603	GRM188R6YA475KE15
C6	4.7 µF 35V X5R	0603	GRM188R6YA475KE15
C7 (1)	1.0 µF 16V X5R	0603	GRM188R61C105KA12D
C8	47 pF 50V C0G	0201	GRM0335C1H470JA01
C9	15 nF X5R	0201	GRM033R61C153KE84D
C10a. C10b	4.7 µF 35V	0603	GRM188R6YA475KE15
L1	6.8 µH 1.2 mm max height	3.2 mm × 2.5 mm	DFE322512F-6R8M
R4	20k Ohms	0201	Generic
U1	ARC1C0608	WLCSP-35	ARC1C06081W

Table 12. Recommended BOM List for 2x Charge Pump Ratio (Figure 29)

Component Name	Value	Part Size (Imperial Unless Otherwise Specified)	Manufacturer's Part Number
C1	22 nF 50V X7R	0402	GRM155R71H223KA12D
C2	470 nF 25V X5R	0402	GRM155R61E474KE01
C3	4.7 µF 35V X5R	0603	GRM188R6YA475KE15
C4	4.7 µF 35V X5R	0603	GRM188R6YA475KE15
C7 (1)	1.0 µF 16V X5R	0603	GRM188R61C105KA12D
C8	47 pF 50V C0G	0201	GRM0335C1H470JA01
C9	15 nF X5R	0201	GRM033R61C153KE84D
C10a. C10b	4.7 µF 35V	0603	GRM188R6YA475KE15
L1	6.8 µH 1.2mm max height	3.2 mm x 2.5 mm	DFE322512F-6R8M
R4	20k Ohms	0201	Generic
U1	ARC1C0605	WLCSP-35	ARC1C06051W

Component Selection

Users of the ARC1C0608/ARC1C0605 should adhere closely to the parts selected for the recommended BOM list. Component selection is a complex process and several of the parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact pSemi for guidance.

Layout Example

An example of a compact 6 WLED string multi-stage converter layout with solution size ~72mm2. is shown in Figure 30. Figure 31 to Figure 34 show individual layers.

Figure 30. Layout Example

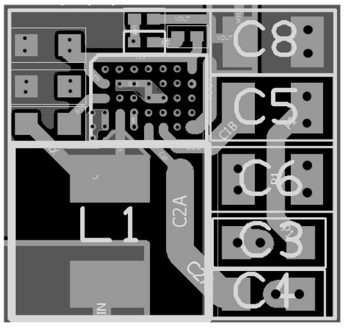


Figure 31. Top Layer

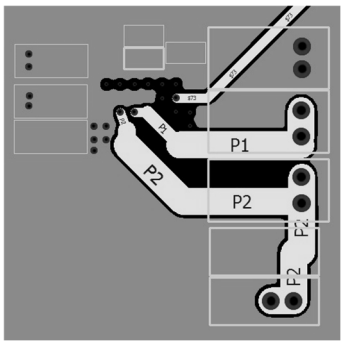


Figure 32. Layer 3

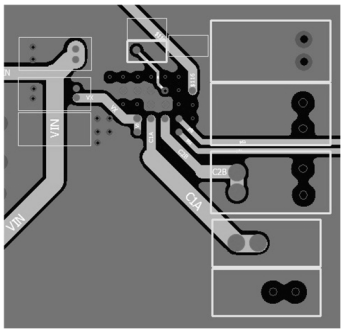


Figure 33. Layer 2

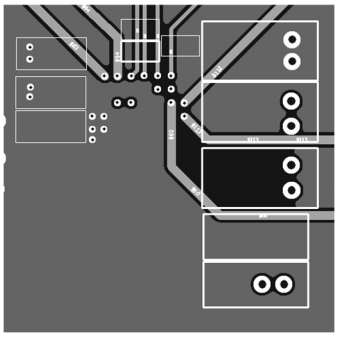


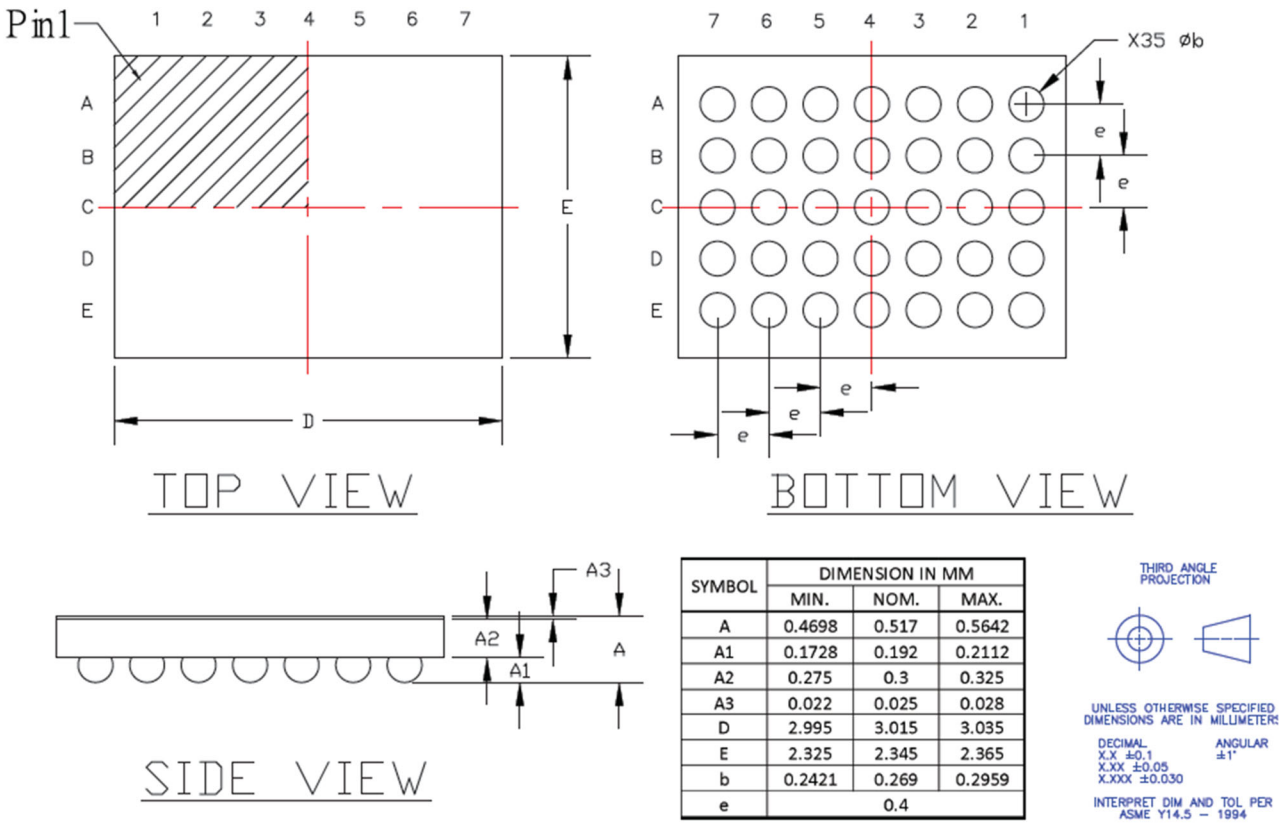
Figure 34. Bottom Layer

Mechanical Details

Package mechanical details are given in this section.

Device Dimension

Device dimensions are shown in Figure 35.

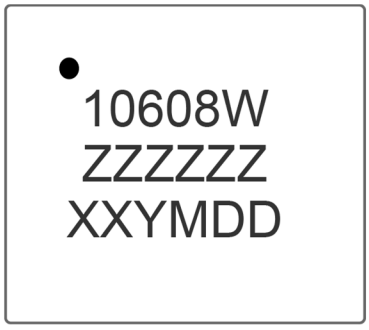


SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.4698	0.517	0.5642
A1	0.1728	0.192	0.2112
A2	0.275	0.3	0.325
A3	0.022	0.025	0.028
D	2.995	3.015	3.035
E	2.325	2.345	2.365
b	0.2421	0.269	0.2959
e		0.4	

Figure 35. Package Mechanical Dimension

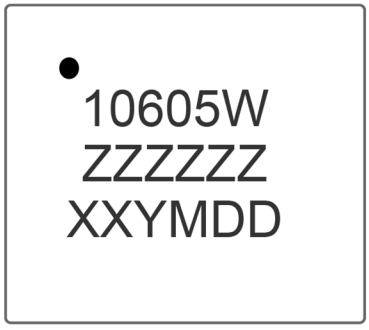
Device Marking

Details of device marking for ARC1C0608 are given in Figure 36 and device marking for ARC1C0605 are given in Figure 37.



● = Pin 1 indicator
10608W = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
XX = Supplier code (maximum two characters)
Y = Last digit of assembly year (2022 = 2)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

Figure 36. ARC1C0608 Device Marking



● = Pin 1 indicator
10605W = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
XX = Supplier code (maximum two characters)
Y = Last digit of assembly year (2022 = 2)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

Figure 37. ARC1C0605 Device Marking

Guidelines for PCB Land Design

PCB land design details are given in this section.

Recommended PCB Pad and Stencil Parameters

The recommended dimensions of the PCB pad and stencil parameters are shown in Figure 38.

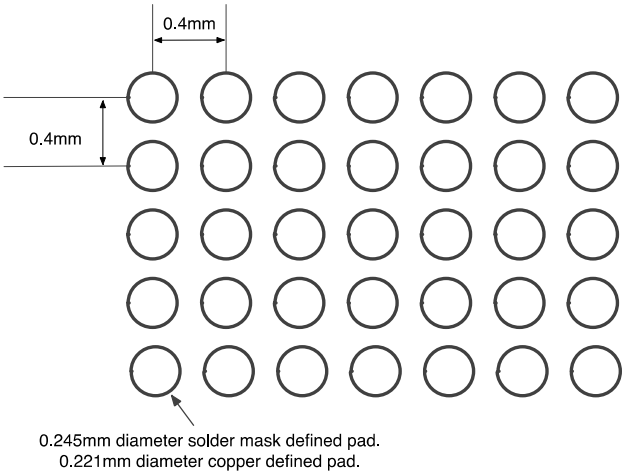
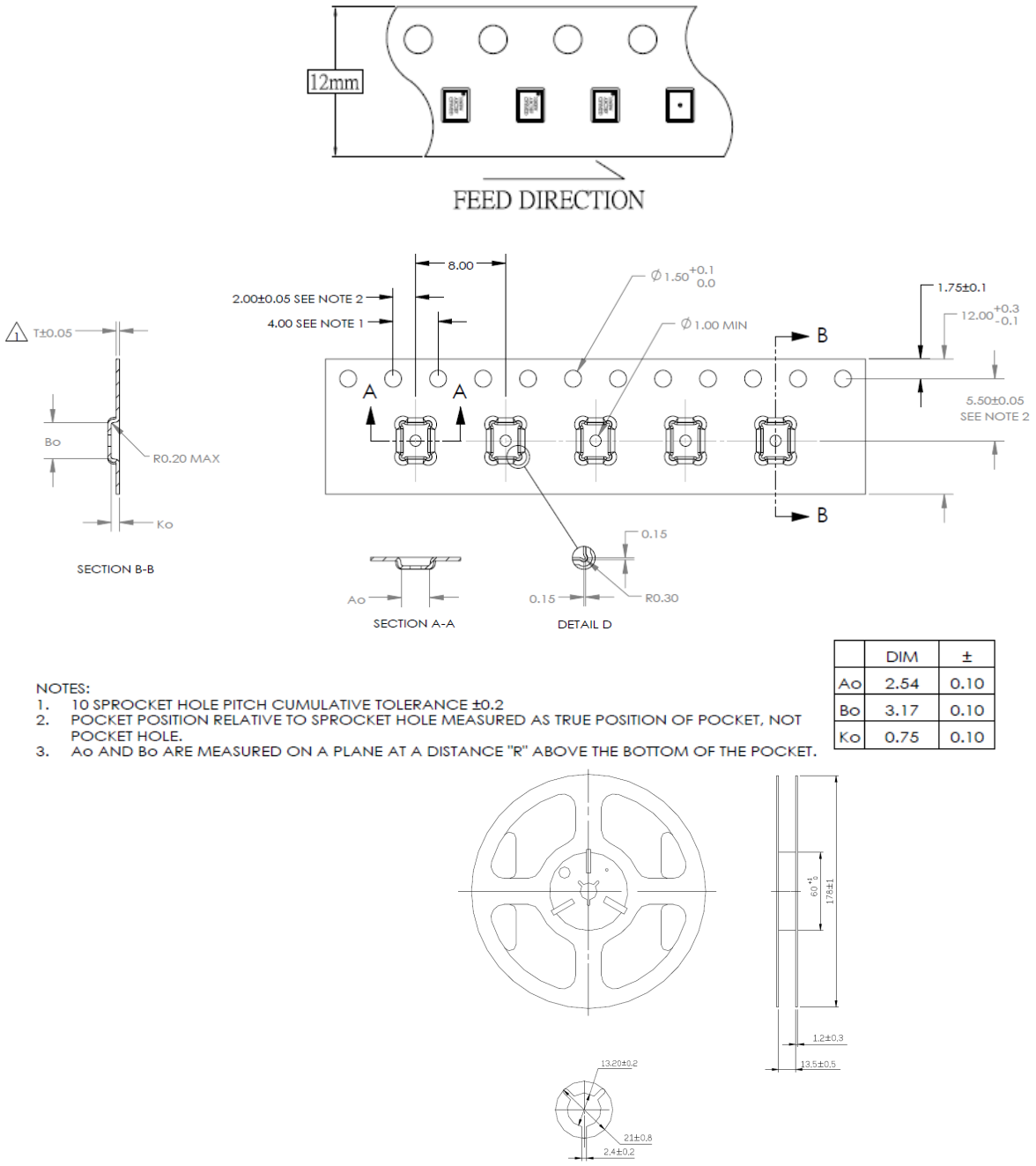


Figure 38. Bottom View and Dimensions

Tape and Reel Information



	DIM	±
Ao	2.54	0.10
Bo	3.17	0.10
Ko	0.75	0.10

Figure 39. Tape and Reel Information

Ordering Information

Information for ordering the ARC1C0608 and ARC1C0605 devices is available in the following table.

Table 13. Order Codes

Ta	Package	Non-I²C Mode Charge Pump Ratio Setting	Orderable Device Number	Pins	Transport Media	Minimum Order Quantity
-40....+85°C	WLCSP	3x	ARC1C06081W-R	35	Large tape-and-reel	5000
			ARC1C06081W-V		Small tape-and-reel	250
			ARC1C06081W-G		Sample waffle tray	10
		2x	ARC1C06051W-R[1]		Large tape-and-reel	5000
			ARC1C06051W-V[1]		Small tape-and-reel	250
			ARC1C06051W-G[1]		Sample waffle tray	10

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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