PE24108

Document Category: Product Specification

3.3 VIN, 10A, Two-stage Buck Regulator for Low Output Voltage Applications

General Description

The PE24108 is a compact, low-profile, and ultra-high efficiency step-down DC-DC converter solution capable of delivering 10A per stage output current from an input voltage range from 3.0V to 3.6V. The output voltage is selected with external feedback resistors and can be adjusted between 0.4 and 1.0V.

Based on Murata's advanced two-stage architecture, the device consists of a two-phase interleaved charge pump followed by an interleaved buck regulator stage. This power system greatly reduces the dependency on inductance for high efficiency solutions in small-footprint and height-constrained applications.

Features

- Proprietary architecture enabling industry-leading efficiency with ultra-low profile and footprint
- 92% peak efficiency
- Wide input voltage range, from 3.0V to 3.6V, that supports running off a nominal 3.3V bus supply
- Output voltage regulation accuracy better than ±1% for all line and load variations
- Output voltage set by external feedback resistors
- Output can be adjusted by external AVS DAC
- External sync pin allows synchronization to an external clock
- Parallel up to four devices

Typical Applications

- Low-profile point-of-load (POL) regulators
- Optical modules
- Core supplies
- ASICs
- FPGA

Efficiency

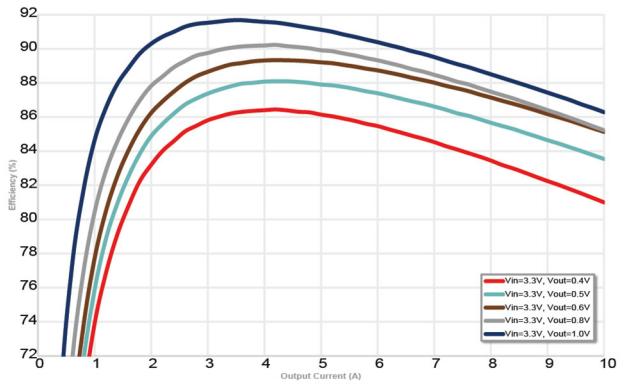

Figure 1. Efficiency Plot of Single Device

Simplified Application

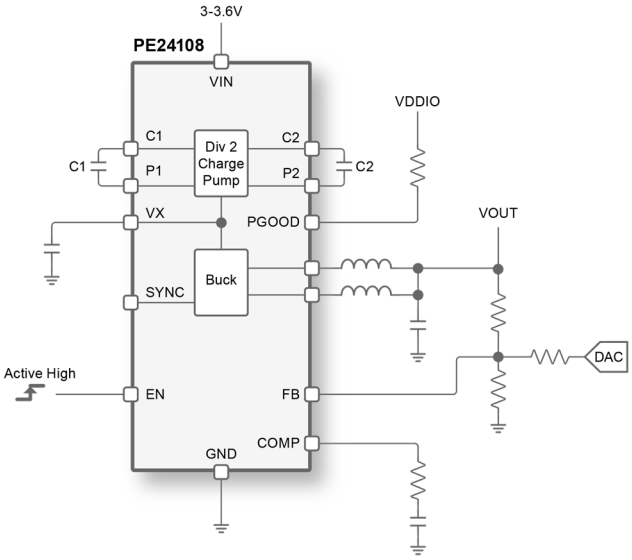

Figure 2. Typical Applications Circuit

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Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. PE24108 Absolute Maximum Ratings

Parameter	Min	Max	Unit
VIN to PGND	-0.3	3.8	V
EN, SYNC, FB, COMP to PGND	-0.3	V_{IN}+0.3	V
LX1, LX2	-0.3	2.1	V
C1, C2	-0.3	3.8	V
P1, P2	-0.3	2.1	V
PGOOD	-0.3	V_{IN}+0.3	V
VX	-0.3	2.1	V
Storage Temperature	-65	150	°C
Junction Temperature	-40	150	°C
Human body model, all pins[1]		2000	±V
Charged device model, all pins[2]		500	±V

Notes:
1. Human Body Model, all pins (Joint JEDEC/ESDA Human Body Model (JS-001-2017))
2. Charged Device Model, all pins (Joint JEDEC/ESDA Charged Device Model (JS-002-2018))

Recommended Operating Conditions

Table 2 lists the PE24108 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE24108 Recommended Operating Conditions

Parameter	Min	Max	Units
VIN Input Voltage Range, relative to AGND or PGND	3.0	3.6	V
Junction Temperature Range, T_J	-40	125	°C

Package Thermal Characteristics(1),(2)

Table 3 lists the package thermal characteristics for the PE24108.

Table 3. Package Thermal Characteristics

Parameter	Condition	Min	Max	Units
Maximum Junction Temperature	Measured at max ambient temperature (T_A) and max power dissipation.		150.0	°C
Junction-to-case Top Thermal Resistance (Θjt)	JEDEC JESD51-12-01 and JESD15-3	19.2		°C/W
Junction-to-board Thermal Resistance (Θjb)	JEDEC JESD51-12-01 and JESD15-3	4.8		°C/W
Junction-to-air Thermal Characterization (Θja)	JEDEC JESD51-12-01 and JESD15-3	20.8		°C/W

Notes:

1. Package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.
2. Junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the IC but is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.

Electrical Characteristics

V_{IN} = 3.0V–3.6V, V_{OUT} = 0.4V to 1.0V, I_{OUT} = 0 to 10A per part, 5A per phase V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40 °C to +125 °C, Rc = 2.7 kΩ Cc = 4.7 nF. Flying capacitors C1 and C2 = 22 µF unless otherwise noted. Typical values are at T_A = T_J = 25°C; V_{IN} = 3.3V; V_{OUT} = 0.5V.

Table 4. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply						
Input Voltage Range	V_{IN}		3.0		3.6	V
UVLO Threshold High	V_{UVLO_H}	V_{IN} rising			2.9	V
UVLO Threshold Low	V_{UVLO_L}	V_{IN} falling	2.5			V
UVLO Hysteresis	V_{HYST}			200		mV
Supply Currents						
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0Vm T_A = 25 °C			215	µA
Operating Supply Current	I_Q	I_{VIN} V_{EN} >1.1V closed-loop switching frequency 800 kHz		50		mA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{TSD}	Typical temperature rising Minimum temperature falling	125	140		°C
Thermal Shutdown Hysteresis	T_{TSD_HYST}	Note device is always guaranteed to be operating < 125 °C		20		°C
Power Good Thresholds						
Power Good Under-voltage		V_{OUT} falling fault		90		% of V_{OUT}
Power Good Over-voltage		V_{OUT} rising		110		% of V_{OUT}
Logic Thresholds (EN)						
Logic Threshold High		Tolerant up to 3.6V	0.4			V
Logic Threshold Low					0.12	V
Hysteresis				50		mV
Pull Down Resistor			100	500		kΩ
Logic Thresholds Sync						
SYNC Threshold High		DC coupled	0.7xVIN			V
SYNC Threshold Low		DC coupled			0.3x V_{IN}	V
Hysteresis				200		mV
Logic Outputs (PGOOD,SYNC)						
Logic Output Low		IL = 1 mA			0.4	V
Buck Converter						
Nominal Clock Frequency	f_{SW_nom}			1600		kHz
Charge Pump Switching Frequency Range	f_{SW_CP}	External sync		0.5 x f_{SW_sync}		kHz
Buck Switching Frequency Range	f_{SW_BUCK}	External sync		0.5 x f_{SW_sync}		kHz

Electrical Characteristics

V_{IN} = 3.0V–3.6V, V_{OUT} = 0.4V to 1.0V, I_{OUT} = 0 to 10A per part, 5A per phase V_{PGND} = 0V, V_{EN} = 1.8V, T_A = T_J = -40 °C to +125 °C, Rc = 2.7 kΩ Cc = 4.7 nF. Flying capacitors C1 and C2 = 22 µF unless otherwise noted. Typical values are at T_A = T_J = 25°C; V_{IN} = 3.3V; V_{OUT} = 0.5V.

Table 4. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synchronization Range	f_{SW_sync}	External sync must be higher than internal sync	1750		2600	kHz
Output Voltage Range	V_{OUT_SET}		0.4		1	V
FB Set Point				300		mV
FB Accuracy			-2		+2	%
FB Accuracy		V_{IN}=3.1V to 3.5V	-1		+1.5	%
Output Voltage Ripple	V_{RIPPLE}	Up to 300 MHz bandwidth C_{LOAD} = 188 µF, I_{LOAD} = 10A V_{OUT} = 0.5V, T_A = 25 °C		10		mV
Output Current	I_{OUT}	5A per phase Two phases per device. See Figure 26, Recommended Operating Area.			10	A
Load Regulation		I_{OUT} = 6 to 10A, C_{OUT} = 188 µF T_A = 25 °C		0.5		mV
Line Regulation		V_{IN} = 3.0V to 3.6V, V_{OUT} = 0.5V C_{OUT} = 188 µF, T_A = 25 °C		1.65		mV/V
Error Amplifier Transconductance				2		mS
Peak Current Limit Set Point		Per phase	6			A
Peak Current Limit Accuracy				±20		%
Timing						
EN to PG time		C_{OUT} = 188 µF, I_{LOAD} = 10A		1		ms

PE24108 Pin Configuration

This section provides pin configuration information for the PE24108. Figure 3 shows the pin map of this device in a QFN package. Pin functions are covered in Table 5.

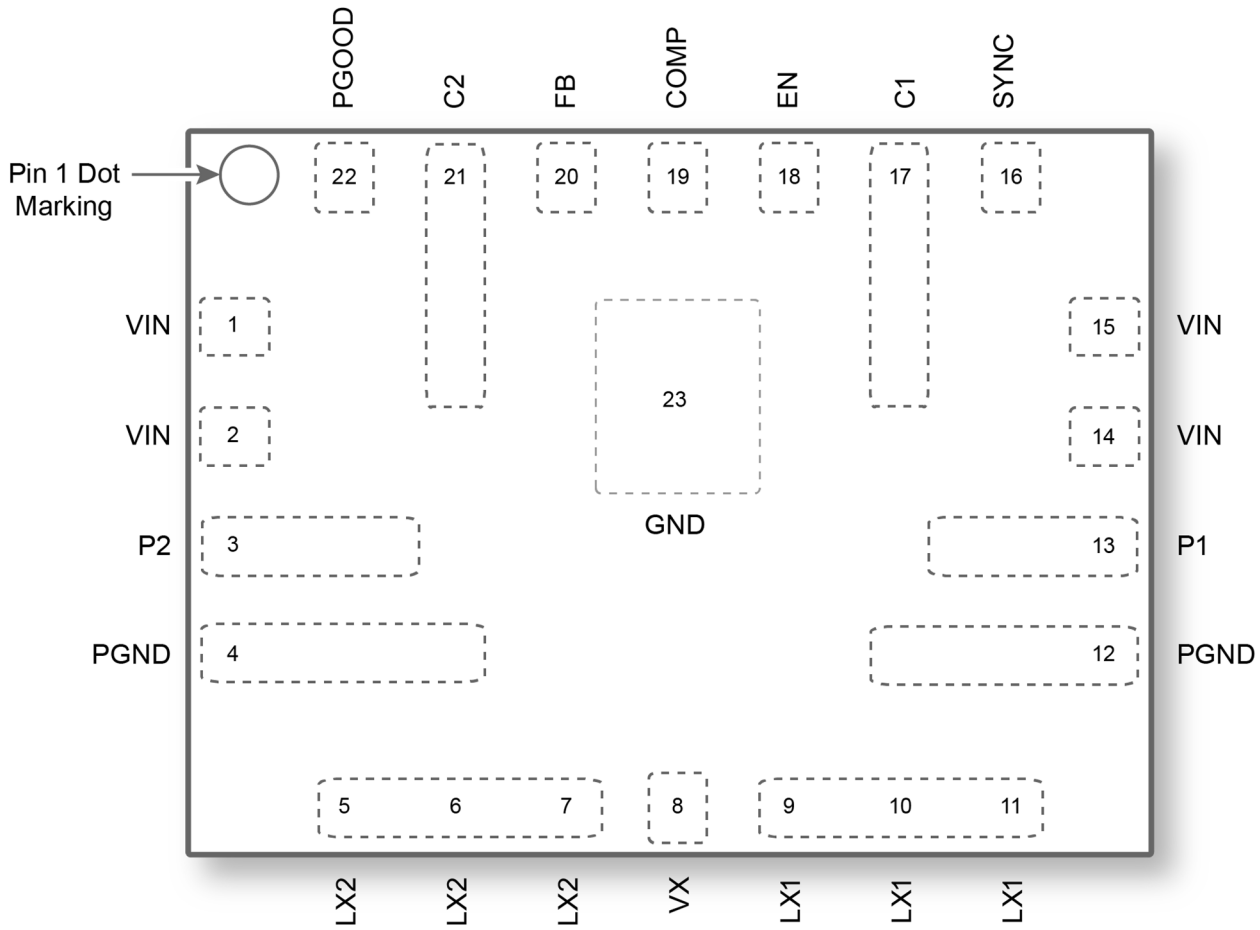


Figure 3. Pin Configuration (Top View)

Pin Descriptions

Table 5. Pin Descriptions

Pin No.	Pin Name	Description
1,2,14,15	VIN	Connect to an input voltage between 3.0V and 3.6V. Ensure that VIN is bypassed by two external capacitors of 4.7 µF.
13	P1	Phase 1 flying capacitor. Connect to capacitor C1.
4,12	PGND	Connect to the power ground.
5,6,7	LX2	Connect to external chip inductor of 150 nH.
8	VX	Output capacitor of the charge pump. Connect a capacitor of 4.7 µF to ground.
9,10,11	LX1	Connect to external chip inductor of 150 nH.
3	P2	Phase 2 flying capacitor. Connect to capacitor C2.
22	PGOOD	Power good pin needs to be pulled up by an external resistor to a voltage less than 3.6V. In a multiple device configuration, all PGOOD pins should be connected to a single pull-up resistor. PGOOD is pulled low if the output voltage is below PGOOD under-voltage or above PGOOD over-voltage. This signal is only valid after soft start is completed.
21	C2	Flying capacitor. Connect to a capacitor of C2 of 22 µF between this pin and P2.
20	FB	Feedback pin. Set external resistor divider to a 0.3V reference to set the output voltage. To reduce output ripple, an optional feed forward capacitor of 470 pF can be added in parallel with the top resistor. In parallel operation, all FB pins should be connected.
19	COMP	Compensation pin. Connect to a 2.7K resistor and 4.7 nF capacitor to ground for operation over the full output voltage range, Compensation can be changed to improve dynamic responses if a narrower output voltage range is used in the application.
18	EN	Enable input. Pull high to VIN or drive with a logic high to enable the converter. Connected to an internal pull down.
17	C1	Flying capacitor. Connect to a capacitor of C1 of 22 µF between this pin and P1.
16	SYNC	The sync pin is an open collector I/O pin. At startup, the internal oscillator will appear on the pin. In parallel operation, all the sync pins should be connected, and the parts will synchronize to the fastest internal oscillator. The sync pin can be overclocked by an external clock after the device initially starts. To synchronize the device, the external clock must be faster than the internal clock of 1600 kHz. Both the charge pump and buck are synchronized to harmonics of this clock.
23	GND	Analog ground pin

Functional Block Diagram

Figure 4 shows the functional block diagram for the PE24108.

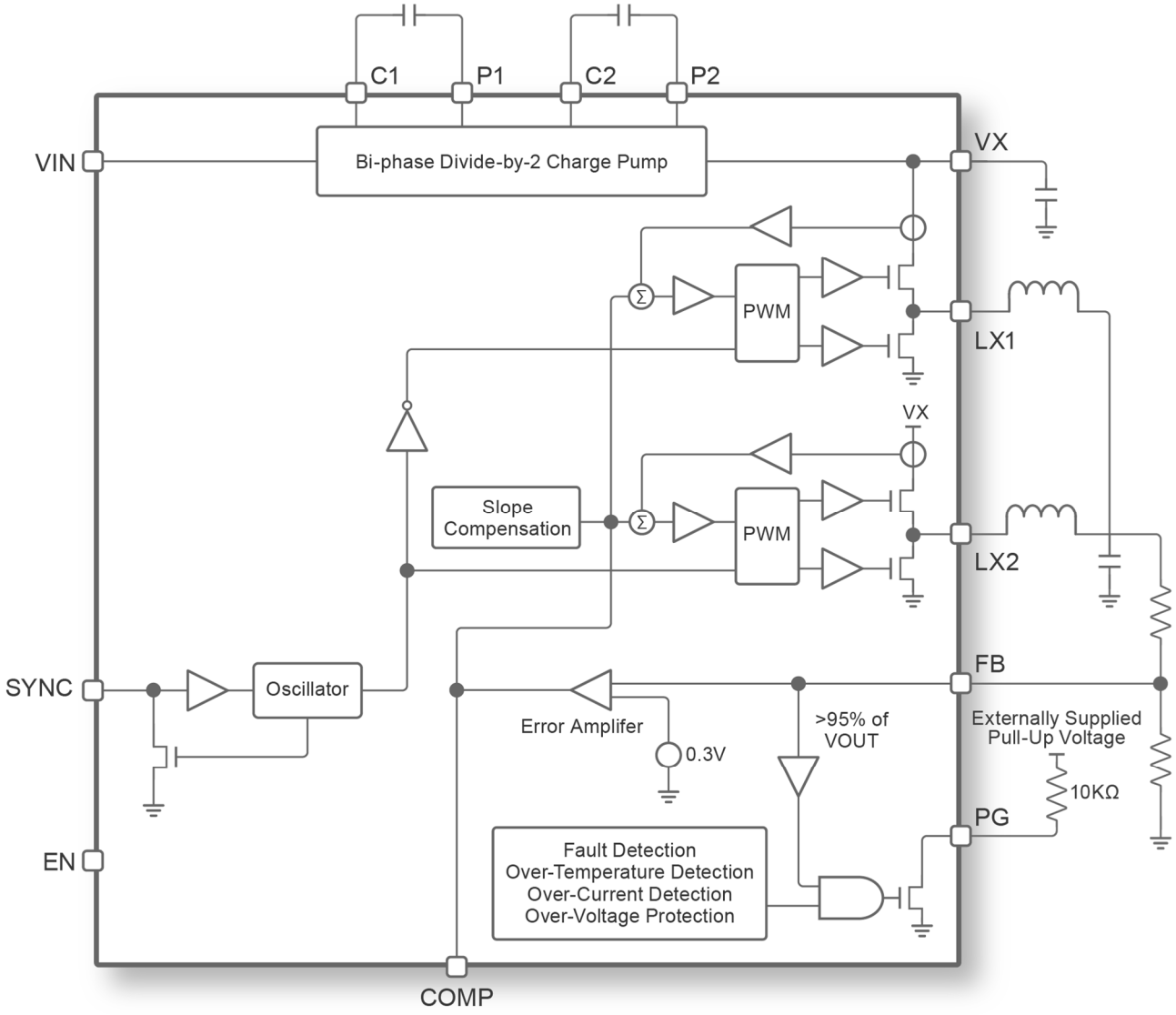


Figure 4. Functional Block Diagram

Typical Performance Characteristics

Figure 5 through Figure 25 show the typical operating performance data of the PE24108.

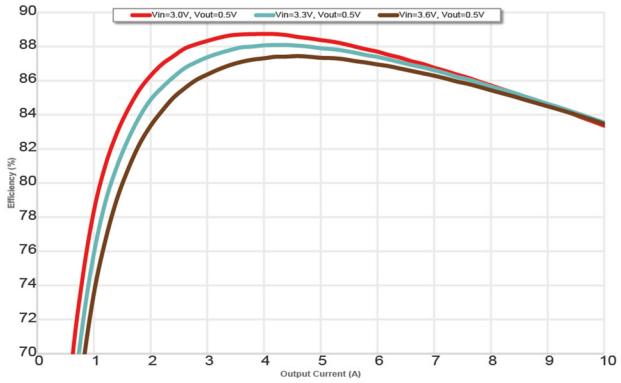


Figure 5. Efficiency vs. Load Current V_{IN} = 3.0V,3.3V,3.6V V_{OUT} = 0.5V Single Device Fsw = 800 kHz

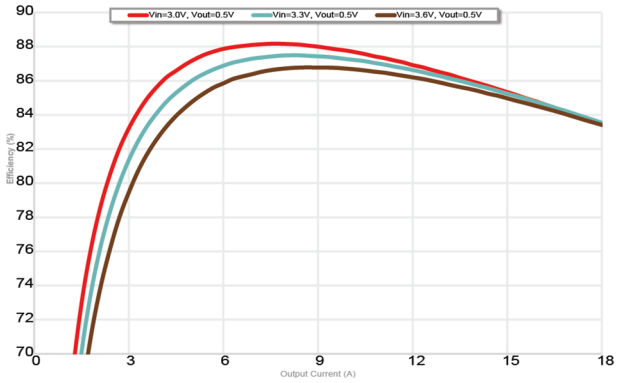


Figure 6. Efficiency vs. Load Current V_{IN} = 3.0V,3.3V,3.6V V_{OUT} = 0.5V 2 Devices in Parallel Fsw = 800 kHz

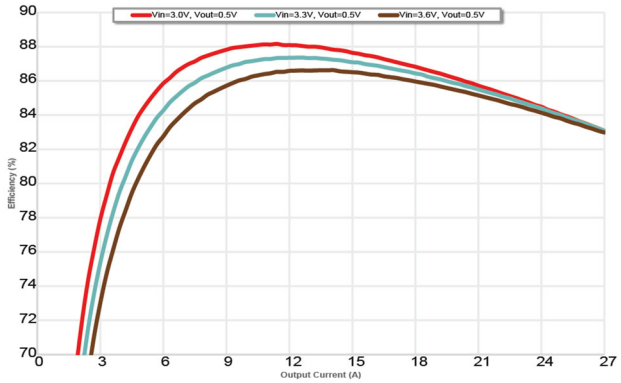


Figure 7. Efficiency vs. Load Current V_{IN} = 3.0V,3.3V,3.6V V_{OUT} = 0.5V 3 Devices in Parallel Fsw = 800 kHz

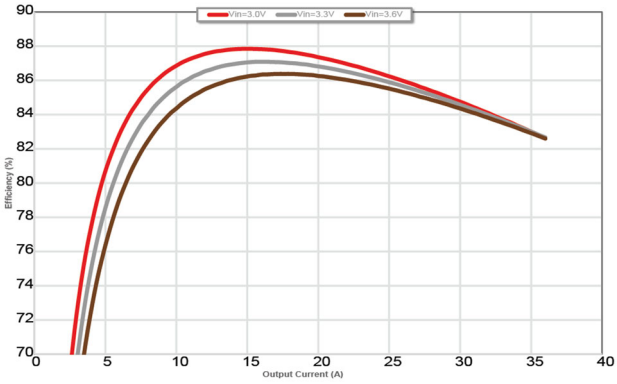


Figure 8. Efficiency vs. Load Current V_{IN} = 3.0V,3.3V,3.6V V_{OUT} = 0.5V 4 Devices in Parallel Fsw = 800 kHz

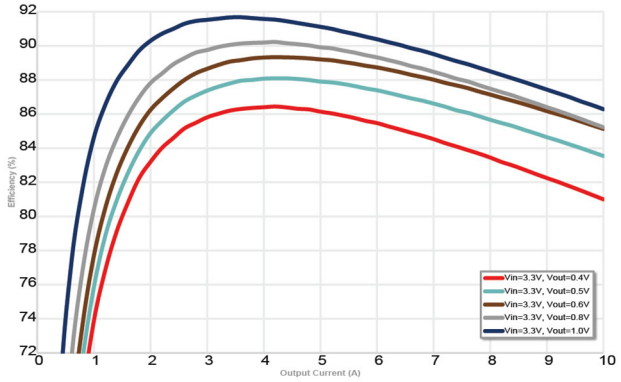


Figure 9. Efficiency vs. Load Current V_{IN} = 3.3V V_{OUT} = 0.4V,0.5V,0.6V,0.8V,1.0V (Single Device)

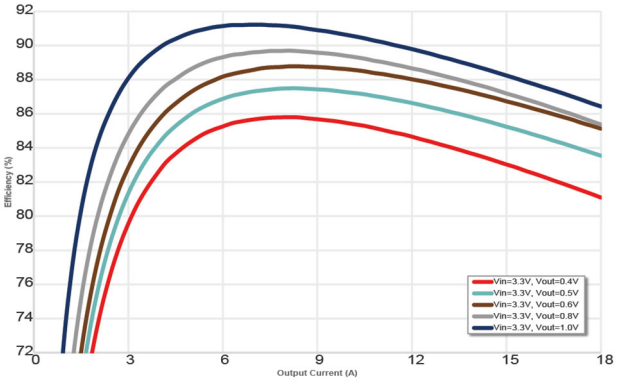


Figure 10. Efficiency vs. Load Current V_{IN} = 3.3V V_{OUT} = 0.4V,0.5V,0.6V,0.8V,1.0V (Two Devices)

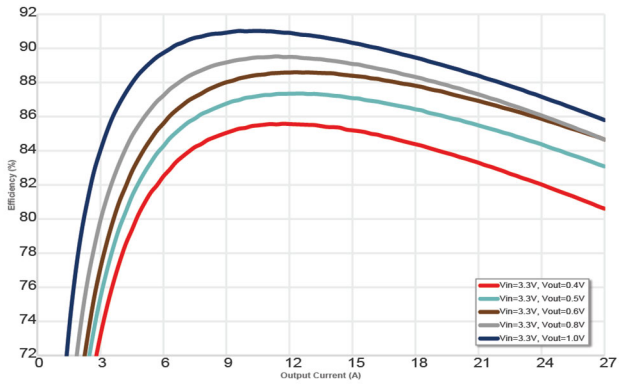


Figure 11. Efficiency vs. Load Current V_{IN} = 3.3V V_{OUT} = 0.4V,0.5V,0.6V,0.8V,1.0V (3 Devices)

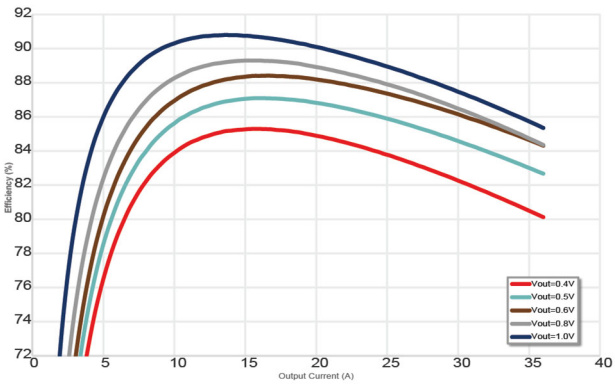


Figure 12. Efficiency vs. Load Current V_{IN} =3.3V V_{OUT} = 0.4V,0.5V,0.6V,0.8V,1.0V (Four Devices)

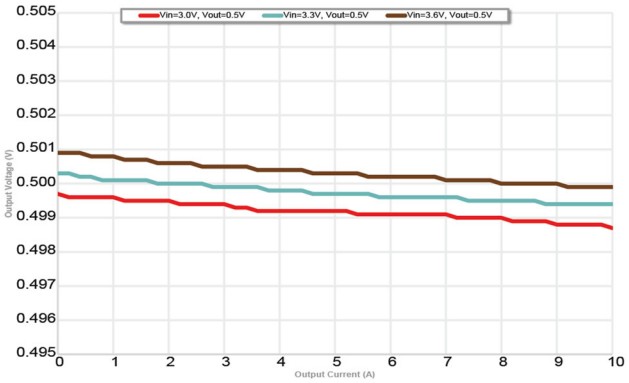


Figure 13. Output Voltage vs. Output Current Single-Device, V_{OUT} = 0.5V

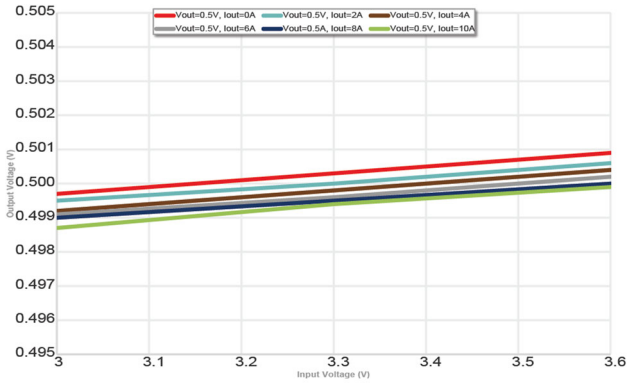


Figure 14. Line Step Output Voltage vs. Input Voltage Single-Device, V_{OUT} = 0.5V (Line Regulation, mV/V)

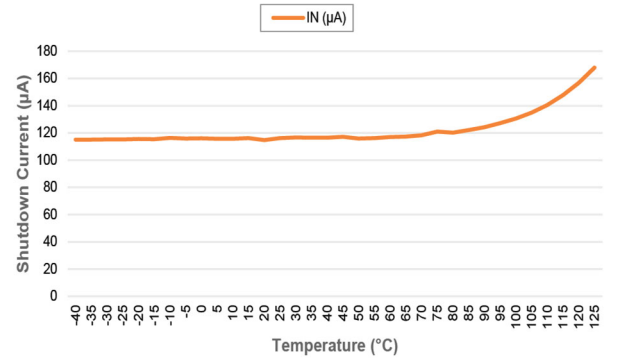


Figure 15. Shutdown Current vs. Temperature

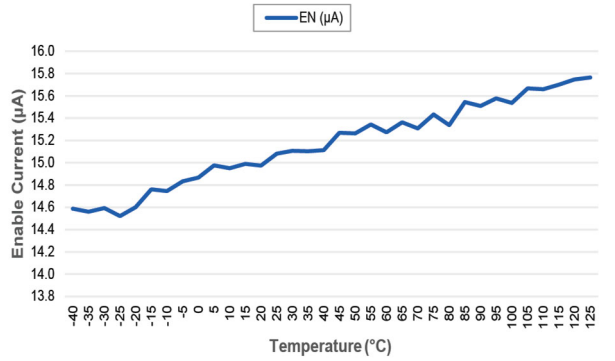


Figure 16. EN Pin Leakage vs. Temperature

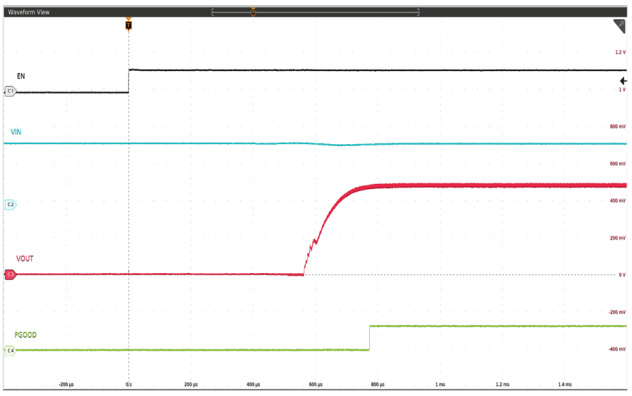


Figure 17. Startup into Load V_{IN} = 3.3V V_{OUT} = 0.5V IOUT = 6A

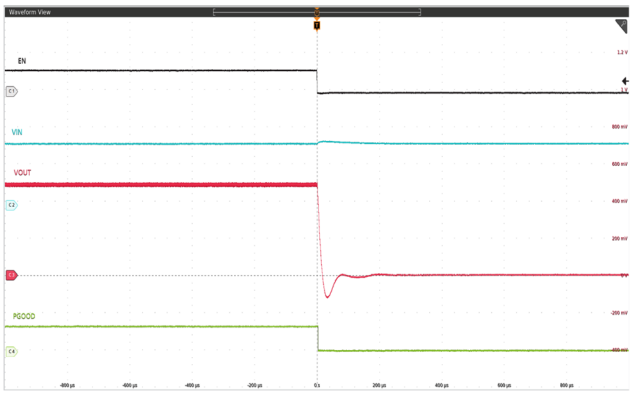


Figure 18. Shutdown into Load V_{IN} =3.3V V_{OUT} = 0.5V I_{OUT} = 6A

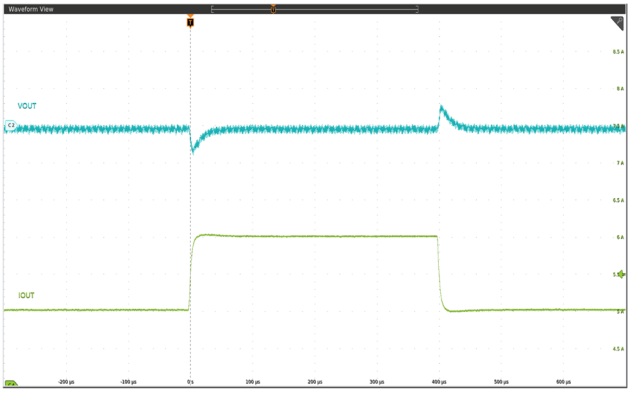


Figure 19. Load Transient 5A to 6A, 0.2A/µs V_{IN} = 3.3V, V_{OUT} = 0.5V

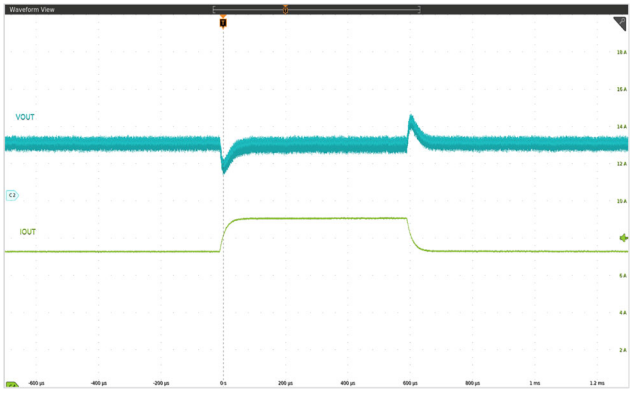


Figure 20. Load Transient 20% 7.2A–9A, 0.5A/µs V_{IN} = 3.3V, V_{OUT} = 0.5V

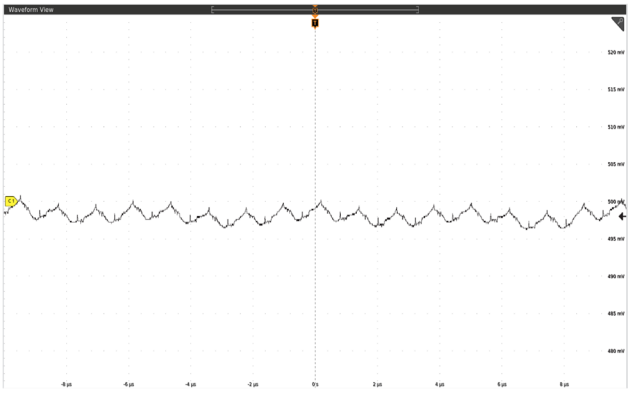


Figure 21. Output Ripple Single EVK V_{IN} = 3.3V V_{OUT} = 0.5V, I = 9A

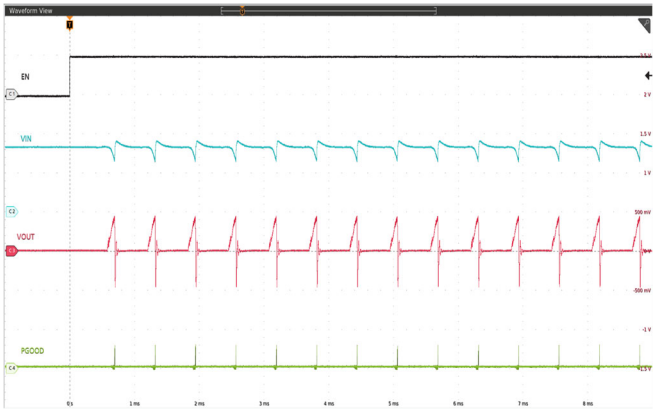


Figure 22. Startup into Short Circuit

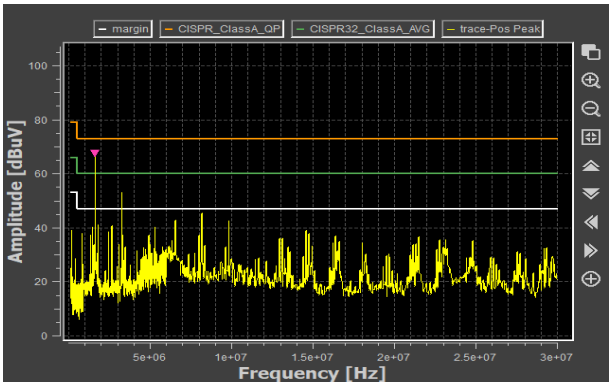


Figure 23. Conducted EMI (Input) Single EVK V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 6A

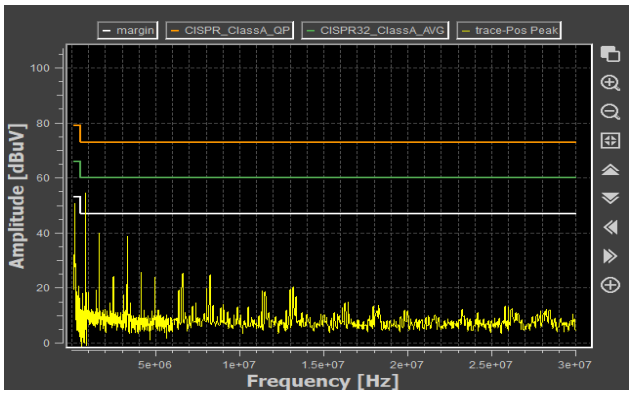


Figure 24. Conducted EMI (VOUT) Single EVK V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 6A

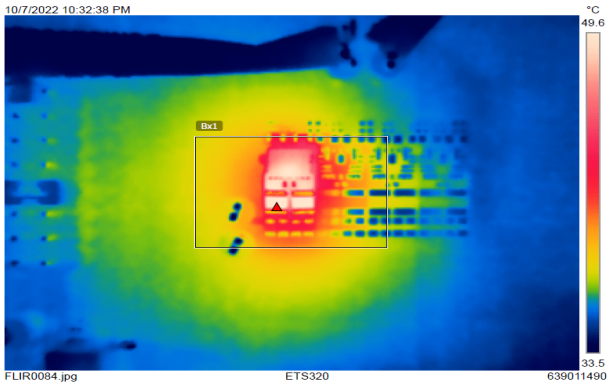


Figure 25. Thermal Plot Single Device V_{IN} =3.3V, V_{OUT} = 0.5V, I_{OUT} = 10A

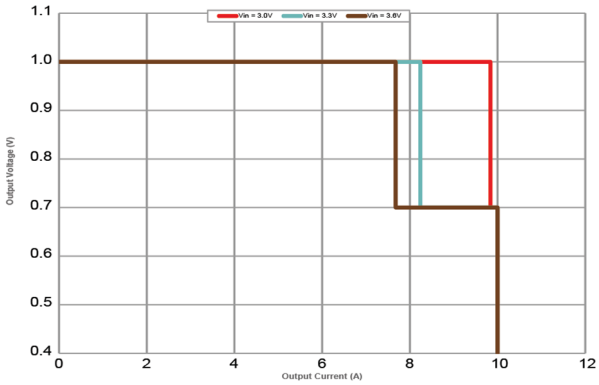


Figure 26. Recommended Operating Area V_{IN} = 3.0V–3.6V, -40°C to +115°C

Theory of Operation

The PE24108 is a two-stage, DC-DC POL regulator that can be used in parallel operation to allow higher current outputs.

Charge Pump

Most of the power conversion is done by a divide-by-two charge pump. This charge pump is in effect an open-loop DC transformer where the output voltage tracks the input voltage and presents the downstream buck regulator with an unregulated but much lower input voltage than a traditional single-stage buck.

The charge pump is based on a patented, proprietary architecture developed by Murata that employs soft start, soft switching, and close synchronization with the buck stage to assure that no current flows during transitions within the charge pump. This eliminates issues such as inrush current, and large transition losses seen with more traditional charge pumps.

The charge pump also demonstrates extremely high conversion efficiency with much lower EMI than traditional single-stage buck architectures. The phase-interleaved design, in which two individual charge pumps operate in parallel, coupled with a 50% charge-pump duty cycle minimizes pulsed currents at the input and exhibits very low input ripple, irrespective of the output voltage of the downstream buck stage.

To assure high efficiency, the charge pump relies on well-balanced values of capacitance throughout the charge pump stage over operating conditions, so particular attention needs to be paid to the physical sizing of the capacitors, and the effects of DC bias on capacitance.

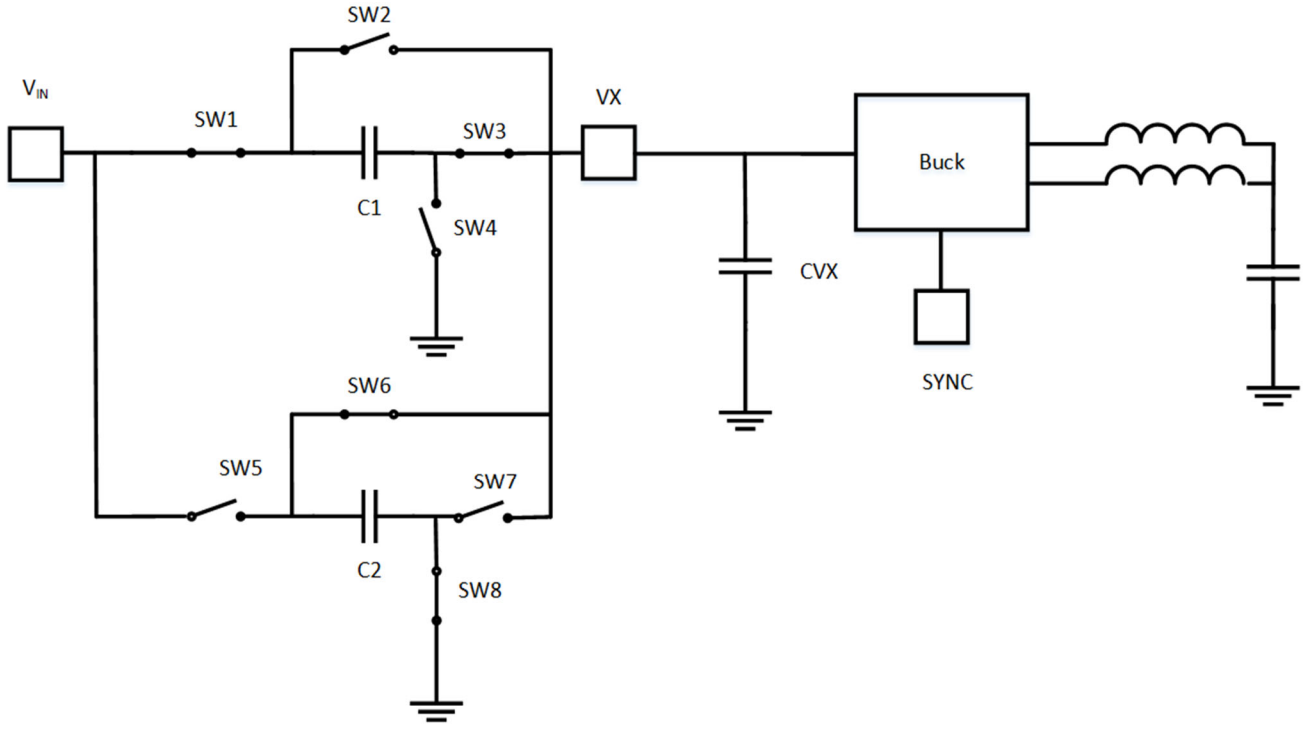


Figure 27. Phase 1 Charge Pump Operation

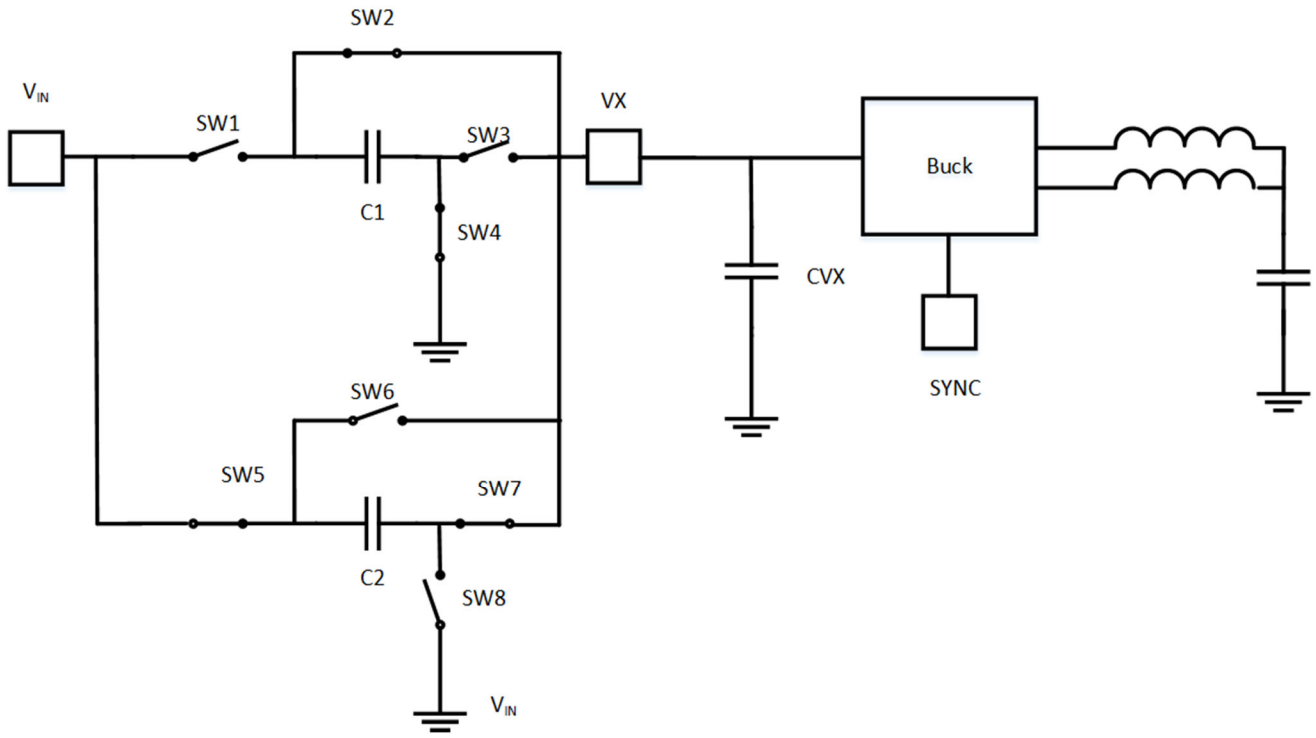


Figure 28. Phase 2 Charge Pump Operation

Between the two phases, a constant flow of energy is drawn from the input and supplied to the downstream buck converter. This further minimizes conducted EMI at the input of the converter and ensures a very low noise intermediate for the buck converter.

Buck Converter

The buck converter utilizes fixed-frequency peak current mode PWM control to regulate the output voltage. It has two PWM phases that are interleaved with a fixed-phase difference of 0 or 180 degrees.

The buck converter switching frequency can be overdriven by using the SYNC pin to further control system EMI. See the Synchronization section.

Compensation of the Buck Regulator

The buck regulator is a bi-phase, fixed-frequency peak current mode regulator, with phases at 0º and 180º.

Both regulators connect to a single-slope compensation pin (COMP). In normal operation, it is recommended to connect this to a 2.7 kΩ resistor with a 4.7 nF capacitor to ground as shown in Figure 29.

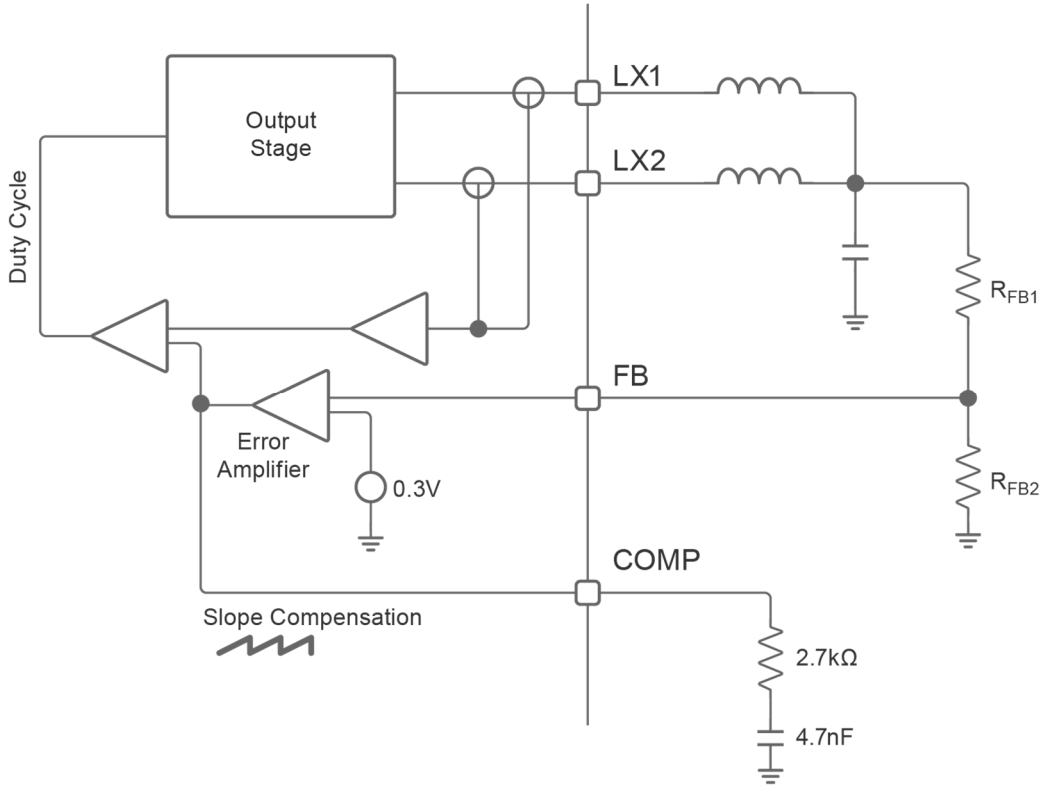


Figure 29. Compensation Circuit

Detailed Description

Setting the Output Voltage

The output voltage is set by the external feedback resistors connected between VOUT and ground which are compared to an internal 300 mV reference. To prevent noise coupling onto the FB pin, the divider resistor values should not be too high. For parallel operation the FB pins should be connected.

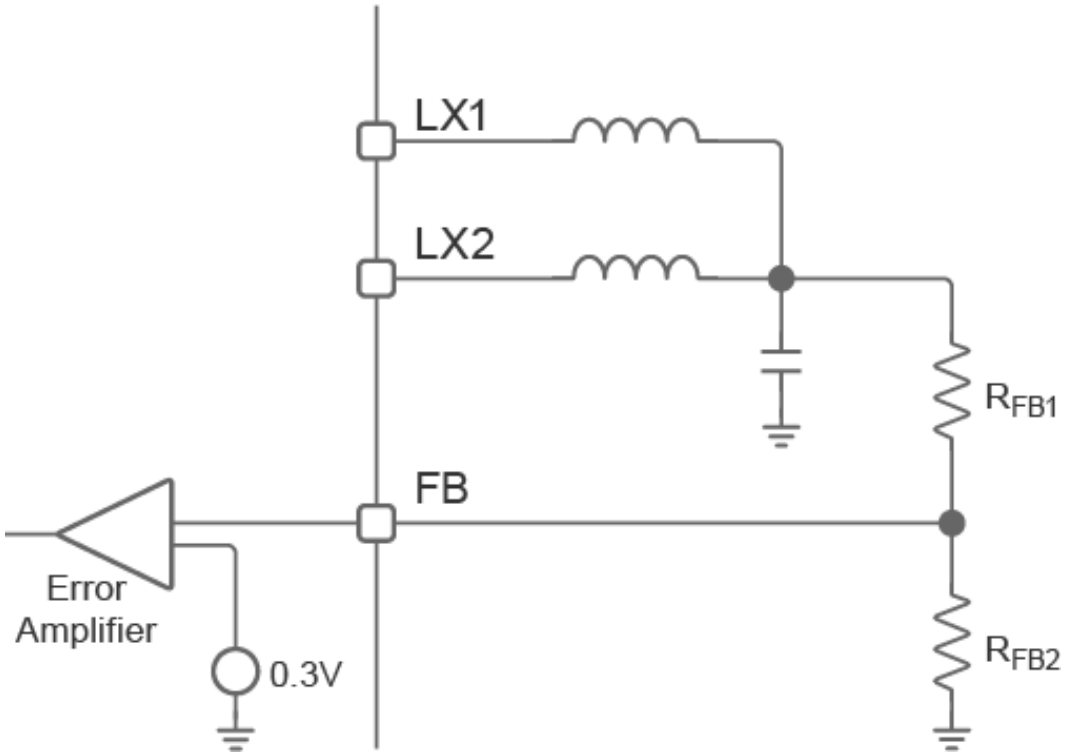


Figure 30. Setting the Output Voltage with External Feedback Resistors

To set the output voltage, first select a value for R_{FB2} of < 10 kΩ.

To calculate the value of R_{FB1}, use the following formula, where VFB=0.3V.

$$R_{FB1} = R_{FB2}.\frac{VOUT - V_{FB}}{V_{FB}}$$

If picking the value of the top resistor first, calculate the bottom resistor R_{FB2} as follows:

$$R_{FB2} = \frac{R_{FB1}.V_{FB}}{V_{OUT} - V_{FB}}$$

To maintain the initial accuracy specifications of the device, it is recommended that the external resistances should be 0.1% resistors. If higher accuracy is required, it is necessary to close the loop with an external DAC.

Power-up Sequence

The PE24108 wakes up when V_{IN} exceeds the input under-voltage (UVLO) threshold of 2.9V and the EN pin is taken high above the threshold voltage.

Initially, the device powers up its internal logic and then, if no fault is present, it proceeds to balance the charge pump for a period of 128 µs.

After this, the charge pump operates in soft start control. This process will continue for 16 µs and until the charge pump is charged to within < 10% of $V_{IN}/2$.

When this happens, the charge pump enters normal switching and can supply the full load current.

Next, the buck regulator soft-starts until the output voltage is reached.

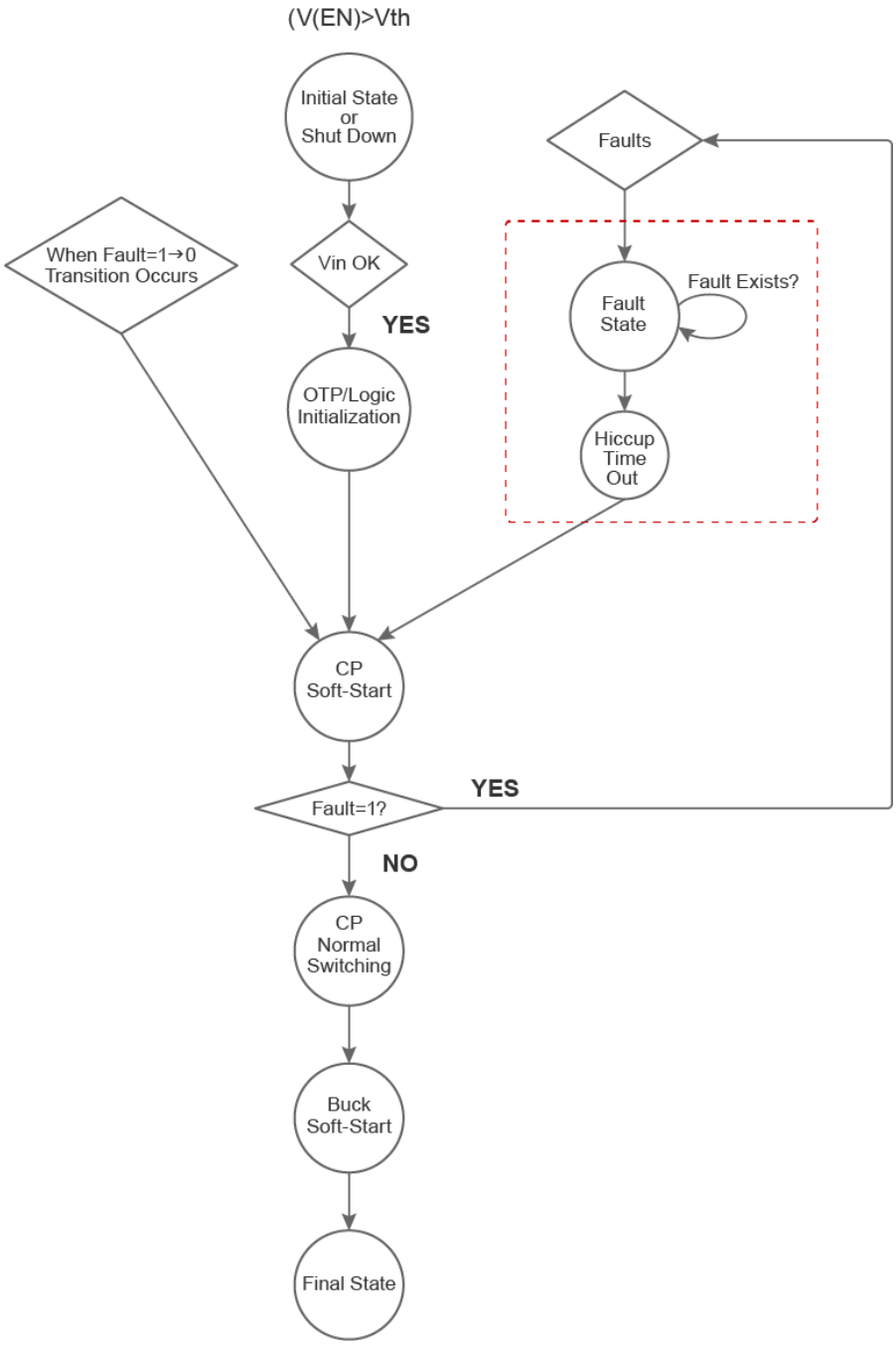


Figure 31. Power-up Sequence

During the initial power-up sequence and until PGOOD goes high, the PE24108 always uses its own internal oscillator. After PGOOD is established, the device may be synchronized to an external clock on the SYNC pin.

Enable (EN)

The EN pin is designed to be compatible with low voltage logic signals from DSP controllers and ASICs and has a threshold high of 0.4V. A voltage on this pin above 0.4V enables the PE24108. The EN pin is tolerant up to voltages up to 3.6V and can be tied directly to the input supply to enable the device upon power-up.

If a voltage of less than 0.2V is present on the pin, the device enters shutdown.

Input Under-voltage Lockout (UVLO)

The PE24108 is intended to work from a 3.3V input supply and begins operating above its UVLO threshold of 2.9V. The UVLO threshold has a typical hysteresis of 50 mV.

Power Good (PGOOD)

The PGOOD pin is an open drain pin. The PGOOD pin must be pulled up externally to a power supply of less than 3.6V.

During startup, the PGOOD pin is pulled low until the output voltage reaches within 5% of the value (i.e., > 95% of VOUT) programed by the feedback resistors. Above this, the PGOOD pulldown FET is high impedance, and the PGOOD pin is pulled up by the external resistor.

If the output voltage goes above the PGOOD over-voltage level, then the PGOOD pin is pulled low.

If operating multiple devices in parallel, the PGOOD pins should be tied together to a single pull-up resistor.

Temperature Detection

The PE24108 includes an integrated temperature sensor that protects the IC in the event of overheating. When the PE24108 enters thermal shutdown, its outputs are turned off to reduce power dissipation inside the chip. When the temperature drops below the hysteresis limit, the output is turned on again. If the underlying cause of the over-temperature fault is not cleared, the system enters a hiccup mode of operation until the fault condition is removed.

Synchronization

The PE24108 contains an internal oscillator that initially switches at 1.6 MHz. If the application only uses the internal oscillator, then nothing should be attached to the SYNC pin.

If the device is required to synchronize to either an external clock, or for multiple devices to synchronize to each other to avoid beat frequencies, then an external pull-up resistor should be pulled up to V_{IN} (RSYNC1) It is recommended that a value of 10 kΩ be used as shown in Figure 33. The internal oscillator will then synchronize to the clock edges of the fastest clock on the SYNC pin. The SYNC pin can be DC or AC coupled; this will affect the level of external clock needed.

From a DC perspective, the SYNC pin has thresholds set at 68.2% and 29.2% of V_{DD}. The input sync waveform needs to exceed these thresholds for the SYNC signal to be recognized.

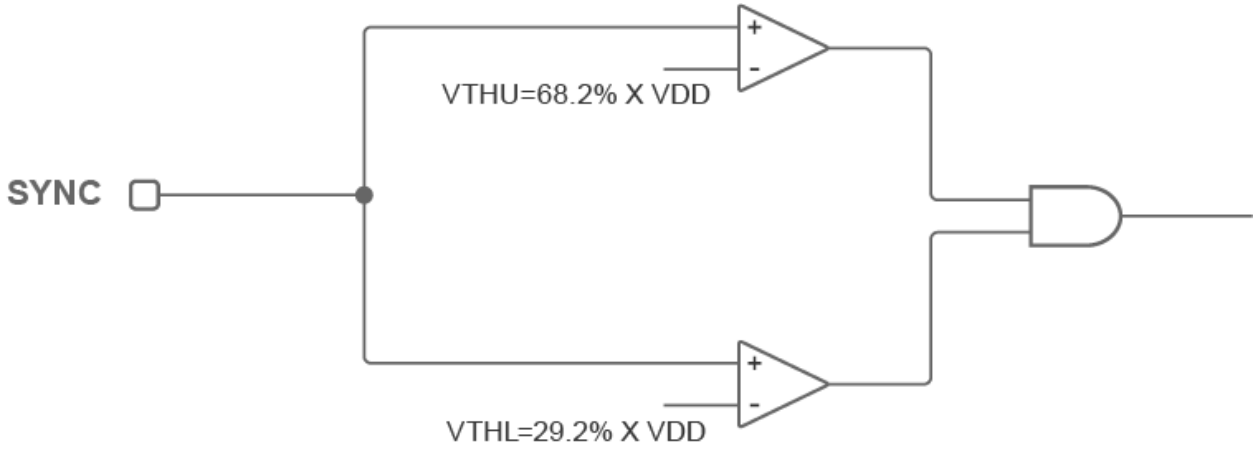


Figure 32. Sync Pin Thresholds

To synchronize with an external clock, the SYNC pin can be overdriven by connecting directly to an external clock as indicated in Figure 33.

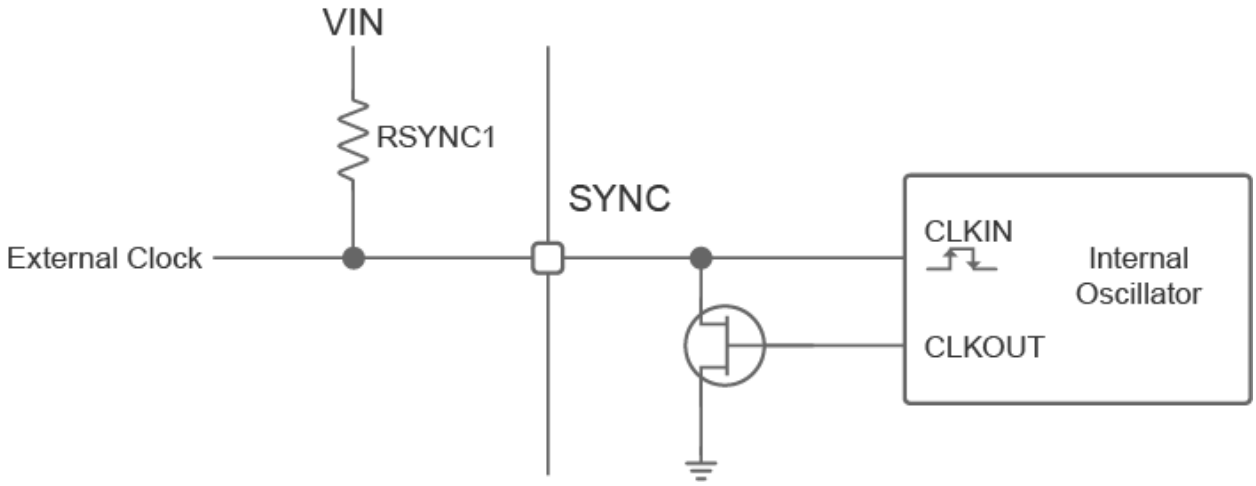


Figure 33. DC Coupled Synchronization Circuit

If the voltage level is less than these levels, the device will not synchronize. The scope plots in Figure 34 and Figure 35 show the device with a SYNC waveform below the threshold and a SYNC waveform above the threshold.

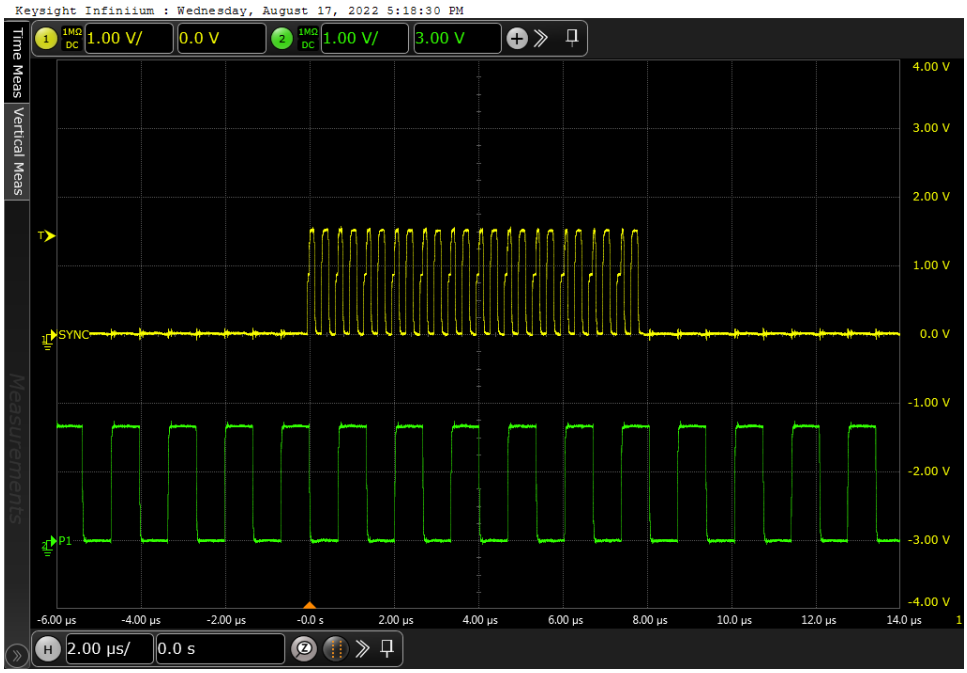


Figure 34. Device Not Synchronizing with SYNC=1.5V DC Coupled

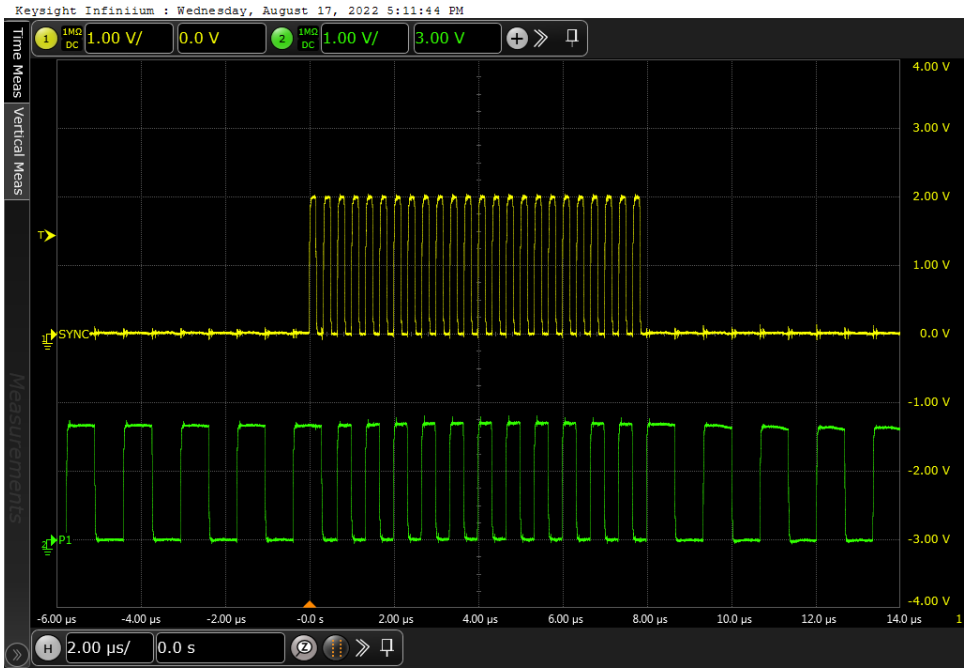


Figure 35. Scope Plot Showing Synchronization with SYNC = 2V DC Coupled

If a lower voltage external synchronization clock is needed, SYNC can be AC-coupled into the sync pin and a pull-down resistor of value equal to the pull-up resistor added as in Figure 36.

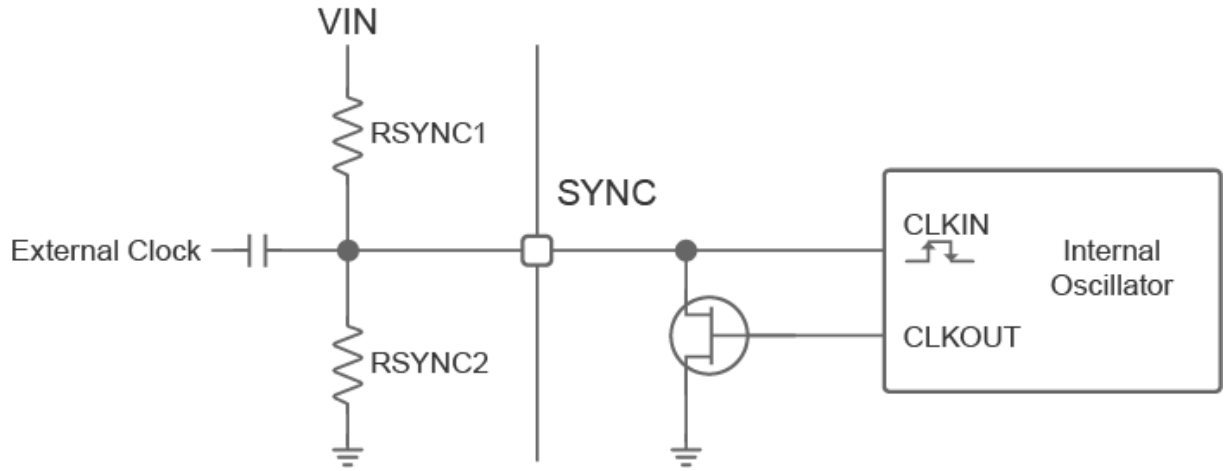


Figure 36. AC-coupled Synchronization Circuit

Faults

The PE24108 provides extensive protection against input and output faults, output overload and over-temperature as summarized in the following table.

Table 6. Faults

Fault	Fault Response	Fault Detection Time(1)	Threshold
VIN Under-voltage	Power on reset	Immediate (VIN falling)	< 2.5V
VOUT Over-voltage	PGOOD pulled low	Immediate	> 110% of target VOUT
VOUT Under-voltage	PGOOD pulled low	Immediate	< 90% of target VOUT
VOUT Short Circuit	PGOOD pulled low; hiccup mode[3]	Immediate	
Peak Current Limit	PGOOD pulled low; hiccup mode(2)	Immediate	> 10A
Over-temperature(3)	PGOOD pulled low; hiccup mode(4)	Immediate	>150°C

Notes:

Typical detection time; see Electrical Characteristics for minimum and maximum specifications.

In hiccup mode, switching is disabled, the output is tri-stated, and a 5 ms wait timer is started. When the wait timer expires, the system attempts to restart the charge-pump stage but will hiccup until the fault condition is cleared. During this state, PGOOD is set to “0” until the fault is removed.

Junction temperature of PE24108 die is used for over-temperature detection.

The system will not attempt to restart until a wait timer has expired and the PE24108 junction temperature has dropped below the over-temperature hysteresis threshold.

Applications Information

Parallel Operation

Up to four PE24108 devices may be connected in parallel as power stages allowing output currents of 10A,18A, 27A or 36A. In parallel operation, the SYNC, COMP and PGOOD and EN pins of both devices should be connected. The output voltage can be adjusted using a single DAC externally feeding a current via a resistor into the feedback network.

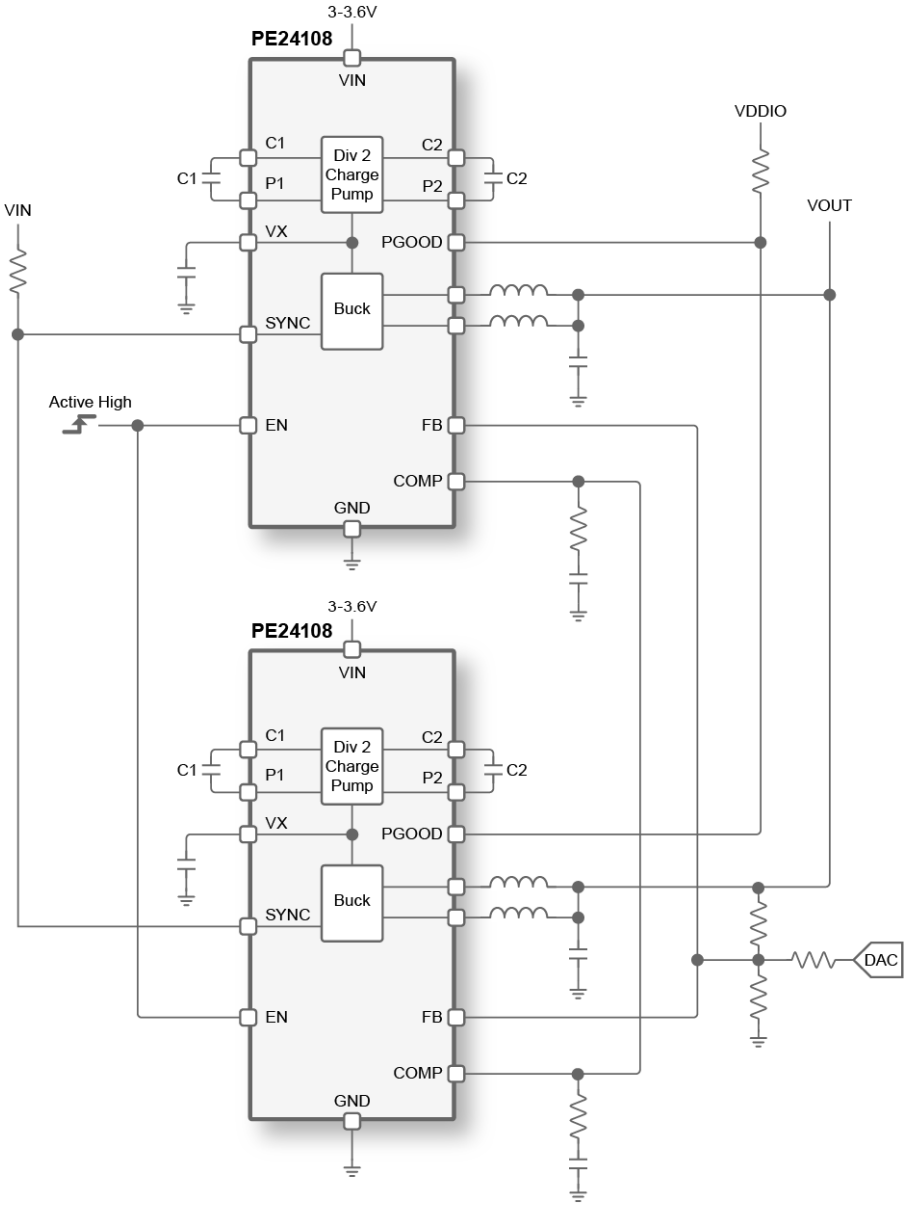


Figure 37. Using Two PE24108 Parts in Parallel

Example Layout of Two Devices in Parallel

The example below shows an example of two parts in parallel providing 18A supply at V_{OUT}=0.4V to 1.0V. This layout can fit in a very small form factor, because the dual-stage architecture is extremely thin at 1.2 mm.

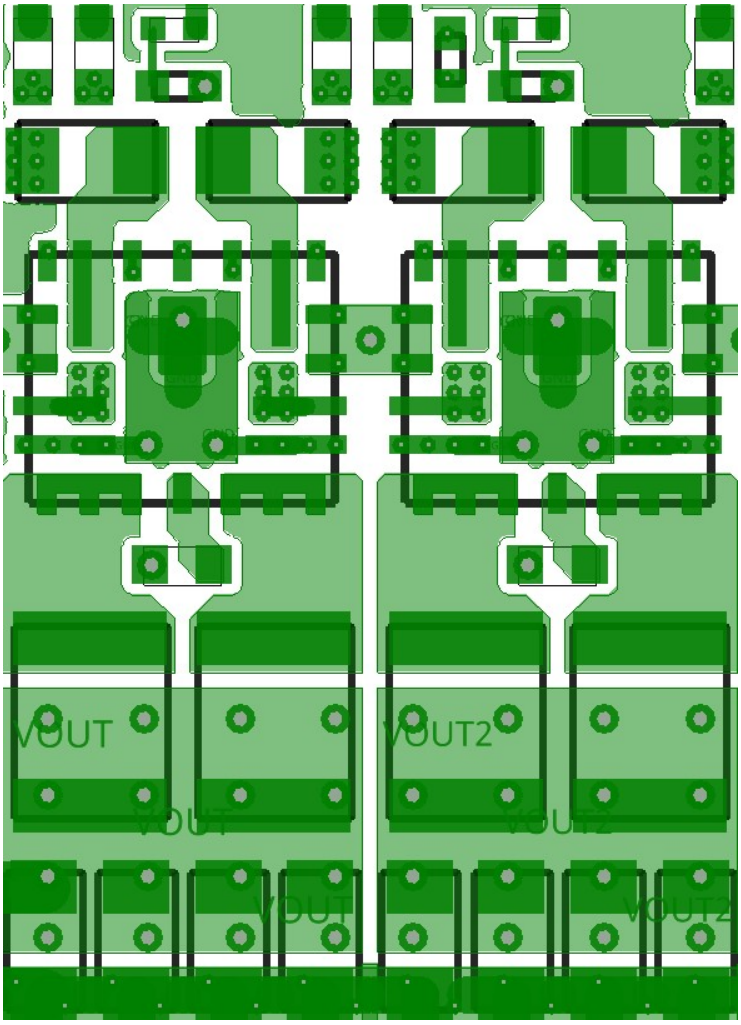


Figure 38. Example Layout of Two Parallel Devices

Oscillator Synchronization in Parallel Operation

The PE24108 has a SYNC pin that can be used in three separate operation modes:

1. *Basic standalone operation*
2. *Parallel operation without an external clock*
3. *Parallel operation with a common external clock*

Basic Standalone Operation

In basic operation mode for a standalone PE24108 configured for a 10A supply, nothing needs to be connected to the SYNC pin. The SYNC pin will oscillate at its own internal oscillator frequency.

If a pullup is connected to the SYNC pin, then a divided-down version of the internal clock will be seen on the SYNC pin This might be useful to synchronize other regulators in the system.

Parallel Operation Without an External Clock

In parallel operation of multiple PE24108s without an external clock, the sync pin should be connected to a common external pull-up resistor. In this mode, the devices will synchronize to the fastest clock of the devices in parallel.

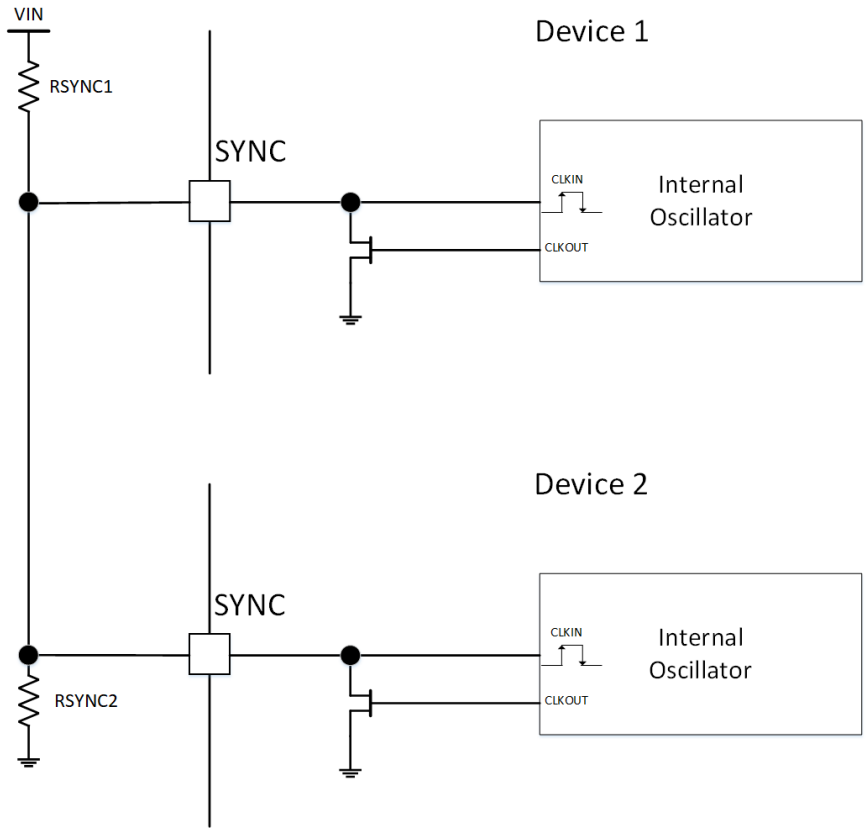


Figure 39. Sync Connections for Parallel Operation without External Clock

Parallel Operation with a Common External Clock

In parallel operation of multiple PE24108s with a common external clock, the SYNC pin should be connected to a common external pull-up resistor. Initially on power-up, the devices synchronize to the fastest of the internal clocks. When the external clock is applied after initial power-up, it needs to clock the SYNC pin at faster than 1600 KHz, and then all the parts will synchronize their internal oscillators to this frequency.

RSYNC1 and RSYNC2 should be of the same value to bias the SYNC pin at 50% of VIN.

If the external clock is at a peak-to-peak voltage of V_{IN}, RSYNC2 is optional. For lower output voltage external clocks, it should be placed to ensure that the SYNC pin is at $V_{IN}/2$.

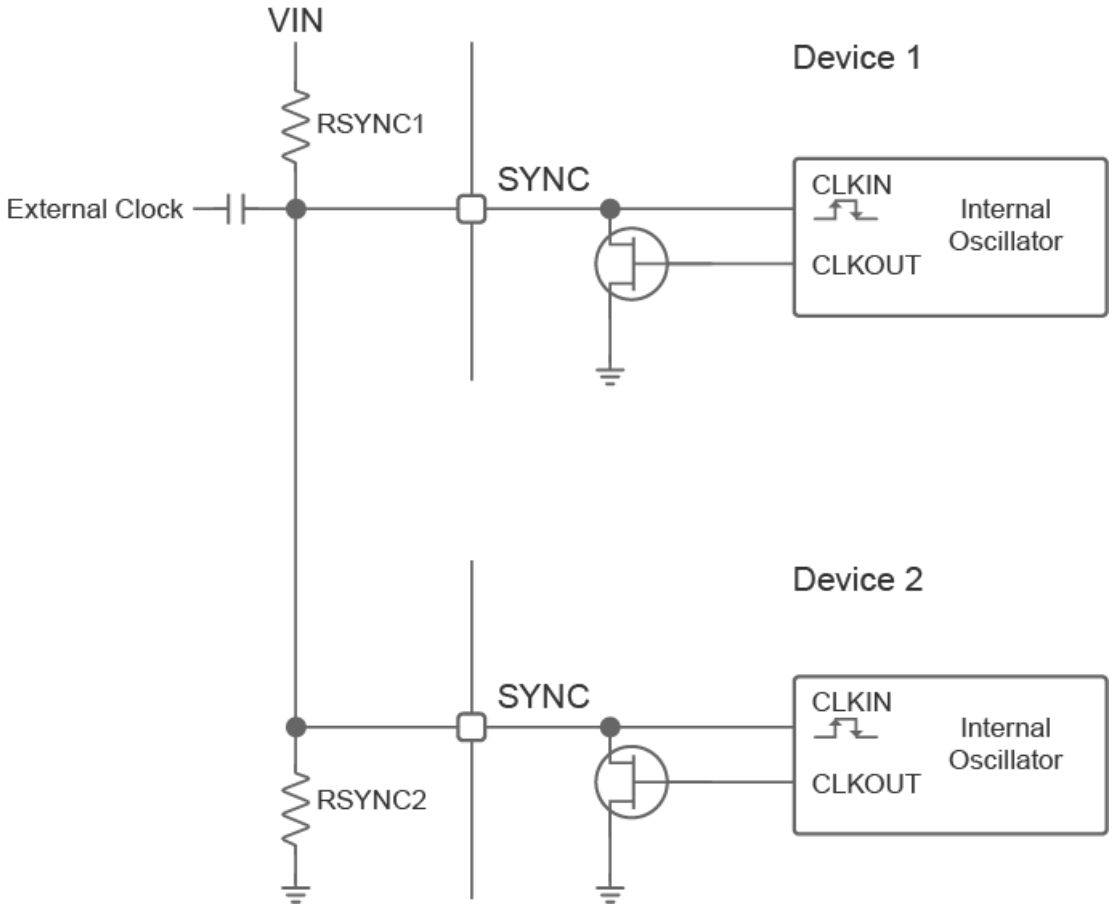


Figure 40. SYNC Connections for Parallel Operation with Common External Clock

Adjusting the Output Voltage AVS

The output voltage of the PE24108 is set externally by the resistor network into the feedback pin. This voltage can be adjusted externally by using a DAC and feeding the adjustment into the feedback node to scale the output voltage to optimize performance for low-voltage core supplies. In parallel operation, only one DAC is required to adjust the feedback node. All other FB pins should be tied together.

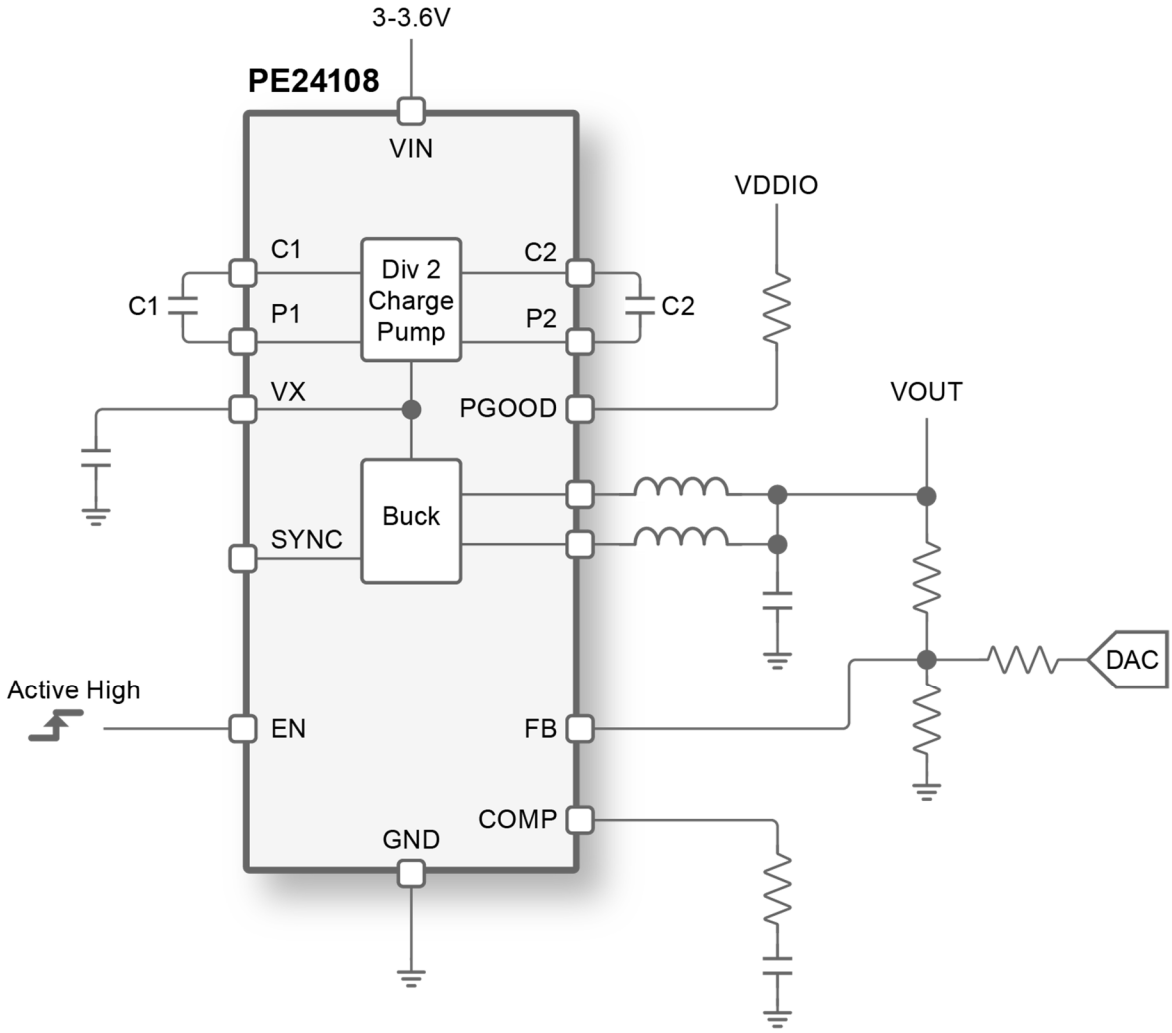


Figure 41. Adjusting the Output Voltage with External DAC

Application Schematic

An applications evaluation board was used to obtain the results in this datasheet. The schematic for a single device is shown in Figure 42, and the assembled evaluation board is shown in Figure 43. Table 7 lists some key recommended Murata passive components that are critical to achieving similar performance. The parts list shows the components required for a single populated device.

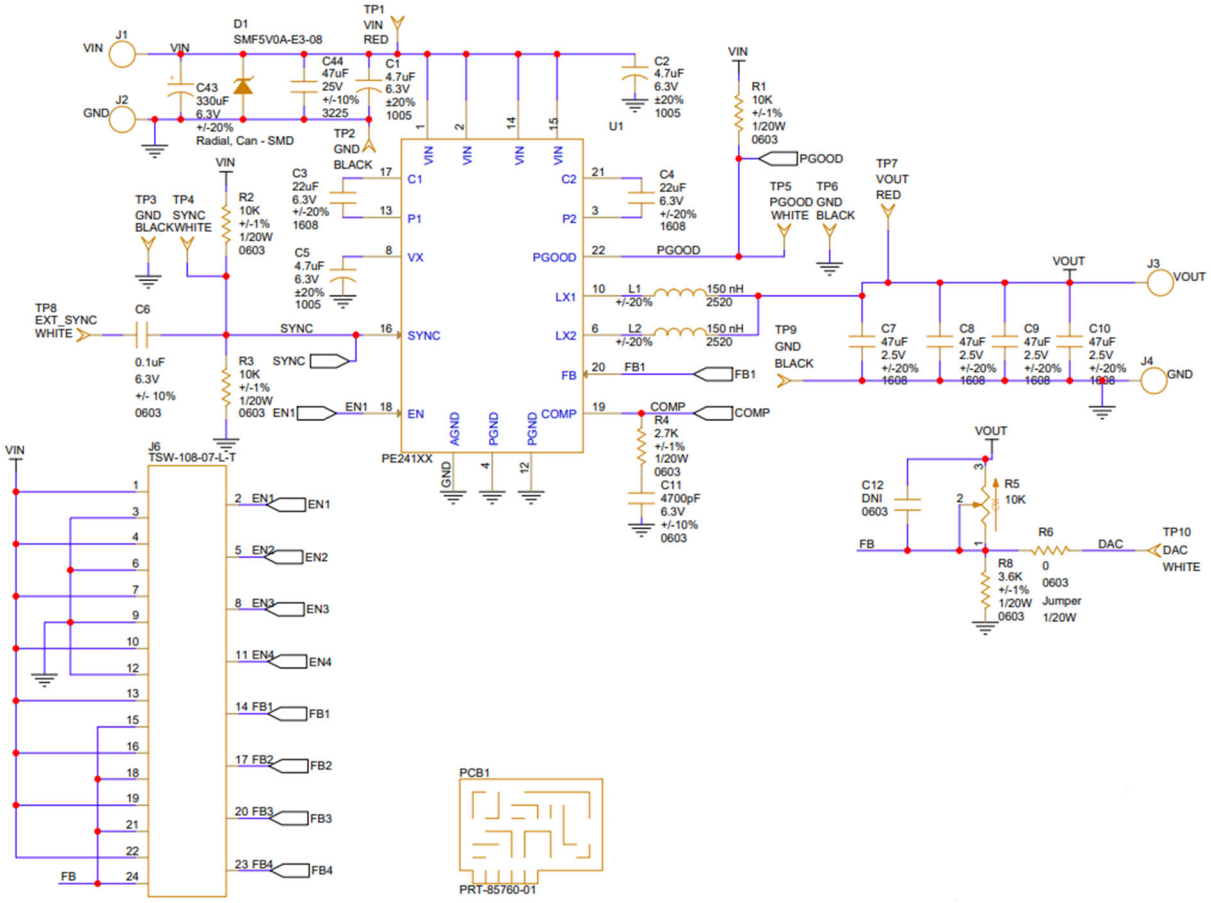


Figure 42. Device Board (EVK) Application Schematic

Evaluation Board

The PE24108 evaluation board is specifically designed for space-limited applications. The high-density, single-sided approach allows proximity of critical components while keeping traces short to reduce resistive power loss and maximize efficiency. The four-layer board is fabricated on FR4 using a minimum of one ounce of copper on each layer.

Each VIN pin on opposite sides of the PE24108 IC are connected to decoupling capacitors. Due to the solution size restrictions of the layout, a power plane is used to connect the IC to the decoupling capacitors to reduce leakage inductance. A PGND layer connected to and under the decoupling capacitors allows for a small power loop.

The inductors are placed close to the LX pins and connected directly to the output capacitors. The output pad is maximized and routed to the bottom layers using an array of vias to reduce inductance. PGND plane is placed under the output components and fed back to the IC on layer 2 to minimize the ground return path. This approach allows the application load to be placed directly under the PE24108 to reduce power losses.

The charge pump capacitors are placed close to the IC and connected to the flying capacitor pins (C1 and C2) and phase pins (P1 and P2) with wide traces to support the constant flow of energy supplied to the buck converter. The VX decoupling capacitor is placed close to the VX pin and bypassed to PGND to reduce charge pump ripple.

The backside of the evaluation board has an area where solder bridges are required to connect the outputs together for parallel operation. Combining the outputs together to the VOUT plane reduces the output resistance to the VOUT jacks.

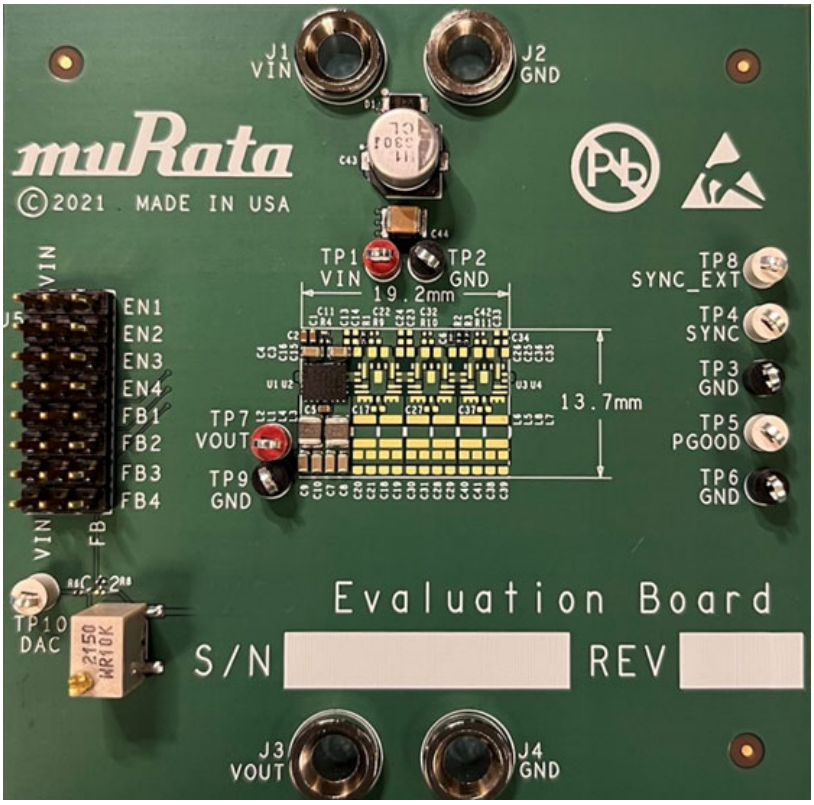


Figure 43. Device Board (EVK)

Application Circuit Part List

Table 7 lists recommended part numbers.

Table 7. Recommended Parts

Qty.	Ref. Number	Value	Description	Mfg.	Mfg. Part Number
3	C1,C2,C5	4.7 µF	CAP, SMD, CER, 4.7 µF, 6.3V, ±20%, X6S, 0402 (1005 Metric)	Murata	GRM155C80J475MEAAD
2	C3,C4	22 µF	CAP, SMD, CER, 22 µF, 6.3V, ±20%, X6S, 0603 (1608 Metric)	Murata	GRM188C80J226ME15D
1	C6	0.1 µF	CAP, SMD, CER, 0.1 µF, 6.3V, ± 10%, X6S, 0201 (0603 Metric)	Murata	GRM033C80J104KE15D
4	C7,C8,C9,C 10	47 µF	CAP, SMD, CER, 47 µF, 2.5V, ±20%, X7T, 0603 (1608 Metric)	Murata	GRM188D70E476ME01D
1	C11	4700 pF	CAP, SMD, CER, 4700 pF, 6.3V, ±10%, X7R, 0201 (0603 metric)	Murata	GRM033R70J472KA01D
1	C12	DNI	DNI		
1	C43	330 µF	CAP, SMD, ALU, 330 µF, 6.3V, ±20%, -, 0.248" Dia (6.30mm)	Nichicon	UCL0J331MCL1GS
1	C44	47 µF	CAP, SMD, CER, 47 µF, 25V, ±10%, X7R, 1210 (3225 Metric)	Murata	GRM32ER70J476KE20L
1	D1		19V (Typ) Clamp 20A (8/20 µs) Ipp Tvs Diode Surface Mount SOD-323	Bourns Inc.	CDSOD323-T03
2	L1,L2	150 nH	IND, SMD, Fixed Inductors, TFM-ALMA, 150 nH, 7.3A, 11 mOhm Max, 1008 (2520 Metric)	TDK	TFM252012ALMAR15MTAA
3	R1,R2,R3	10K	RES, SMD, Thick Film, 10K, ±1%, 1/20W, 0201 (0603 Metric)	Panasonic	ERJ-1GNF1002C
1	R4	2.7 kOhms	2.7 kOhms ±1% 0.05W, 1/20W Chip Resistor 0201 (0603 Metric) Moisture Resistant Thick Film	Yageo	RC0201FR-072K7L
1	R5	10K	RES, SMD, Potentiometers, 10K, ±10%, 0.25W, 1/4W, 0.250" x 0.170" Face x 0.295" H (6.35mm × 4.32 mm × 7.49 mm)	TT Electronics/BI	84WR10KLFTR
1	R6	0	RES, SMD, Thick Film, 0, Jumper, 1/20W, 0201 (0603 Metric)	Panasonic	ERJ-1GN0R00C
1	R8	3.6K	RES, SMD, Thick Film, 3.6K, ±1%, 1/20W, 0201 (0603 metric)	Panasonic	ERJ-1GNF3601C
1	U1		IC, SMD, IC, QFN, 4mm × 3.25 mm	Murata	PE24108

Packaging Information

This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE24108 in the 4 × 3.25 × 0.55 mm QFN is MSL 1.

Package Drawing

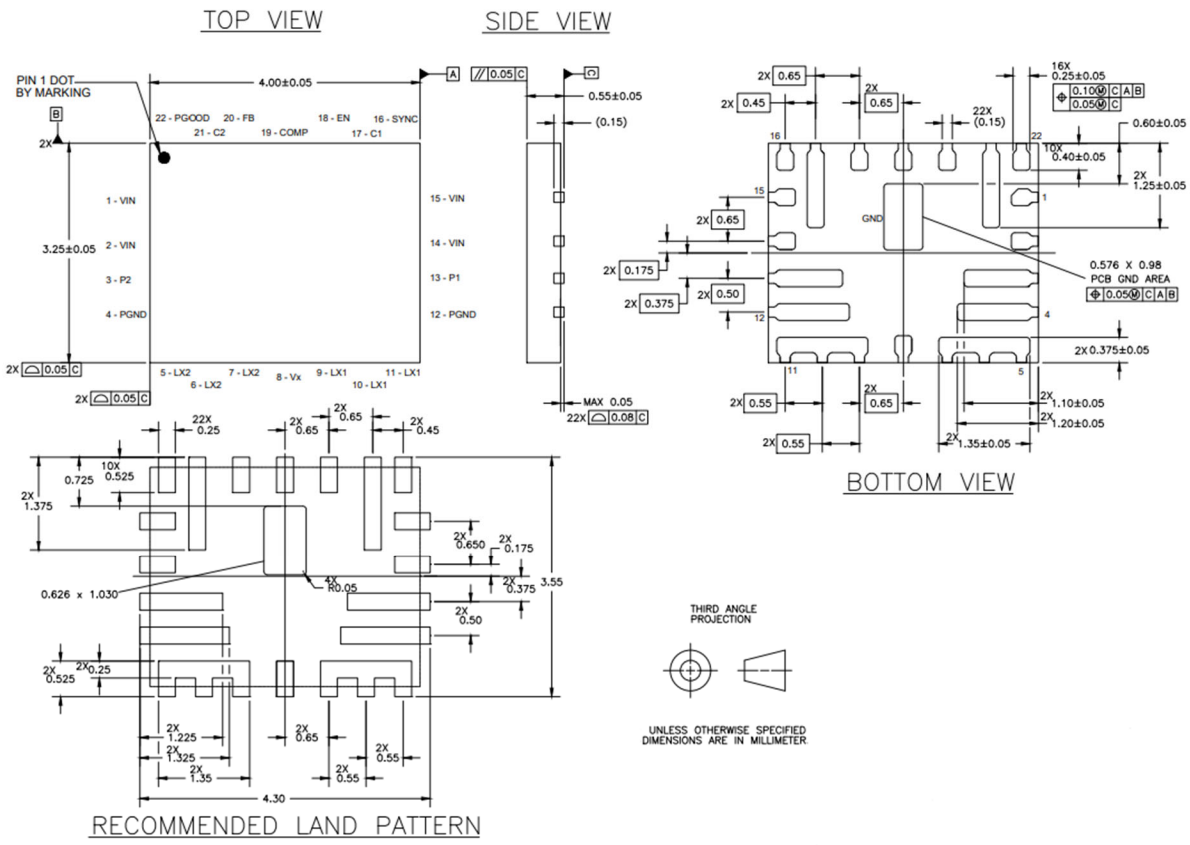


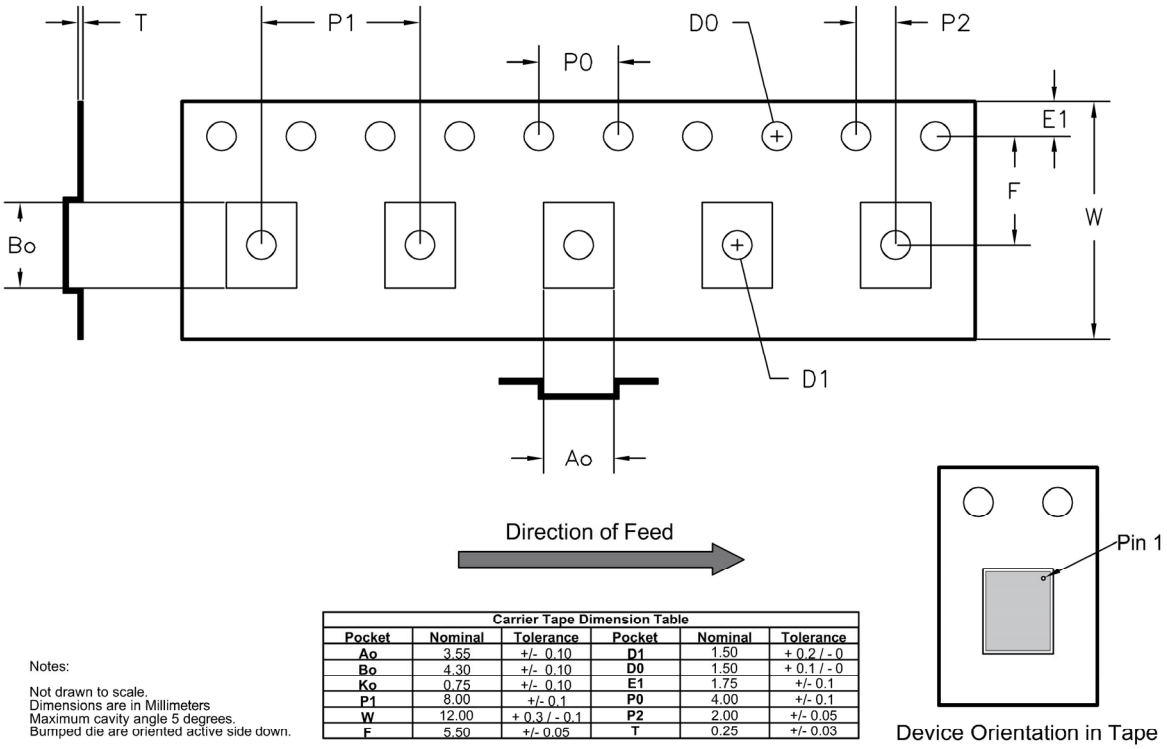
Figure 44. Package Drawing QFN 4 mm x 3.25 mm x 0.55 mm

Top Marking Specification

● = Pin 1 indicator
PPPPP = Product part number
YY = Last two digits of assembly year (2022 = 22)
WW = Assembly Work Week (01,02,03,...,52)
ZZZZZZ = Assembly lot code (maximum six characters)

Figure 45. Package Marking Specifications for PE24108

Tape and Reel Specification



Notes:

Not drawn to scale.
Dimensions are in Millimeters
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table

Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	3.55	+/- 0.10	D1	1.50	+ 0.2 / - 0
Bo	4.30	+/- 0.10	D0	1.50	+ 0.1 / - 0
Ko	0.75	+/- 0.10	E1	1.75	+/- 0.1
P1	8.00	+/- 0.1	P0	4.00	+/- 0.1
W	12.00	+ 0.3 / - 0.1	P2	2.00	+/- 0.05
F	5.50	+/- 0.05	T	0.25	+/- 0.03

Figure 46. Tape and Reel specifications

Order Codes

Table 8 lists the available ordering codes for the PE24108 as well as available shipping methods.

Table 8. Order Codes

Order Codes	Description	Packaging	Shipping Method
PE24108A-X	10A buck regulator	QFN on tape and reel	500 Units / T&R
PE24108A-Z	10A buck regulator	QFN on tape and reel	3000 Units / T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

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For additional information, contact Sales at sales@psemi.com.

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