PE25200

Document Category: Product Specification

Divide-by-2 and -3, 10A Charge Pump, Capacitor Divider

General Description

The PE25200 is an ultra-high efficiency charge pump that is configurable to divide down an input voltage by two or three and deliver up to 45 watts at 97% peak efficiency.

The PE25200 supports an input voltage range of 5.5V to 10V in divide-by-two mode and 8.2V to 15V in divide-by-three mode.

Features

- Proprietary architecture enables industry leading efficiency with an ultra-low profile
- Wide input voltage range, from 5.5V to 15V, supports two- or three-cell mobile computers and 12V-bus point-of-load applications
- Peak efficiency of 97.9%
- Pin-selectable cycle skipping mode for improved light load efficiency
- Configurable in either divide-by-two or -three modes
- Low EMI fixed-frequency operation under heavy load conditions
- Fully protected input under-voltage, output overcurrent, and thermal shutdown

Typical Applications

- Two-cell and three-cell lithium platforms
- Ultrabook and notebook computers
- Full-size tablet computers
- Ultra-thin form factor designs
- $12V_{IN}$ point-of-load designs in networking and telecommunications

Efficiency

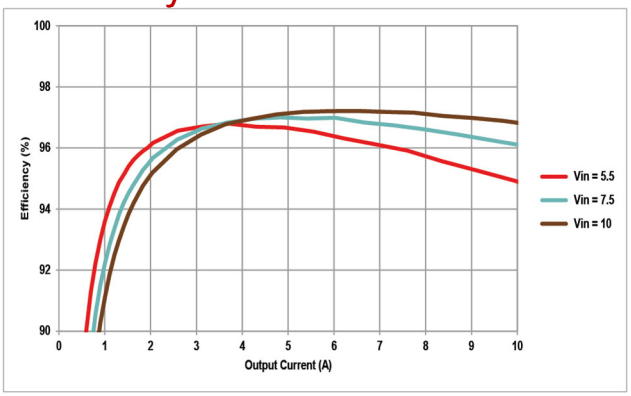


Figure 1. Typical Efficiency in Divide-by-Two and Fixed Frequency Mode

Simplified Application

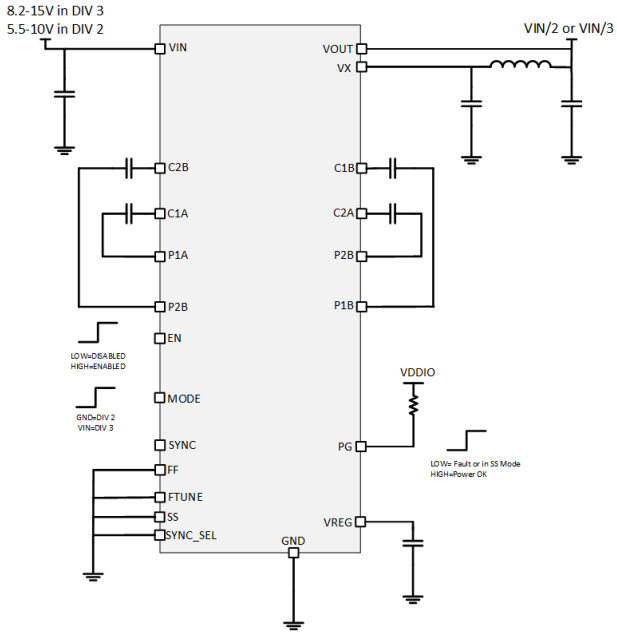


Figure 2. Application Schematic Showing Device Configured in Divide-by-Two Mode, Fixed Frequency, with a 0.1A Soft Start

Contents

Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the maximum operating range and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. PE25200 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Input voltage, divide-by-3 mode	-0.3	16.7	V
Input voltage, divide-by-2 mode	-0.3	11.2	V
Input voltage, transient (< 50 ms)	–	18.8	
Enable range	-0.3	V_{IN} + 0.3	
Output voltage, V_{OUT}	-0.3	5.57	V
Output current(1)	0	20	A
Storage temperature	-65.0	150.0	°C
Junction temperature	-40.0	150.0	°C
Operating bump or lead temperature	–	260.0	°C
EN, FF, SS, MODE, SYNCSEL, FTUNE, and PGOOD	-0.3	V_{DD} + 0.3	V
CLKSYNC	-0.3	V_{IN} + 0.3	V
Human body model, all pins(2)	–	± 1500	V
Charged device model, all pins(3)	–	± 1000	V

Notes:
1. Tested with a DC current of 20A.
2. Human Body Model, all pins (Joint JEDEC/ESDA Human Body Model (JS-001-2017)).
3. Charged Device Model, all pins (Joint JEDEC/ESDA Charged Device Model (JS-002-2018)).

Recommended Operating Conditions

Table 2 lists the PE25200 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE25200 Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{IN} input voltage range, relative to GND, V_{IN}, in divide-by-3 mode	8.2	15	V
V_{IN} input voltage range, relative to GND, V_{IN}, in divide-by-2 mode	5.5	10	V
Junction temperature range, T_J	-40.0	125.0	°C

Package Thermal Characteristics

Table 3. Package Thermal Characteristics(*)

Parameter	Condition	Min	Max	Unit
Maximum junction temperature	Measured at max ambient temperature (T_A) and max power dissipation.	–	150.0	°C
Junction-to-case top thermal resistance (ΘJt)	JEDEC JESD51-12-01 and JESD15-3	0.1	–	°C/W
Junction-to-board thermal resistance (ΘJb)	JEDEC JESD51-12-01 and JESD15-3	3	–	°C/W
Junction-to-board thermal characterization (ΨJB)	–	2.1	–	°C/W

Note:
* Package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-12. See also pSemi Application Note 57, *Thermal Characterization*.

Electrical Characteristics

Table 4 lists the PE25200 key electrical specifications at the following conditions, unless otherwise noted:

- V_{IN} = 5.5V to 10V, MODE = GND, T_J = -40 °C to +125 °C, FTUNE = GND
- V_{IN} = 8.2V to 15V, MODE = V_{IN}, T_J = -40 °C to +125 °C, FTUNE = GND

Table 4. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input voltage range						
Input voltage range	V_{IN}	MODE = GND (V_{OUT} = V_{IN}/2)	5.5	–	10	V
		MODE = V_{IN} (V_{OUT} = V_{IN}/3)	8.2	–	15	V
V_{IN} under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{IN} rising [MODE = GND (V_{OUT} = V_{IN}/2)]	–	–	4.5	V
		V_{IN} rising [MODE = V_{IN} (V_{OUT} = V_{IN}/3)]	–	–	8	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	–	–	150	–	mV
Output current						
Maximum output current	I_{LOAD}	–	10	–	–	A
Output current limit	I_{LIM}	MODE = GND (V_{OUT} = V_{IN}/2)	13.1	–	28.5	A
Supply current						
Operating supply current	I_{VIN}	I_{LOAD} = 0A, FF= Float (@MAX V_{IN}) @ 25 °C	–	8.5	–	mA
		I_{LOAD} = 0A, FF = GND (@MAX V_{IN}) @ 25 °C	–	47	–	
		I_{LOAD} = 0A, FF = V_{IN} (@MAX V_{IN}) @ 25 °C	–	8.7	–	
Shutdown supply current	I_{VIN_SD}	EN = GND @ 25 °C	–	2.65	6.0	µA
Full-load switching frequency typical setting(1)	F_{SW_FL}	FF = GND	450	500	550	kHz
Nominal output voltage	V_{O_NOM}	MODE = GND	–	V_{IN}/2	–	V
		MODE = V_{IN}	–	V_{IN}/3	–	V
Soft-start input current limit	I_{SS_LIM}	SS = GND	0.1	0.21	0.42	A
		SS = Float	0.1	0.63	1.14	A
		SS = V_{IN}	0.27	1.2	2.13	A
V_{OUT} under-voltage protection threshold	V_{UVP}	MODE = GND (V_{OUT} = V_{IN}/2)	0.77 × V_{IN}/2	0.8 × V_{IN}/2	0.87 × V_{IN}/2	V
		MODE = V_{IN} (V_{OUT} = V_{IN}/3)	0.77 × V_{IN}/3	0.8 × V_{IN}/3	0.87 × V_{IN}/3	V
V_{OUT_UVP} glitch suppression	T_{UVP}	V_{OUT} must be less than V_{UVP} for longer than T_{UVP} to trigger fault	1.5	1.7	1.9	µs
Vx over-voltage protection	V_{XOVP}	–	5.87	6.0	–	V
Thermal shutdown threshold	T_{TSD}	–	125	140	–	°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal shutdown hysteresis	T_{TSD_HYST}	–	–	12.8	–	°C
Maximum soft-start timeout duration	–	SS = GND	–	80	–	ms
CLKSYNC pin input frequency	f_{SYNC}	Charge-pump switching frequency is 0.5 * CLKSYNC pin frequency. Frequency applied outside this range could cause improper behavior.	0.625	–	1	MHz
Power good (PGOOD) pin						
Pull-down resistance	R_{PGOOD}	I_{SINK} = 15 mA	–	–	18.5	Ω
PGOOD rising threshold	PG_{TH}	–	–	1.3	–	V
PGOOD hysteresis	PG_{HYS}	–	–	160	–	mV
Output leakage	–	V_{OUT} > PG_{TH}	–	–	15	µA
Time for PGOOD detect	$PGOOD_{DETECT}$	Time from falling edge of PGOOD to PE25200 no longer able to support full load.	–	10.0	–	µs
V_{REG} output voltage[2]	V_{REG}	Used as max for the CLKSYNC pin.	–	4.0	–	V
Logic levels EN						
Input high voltage	V_{IH}	–	1.2	–	–	V
Input low voltage	V_{IL}	–	–	–	0.4	V
Input current	I_{EN}	EN = 15V	–	–	11	µA
Logic levels CLKSYNC						
Input high voltage	V_{IH}	–	1.2	–	–	V
Input low voltage	V_{IL}	–	–	–	0.4	V
Input current	I_{EN}	V_{IH} = 3.3V	–	–	1.0	µA
MODE, FF, SS, FTUNE, and SYNCSEL input current	–	V_{IH} = 15V	–	–	1.0	µA

Notes:
1. Minimum and maximum specifications are 100% production tested at $T_A = T_J$ = 25 °C unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Thermal shutdown is not production tested.

Pin Configuration

Figure 3 shows the PE25200 pin map for the 6.850 mm × 4.450 mm × 0.492 mm WLCSP, and Table 5 lists the description for each pin.

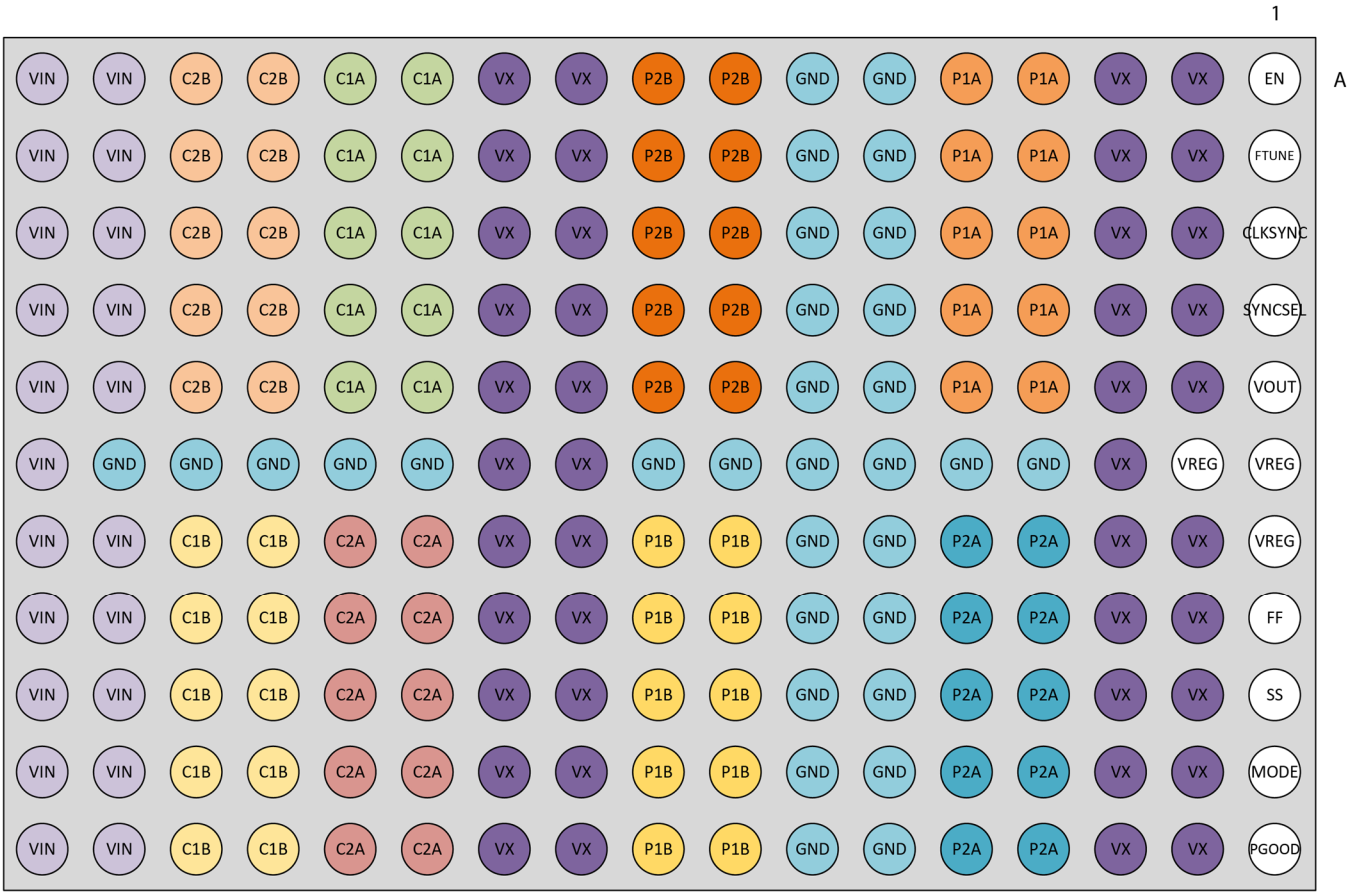


Figure 3. PE25200 Pin Configuration (Bottom View)

Pin Descriptions

Table 5. Pin Descriptions

Pin number	Name	Description
G15, G14, H15, H14, I15, I14, J15, J14, K15, K14	C1B	Flying capacitor C1B positive terminal
A15, A14, B15, B14, C15, C14, D15, D14, E15, E14	C2B	Flying capacitor C2B positive terminal
A13, A12, B13, B12, C13, C12, D13, D12, E13, E12	C1A	Flying capacitor C1A positive terminal
C1	C2A	Flying capacitor C2A positive terminal
A1	CLKSYNC	Clock output or sync pin input. Select the function with the SYNCSEL pin.
H1	EN	Part enable. Connect to VIN if not used.
B1	FF	Selects the charge pump clock mode: ▪ GND = fixed frequency ▪ Float = cycle skipping ▪ V_{IN} = asynchronous mode
F9, F8, F5, F4, F12-16, A-K7, A-K6	GND	Power ground. Connect to the ground plane.
J1	MODE	Selects the charge pump voltage division ratio: ▪ MODE = V_{IN} for divide-by-three mode ▪ MODE = GND for divide-by-two mode This pin must not float.
G8, G9, H8, H9, I8, I9, J8, J9, K8, K9	P1B	Flying capacitor C1B negative terminal
A9, B9, C9, D9, E9, A8, B8, C8, D8, E8	P2B	Flying capacitor C2B negative terminal
A5, B5, C5, D5, E5, A4, B4, C4, D4, E4	P1A	Flying capacitor C1A negative terminal
G5, H5, I5, J5, K5, G4, H4, I4, J4, K4	P2A	Flying capacitor C2A negative terminal
K1	PGOOD	Open-drain power-good signal/multi-device input
I1	SS	Selects the soft-start current: ▪ GND = 0.6A ▪ Float = 1.1A ▪ V_{IN} = 2.1A
D1	SYNCSEL	Controls the CLKSYNC pin input: ▪ GND = clock output ▪ Float = CLKSYNC disabled ▪ V_{IN} = sync input
A-K17, A-E16, G-K16	VIN	Input voltage
E1	VOUT	Sensed output voltage, connect to filtered version of VX.
F1, F2, G1	VREG	Internal LDO output voltage
A-K3, A-E2, G-K2, A-K10, A-K11	VX	Output voltage

Functional Block Diagram

The PE25200 uses proprietary charge pump technology to deliver superior efficiency in a fully integrated WLCSP.

The PE25200 provides the following protection features to ensure robust system operation:

- Input under-voltage lockout (UVLO)
- Thermal shutdown (TSD)
- Over-current protection (OCP)
- Output under-voltage protection (UVP)
- Output over-voltage protection (VX OVP)
- Soft-start timeout (SST)

Figure 4 shows the PE25200 functional block diagram.

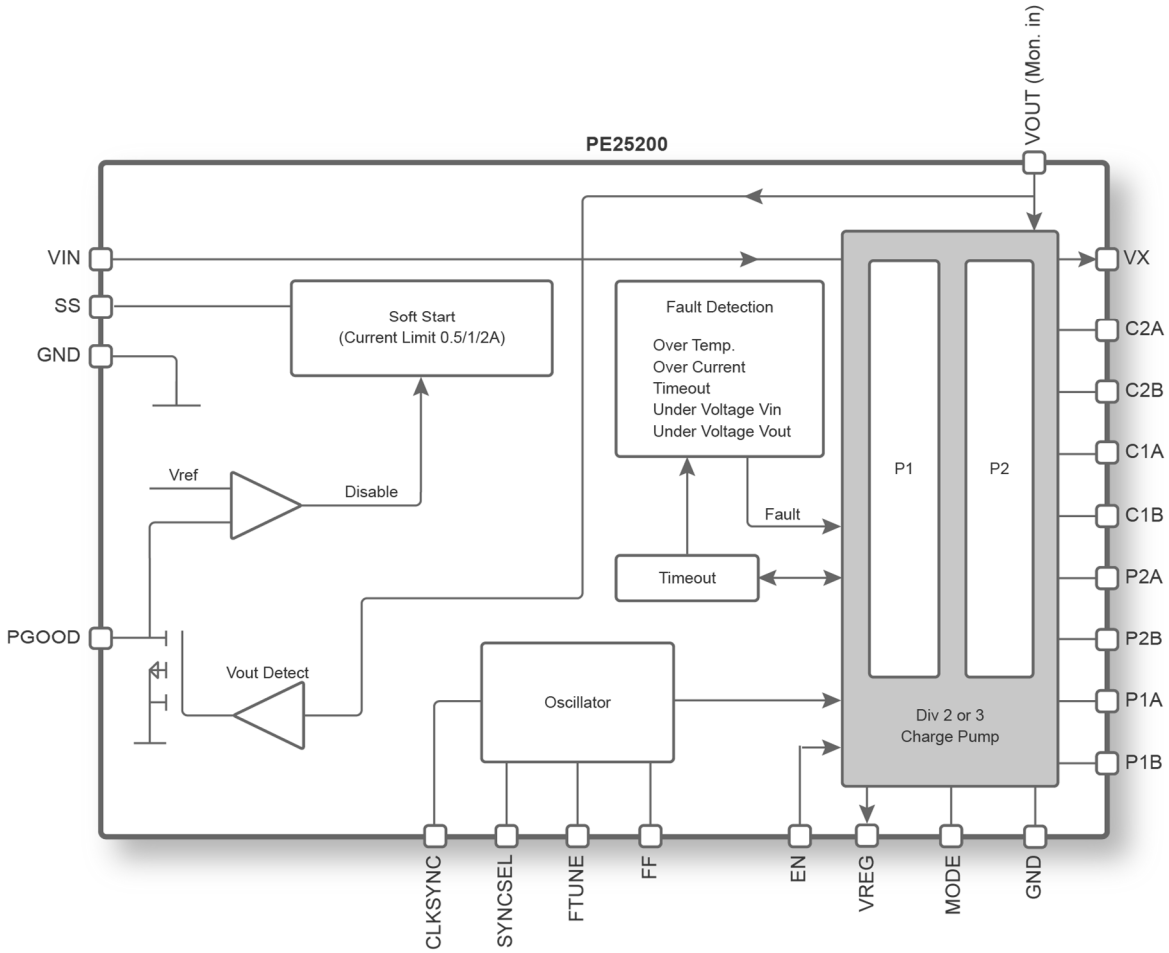


Figure 4. PE25200 Functional Diagram

Application Circuit

Figure 5 shows a typical application circuit configured to operate in divide-by-2 and divide-by-3 modes. For the specific component values, see the Application Information on page 28.

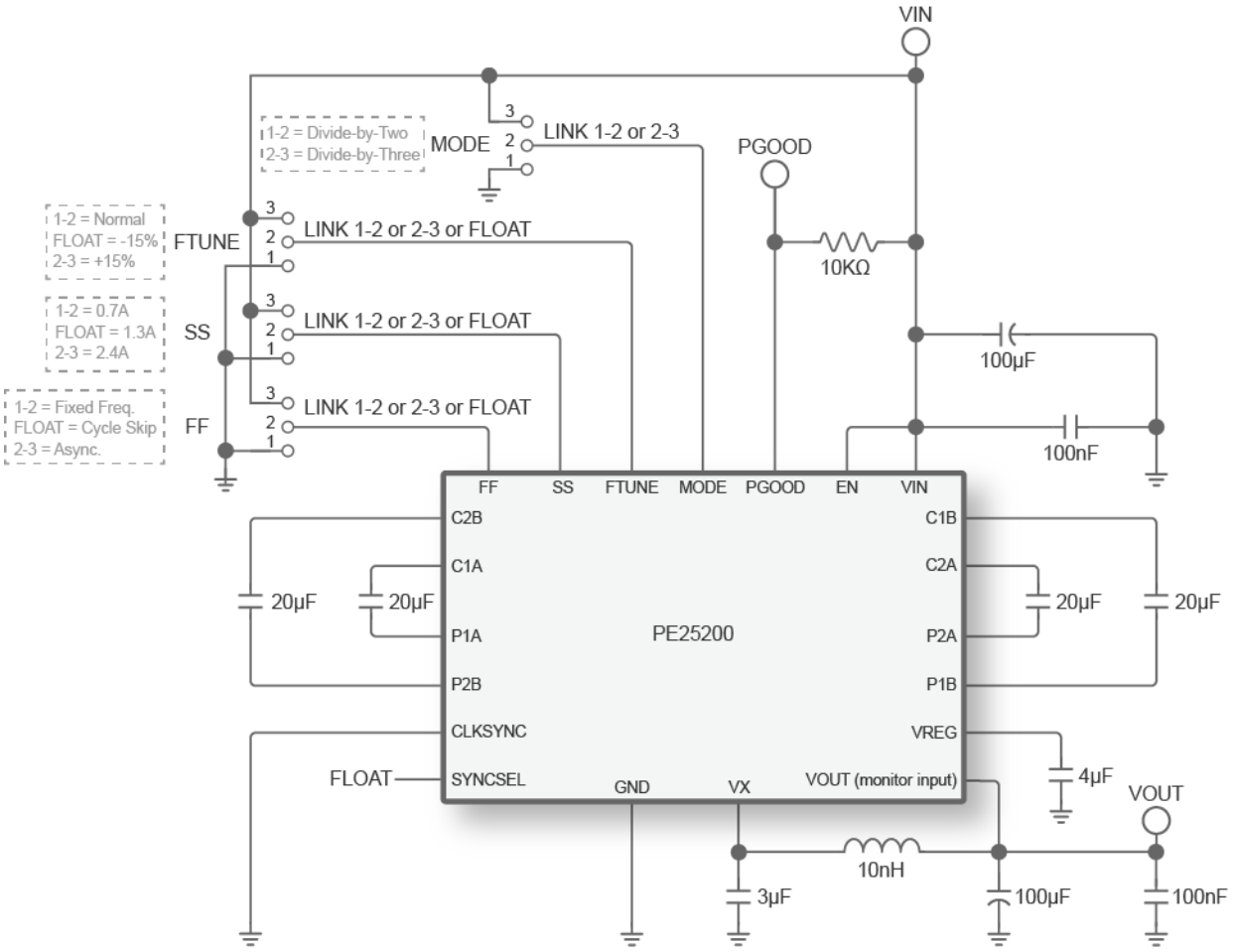


Figure 5. Simplified Application Circuit

Typical Performance Characteristics

Figure 6–Figure 24 show the PE25200 typical operating performance data. In each case, the figures show performance with FTUNE = GND.

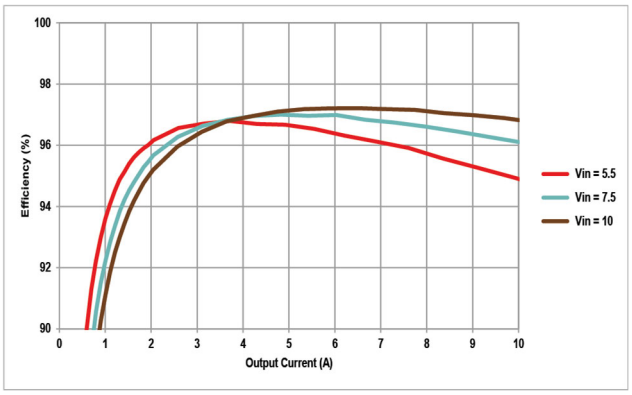


Figure 6. Efficiency vs. Load Current Fixed Frequency, DIV2, 25 °C

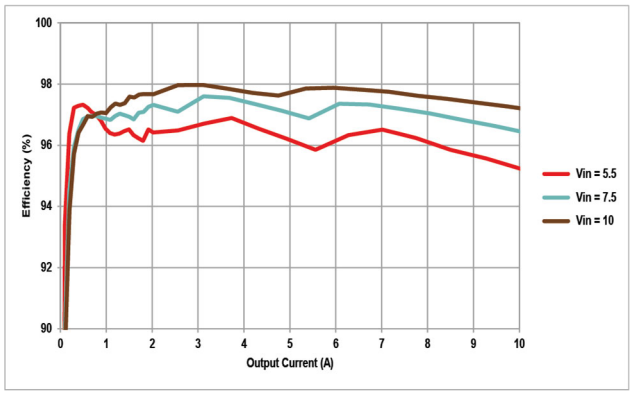


Figure 7. Efficiency vs. Load Current Cycle Skipping, DIV2, 25 °C

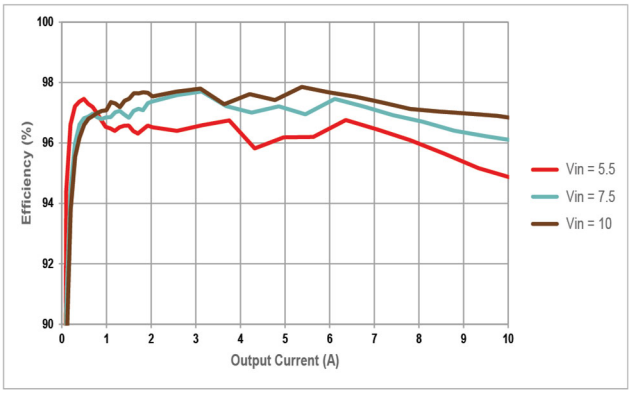


Figure 8. Efficiency vs. Load Current Asynchronous, DIV2, 25 °C

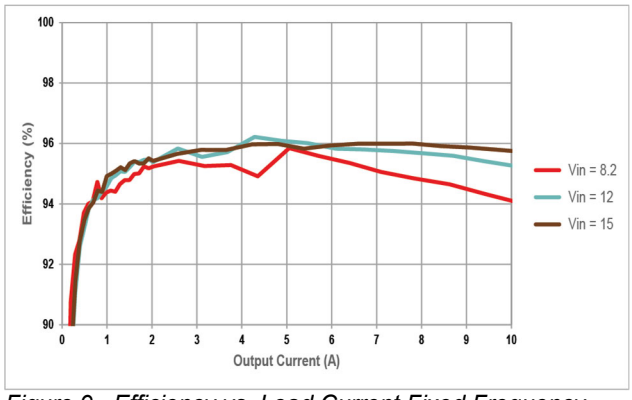


Figure 9. Efficiency vs. Load Current Fixed Frequency, DIV3, 25 °C

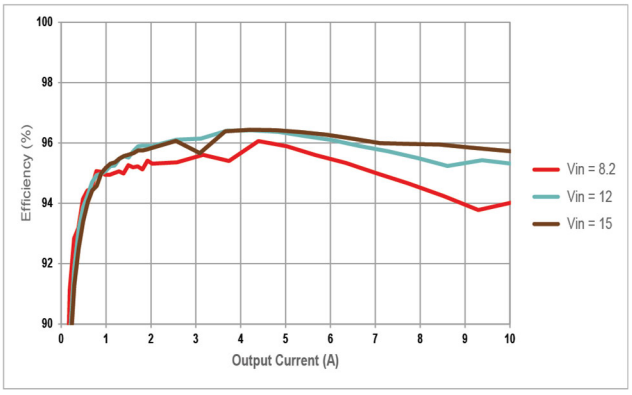


Figure 10. Efficiency vs Load Current Cycle Skipping, DIV3, 25 °C

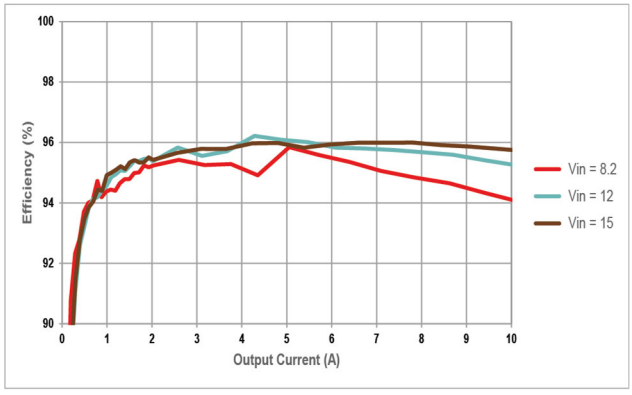


Figure 11. Efficiency vs Load Current Asynchronous, DIV3, 25 °C

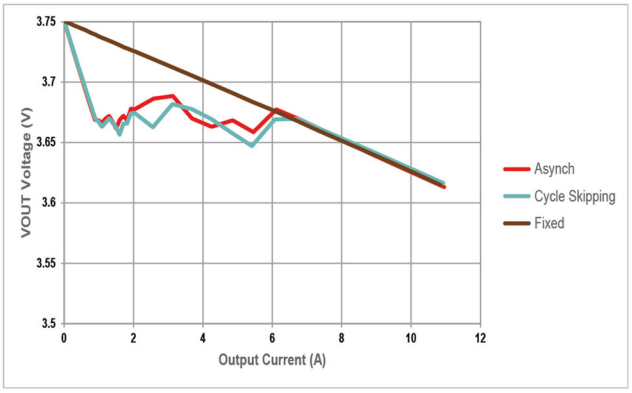


Figure 12. V_{OUT} vs. Load Current DIV2, 25 °C, V_{IN} = 7.5V

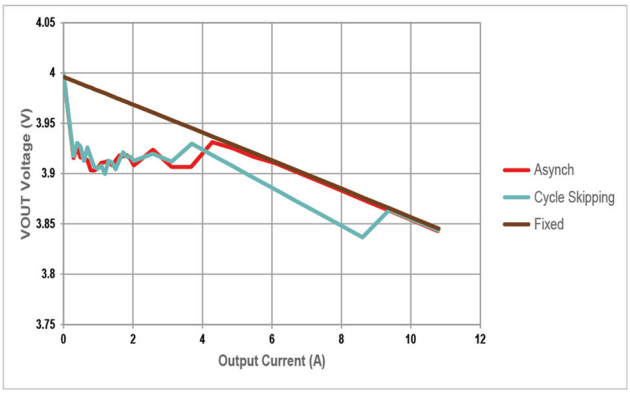


Figure 13. V_{OUT} vs. Load Current DIV3, 25 °C, V_{IN} = 12.0V

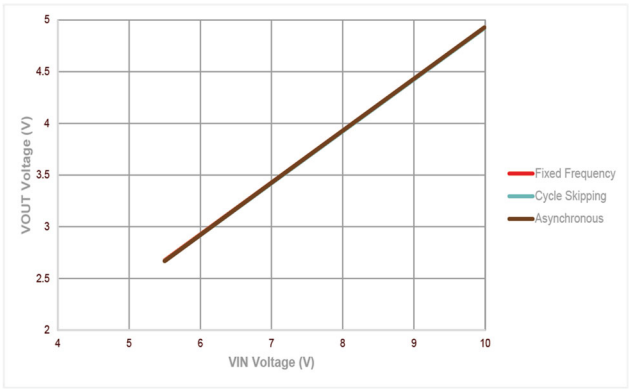


Figure 14. V_{OUT} vs. V_{IN} DIV2, 25 °C, 5A Load Current

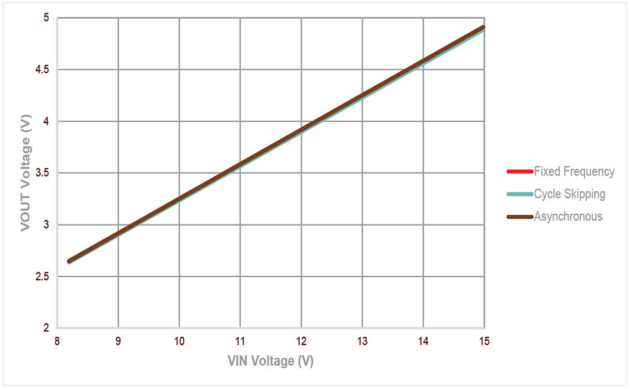


Figure 15. V_{OUT} vs. V_{IN} DIV3, 25 °C, 5A Load Current

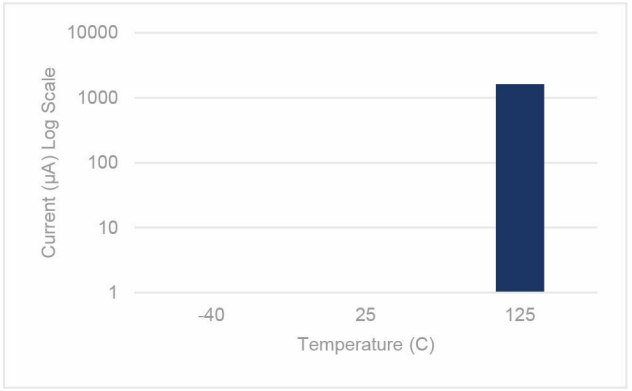


Figure 16. Shutdown Current vs. Temperature, DIV3, V_{IN} = 15V

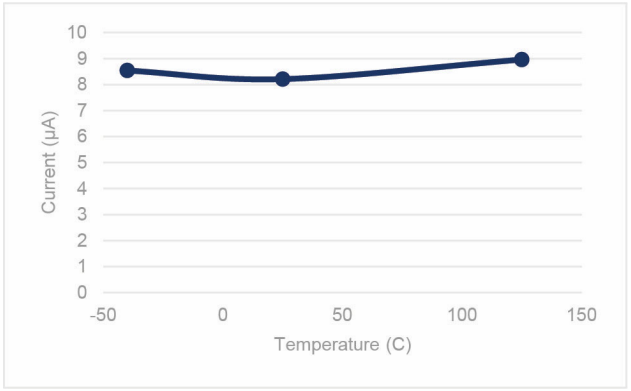


Figure 17. EN Pin Input Leakage Current vs. Temperature, EN = 15V

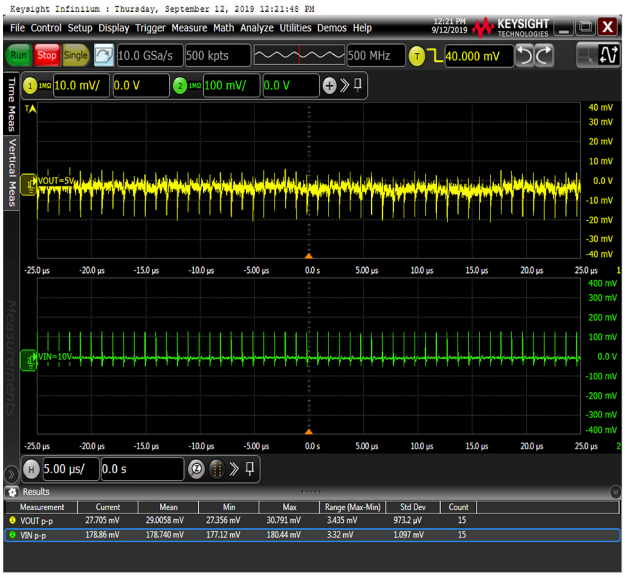


Figure 18. DIV2 Ripple @ I_{LOAD} = 10A(*)

Figure 19. DIV3 Ripple @ I_{LOAD} = 10A(*)

Figure 20. DIV2 Soft Start

Figure 21. DIV2 Soft Start from Cold, Zoomed-in

Figure 22. DIV2 Soft Start, Zoomed-in

Figure 23. DIV3 Soft Start

Figure 24. DIV3 Soft Start, Zoomed-in

Note:

* Using the EVK (see the Figure 29 schematic) with corresponding, defined capacitances: fixed-frequency mode, into the full 10A load.

Detailed Description

The PE25200 is a dual-phase, charge pump-based, DC-DC converter designed to operate in fixed divide-by-two or divide-by-three modes. The supported output voltage range is from 2.75V to 5.0V with load currents of up to 10A and up to 45W delivered to the external load. You can configure the charge pump to operate in a range of clocking modes to allow easier optimization of EMI vs. efficiency for the target application.

To set the device configuration, connect the following pins to VIN, GND, or leaving the pin floating:

- FF
- SS
- FTUNE
- SYNCSEL

The MODE pin is slightly different and must only be connected to VIN or GND. The pin configurability is designed to minimize the external components needed to reduce the cost of the total solution. The configuration pin values are sampled once when the PE25200 starts up, and before the charge pump power stage is enabled. The configuration pins are not designed to be driven dynamically.

Startup: The EN, VIN, and VREG Relationship

The PE25200 enable input pin, EN, was designed to be compatible with typical low-voltage digital I/O levels so that it can be easily driven by an external controller. EN can also be connected to the VIN pin if external power sequencing or control is not needed.

If the EN pin is held low until VIN has reached its nominal voltage, the PE25200 follows the initialization sequence shown in Figure 25.

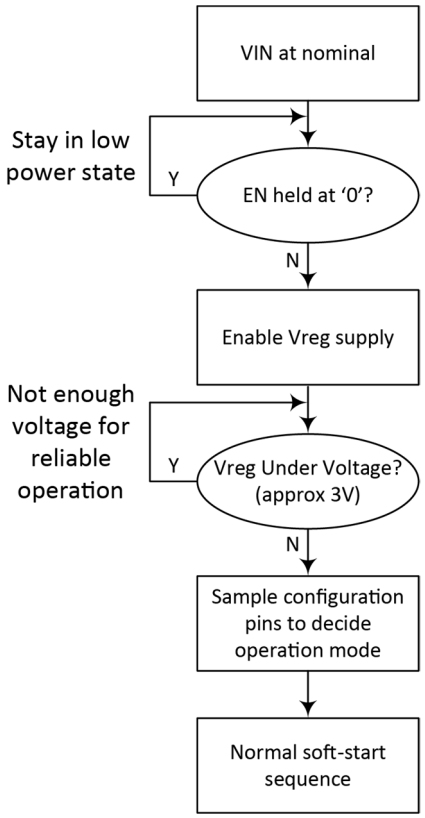


Figure 25. EN-controlled Startup Flow

When the EN pin is connected to VIN, and VIN ramps quickly, the start-up sequence is like Figure 25. This is because of the external capacitor connected at VREG, which means that VIN likely reaches nominal voltage levels before VREG reaches its target voltage.

Figure 21 shows the fast start-up sequence expected when starting without charge in the system.

If a slow ramp for VIN—and EN connected to VIN—occurs, extra states might be seen as listed in Table 6Table 7 because now the VREG voltage tends to track (a slow changing) VIN more closely.

Table 6. PE25200 Supply Voltage Sequence

VIN voltage	EN voltage	VREG state	PE25200 state
0V	0V	Disabled	Unpowered
Below approx. 3.0V	Less than V_{IL}	Disabled	Lowest power disabled state
Between 3.0V and V_{UVLO_H}	Less than V_{IL}	Disabled	Lowest power disabled state
Higher than V_{UVLO_H}	Less than V_{IL}	Disabled	Lowest power disabled state
Below approx. 3.0V	Higher than V_{IH}	Ramps with VIN, but most other internal circuits remain disabled.	▪ Some internal circuitry is waking up. ▪ Still in a low power state.
Between 3.0V and V_{UVLO_H}	Higher than V_{IH}	VREG is approximately the same as VIN until 4.0V.	▪ Internal circuits are starting up. ▪ Configuration pins are sampled. ▪ Charge pump power stage remains disabled.
Higher than V_{UVLO_H}	Higher than V_{IH}	4.0V	▪ Enabled. ▪ Capable of full power operation.

Soft-start and the SS Pin

The PE25200 is a high-power device. To protect the system and the PE25200 internal circuitry, power is supplied to the output and the flying capacitors in a controlled soft-start sequence. The soft-start current supplied to the load is sufficient to ramp VOUT to the target voltage in less than the soft-start timeout duration. You can configure the soft-start current level by connecting the SS pin to GND, VIN, or by leaving it floating, as shown in Table 7.

Table 7. Soft-start Current Truth Table

SS pin	Current limit
GND	0.2A
Float	0.6A
VIN	1.2A

Before enabling the soft-start current source, the PE25200 pre-charges the flying capacitors to their nominal voltage (VOUT or 2VOUT depending on the division ratio). If the VOUT voltage is pre-charged by an external source, for example, the flying capacitor pre-charge stage could add up to 40 ms additional delay to the PE25200 start-up time while the flying capacitors ramp to the target voltage. Figure 20 shows the delayed start-up that could be expected when starting the PE25200 with the charge still in the system.

The PE25200 exits the soft-start phase and transitions to full power switching mode when the VOUT voltage reaches within 5% of the target voltage. The power good (PGOOD) pin is allowed to go high at the same time. Figure 22 shows the small step in VOUT voltage from approximately 95% of target to 100% of target as the PE25200 leaves soft-start mode and enters full power.

Throughout soft-start, the PE25200 operates the charge pump in fixed frequency mode—regardless of how the FF pin is configured—to ensure a predictable power-up time.

Set the soft start current to the lowest level that reliably ramps VOUT in less than 10 ms. If VOUT is shorted, the soft-start current could cause considerable power dissipation in the PE25200. For VIN = 15V, VOUT = 0V, and a

2.1A soft-start current, the PE25200 could have to sustain >30W for up to 2.5 ms. The soft-start timeout value is based on ramping 100 µF to 5V using a 0.5A soft-start current.

Voltage Division and the MODE Pin

The PE25200 supports two divide ratios from VIN to VOUT: 2 or 3. You can configure the division ratio by connecting the MODE pin to GND or VIN, as listed in Table 8.

Table 8. MODE Pin

MODE pin	Division ratio
GND	Divide-by-two
VIN	Divide by-three

Do not leave the MODE pin to float If a board-level fault occurs. The charge pump is designed not to turn on for a floating MODE pin to reduce the risk of unplanned operation, such as starting in divide-by-two mode for a divide-by-three application.

The PE25200 implements all the power switches and switch control to operate in divide-by-two or divide-by-three mode. The same PCB design can support either mode, although the MODE pin is only sampled during start-up and it is not possible to swap division ratios dynamically. It is possible to achieve some small efficiency improvements when operating in divide-by-two if the C1B/C2A, and the C2B/C1A pins are shorted to each other at the PCB level. These shorts operate in parallel with internal power switches in the PE25200, decreasing switch impedance and slightly reducing losses as a result. The C1B/C2A and C2B/C1A pins are placed adjacent to each other on the PE25200 pin-out to make this board level connection easier for fixed divide-by-two applications.

Charge Pump Frequency and the FTUNE Pin

The PE25200 has a precision on-chip oscillator used for internal operations and to drive the charge pump output power stage. Typically, the oscillator frequency is fixed, leading to a charge pump clock frequency—while in fixed frequency mode—of 500 kHz.

To help with potential EMI issues, you can vary the oscillator frequency by ±15% using the FTUNE pin connections, as listed in Table 9. Like the other configuration pins, the FTUNE pin is not designed to be driven dynamically.

Table 9. FTUNE Operation

FTUNE pin	Frequency
GND	Nominal
Float	-15%
VIN	+15%

In fixed-frequency mode, varying the oscillator by ±15% also varies the charge pump clock frequency by ±15%. The timings in the EC table will also vary by ±5%.

The frequency control available using the FTUNE pin configuration is intended for EMI mitigation in the end application.

Clock Modes and the FF Pin

The PE25200 charge pump power stage supports three clock modes to allow flexibility in optimizing system issues, such as VOUT ripple, EMI considerations, and efficiency for a particular application. You can select the clock mode by connecting the FF pin to GND, VIN, or leaving it to float, as listed in Table 10.

Table 10. Frequency Mode Operation (FF)

FF pin	Frequency mode
GND	Fixed-frequency mode
Float	Cycle-skipping mode
VIN	Asynchronous mode

In fixed-frequency mode, the charge pump clocks at a fixed fraction of the on-chip precision oscillator. The nominal charge pump fixed frequency is 500 kHz. In fixed-frequency mode, only the FTUNE configuration pin connection varies the charge pump frequency, with three fixed frequencies possible depending on the FTUNE setting.

The PE25200 operates the charge pump in fixed-frequency mode, regardless of how the FF pin is connected, during soft-start. The clock mode set by the FF pin is used when PE25200 exits soft-start and throughout normal, fault-free operation.

Cycle skipping is a variant of fixed-frequency mode that can increase efficiency at light loads by allowing the voltage ripple at VX to increase slightly. Figure 26 shows an example of the two clock phases of the charge pump when operating in fixed-frequency and cycle-skipping modes.

A key feature of the cycle-skipping mode is that at low output loads, the charge pump switches at the normal (fixed frequency) clock intervals, so EMI filtering remains straightforward, but only when the voltage droop at VX requires more power to the load. As the load current increases, the cycle skipping mode becomes closer to fixed frequency, and at high loads there is no difference between fixed-frequency and cycle-skipping modes. As shown in Figure 26, at light loads the two phases of the charge pump might not be equal on a cycle-by-cycle basis, but if the flying capacitors have equal values and the load is constant, the two phases share the load equally on average.

In low or no-load conditions, a minimum switching frequency is applied in cycle skipping mode which ensures the charge pump always operates at a frequency above the audio band.

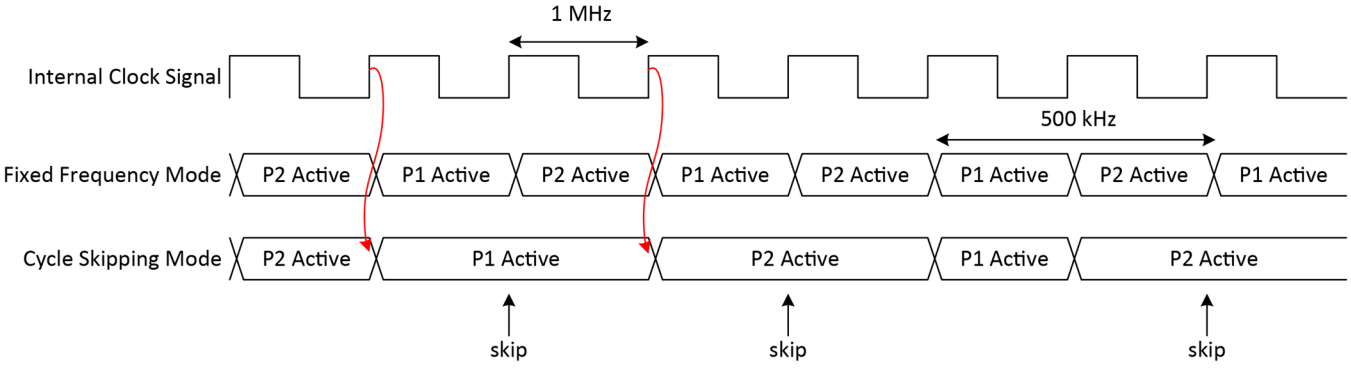


Figure 26. Switching Waveforms in Fixed Frequency and Cycle Skipping Modes

Asynchronous clock mode is different from fixed-frequency and cycle-skipping modes. Asynchronous clock mode is controlled by monitoring the voltage at the VX pin. When the VX voltage droop is sufficient, the charge pump is clocked to restore the VX voltage and deliver power to the load. For light loads, the voltage at VX reduces more slowly, leading to a lower charge pump clock frequency. As the load increases, the rate that VX reduces increases, and the charge pump clocks more frequently to compensate while keeping the amplitude of the VX ripple constant.

Figure 26 shows the expected voltage waveforms in asynchronous clock mode, including the VX ramp rate relationship to load and the resulting potential charge pump clock rate.

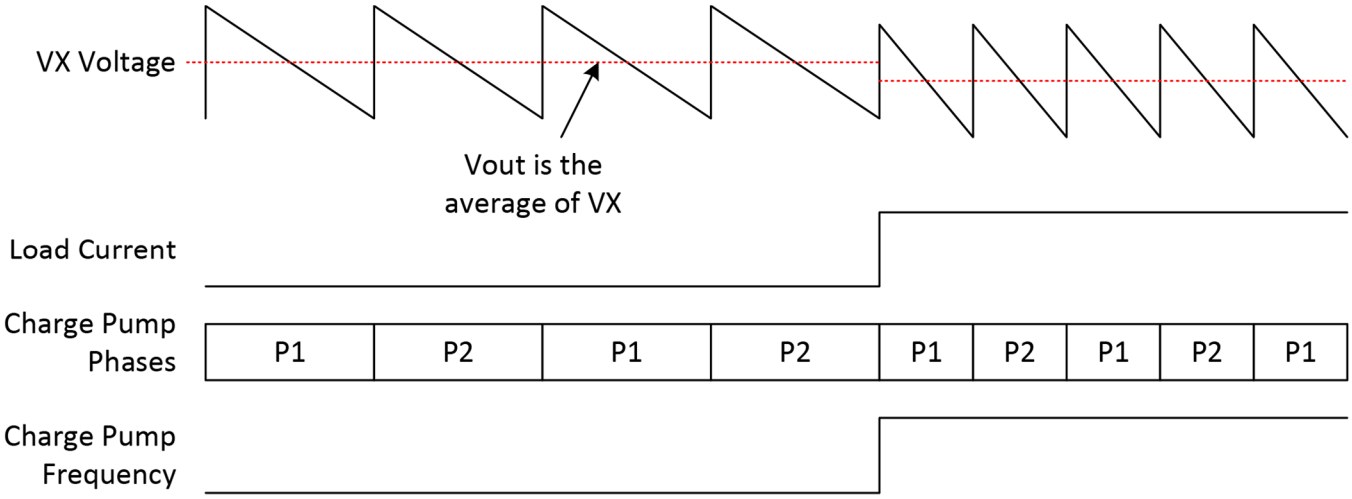


Figure 27. Potential Voltage Waveforms in Asynchronous Clock Mode

As with cycle skipping mode, the asynchronous clock frequency at low- or no-load is limited to being above the audio band. At very high loads the asynchronous charge pump clock frequency is limited to a maximum of 500 kHz. The charge pump clock frequency varies for different load currents to keep the maximum VX ripple constant. Asynchronous clock mode provides support to prioritize the VOUT ripple over efficiency in certain applications.

Power Good (PGOOD) Operation

The PE25200 has an open drain “power good” pin. For proper operation, PGOOD must have an external pull-up to VIN, VREG, or an external voltage >1.5V. The PE25200 holds the PGOOD pin low whenever the charge pump is in soft-start, or when a fault condition is detected and being handled. During soft-start, the power that the PE25200 can supply to a load is limited—as set by the SS pin configuration—and the load current must be kept well below the selected soft-start current level to ensure that VOUT can ramp to the target voltage in less than 10 ms (the soft-start timeout value). When the PE25200 allows PGOOD to be pulled high, the charge pump is ready to support the full load current.

The PGOOD pin of a disabled device is NOT pulled low. In effect, if EN=0, ignore the PGOOD pin.

External and Internal Clock Modes and the SYNCSEL Pin

In most applications, the PE25200 charge pump operates using an internal precision oscillator. The SYNCSEL and CLKSYNC pins can also be configured to support the use of an external clock source for the charge pump. This configurability is controlled by the SYNCSEL pin connection, as listed in Table 11.

Table 11. SYNCSEL Operation

SYNCSEL pin	CLKSYNC pin
GND	Clock output
Float(*)	CLKSYNC disabled
VIN	Sync input

Note:
* When floating SYNCSEL, ensure that the pin cannot sink or source > 100 mA. If driven from a tri-state buffer and the 100-mA condition cannot be guaranteed under all conditions, add a 100-ohm resistor in series with the pin.

SYNCSEL and CLKSYNC support a range of possible use cases, for example, using an external clock source to vary the charge pump switching frequency for EMI reasons in fixed-frequency or cycle-skipping clock modes.

If an external clock is not being used in the application, leave the SYNCSEL pin to float and tie the CLKSYNC pin to GND.

Using an External Clock

If the SYNCSEL pin is connected to VIN, the PE25200 expects a free running 625 kHz to 1 MHz clock at the CLKSYNC pin with voltage levels nominally 0V and VREG. The charge pump operates at half the frequency of the external clock (312 kHz to 505 kHz). This ratio from the external clock frequency to the charge pump switching frequency is fixed. The external clock only controls the charge pump clock frequency when the PE25200 is configured to operate in fixed-frequency or cycle-skipping clock modes. Using an external clock when operating in asynchronous clock mode (FF = VIN) is not supported.

To improve the PE25200 fault tolerance and support external clock signals which might not be free-running, the PE25200 includes an external clock watchdog function. If configured to use an external clock (SYNCSEL = VIN), and the external clock stops or is not present, the watchdog detects the missing clock and causes the PE25200 to revert to the internal clock source. After the expected external clock source resumes, the PE25200 reverts to the external clock.

Protection Modes

The PE25200 is a high-power device. To protect the system and the PE25200 internal circuitry, multiple fault detection circuits are built in, as listed in Table 12.

Table 12. Protection Modes

Detector	Persistent fault(*)	Response time	Effect of fault on PE25200
Over-temperature thermal shutdown	Yes	µs	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown and stays off until the die temperature has reduced below the thermal shutdown level minus hysteresis.
VIN under-voltage	Yes	µs	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown and stays off until the VIN voltage exceeds the under-voltage lockout threshold.
VX over-voltage	Yes	Instant	PGOOD goes low. The PE25200 charge pump disconnects from VIN (so no further power should pass from VIN to the load) but continues to clock to discharge the VX node. When the VX voltage falls below the V_{XOVP} threshold, the power stage fully turns off through a soft shutdown.
ILOAD short circuit current	No	Instant	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown. After a cooldown/pre-charge period of 40 to 160 ms, the charge pump attempts to soft start again.
VOUT short circuit	No	Instant	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown. After a cooldown/pre-charge period of 40 to 160 ms, the charge pump attempts to soft start again.
ILOAD over-current	No	µs	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown. After a cooldown/pre-charge period of 40 to 160 ms, the charge pump attempts to soft start again.
VOUT under-voltage	No	µs	PGOOD goes low. The PE25200 power stage is turned off through a soft shutdown. After a cooldown/pre-charge period of 40 to 160 ms, the charge pump attempts to soft start again.
VREG under-voltage	Yes	µs	PGOOD goes low. The PE25200 power stage is turned off immediately. This is an uncontrolled shutdown. The charge pump remains off until VREG recovers back above the VREG UVLO level.

Soft-start timeout	No	µs	If VOUT does not reach the target voltage within the soft-start timeout period, the charge pump enters the cooldown/pre-charge state for at least 40 to 160 ms before it attempts to soft-start again.
PGOOD held (or set) low when expected high	Yes	µs	From full power, the charge pump initially returns to a limited load current soft-start mode. If the PGOOD signal is held low for less than the soft-start timeout period, the charge pump returns to full power operation. If PGOOD = 0 exceeds the soft-start timeout, the charge pump loops through soft-start, cooldown/pre-charge, soft-start, cooldown/pre-charge and so on until PGOOD is allowed to go high.

Note:
* A persistent fault keeps the charge pump in a fault state for as long as the fault is present. A non-persistent fault does not prevent the charge pump from re-enabling after some fault recovery time has been applied.

Pre-charge Phase

The recovery from all fault conditions passes through a pre-charge phase before the PE25200 attempts to soft start. The goal of the pre-charge phase is to set the flying capacitors to their nominal voltage (VOUT or 2VOUT, depending on the division ratio) prior to applying power to the load. The pre-charge circuit is used as part of the fault recovery mechanism because it is a push-pull circuit that can charge or discharge the flying capacitors as needed to reach the target voltage. In normal (fault free) operation, the pre-charge phase typically is fast because VOUT is close to 0V (cold start-up), or the flying capacitors are close to nominal anyway (if EN is being cycled ON/OFF quickly enough for VOUT and the flying capacitors to remain close to normal operating voltages). The minimum and maximum times for the pre-charge phase are 40 and 160 ms, respectively.

VIN Under-voltage and Thermal Shutdown Faults

The VIN under-voltage and thermal shutdown faults are grouped together because the effect they have on the charge pump is similar. If either of these faults are present when the charge pump is first enabled, the charge pump starts to power up but holds before any power (even soft-start current) is applied to the load. The charge pump holds in this state until both faults are clear (regardless of how long this takes). VIN under-voltage and thermal shutdown faults are considered “persistent” as they hold the charge pump disabled until the fault clears.

If a VIN under-voltage occurs, it is unlikely that the charge pump can support the full load current when VIN—and therefore VOUT—is too low. This is not ideal for the PE25200 or for the load, so the charge pump waits for VIN to improve/recover.

An over-temperature fault only occurs if the PE25200 is dissipating too much internal power. An over-temperature fault normally results from some other fault condition or from operating the PE25200 with low efficiency and high-power levels. If an over-temperature occurs, the PE25200 could start to operate outside of its guaranteed performance specs, which is not ideal for the system. To recover from over-temperature, the power dissipation in the chip must be reduced to allow the heatsink to reduce the die temperature.

When a VIN under-voltage or an over-temperature fault are detected during normal operation, the PE25200 enters a controlled shutdown sequence with an unlimited cooldown period (the minimum cooldown time is 80 µs). When the faults clear, the PE25200 enters a pre-charge phase followed by a normal soft-start sequence.

VX Over-voltage Protection

The VX over-voltage fault detector protects both the PE25200 and the output load from over-voltage conditions. To ensure that over-voltage at VX does not propagate to VOUT, the VX over-voltage detection circuit operates quickly. VX over-voltage faults are initially treated differently from most of the other fault flags.

The first response is to disconnect the PE25200 power stage from VIN. The path for power from VIN to VOUT is opened to remove one possible source of the over-voltage. The charge pump continues to clock, and a fixed-frequency mode is temporarily forced regardless of the FF pin connection. Clocking the charge pump without a connection to VIN creates a path from VX to GND, which acts to discharge VX. VX typically discharges rapidly and, as a result, the VX fault is cleared quickly.

To complete the recovery from the VX over-voltage, the PE25200 enters a controlled shutdown sequence that includes pre-charge. When the pre-charge is complete and after a minimum cooldown time of 40 ms, the PE25200 enters a normal soft-start sequence and attempts to restart.

The initial response to the VX over-voltage of disconnecting VIN and continuing to clock continues with no time limit for as long as the VX over-voltage fault is detected. In most cases, this is expected to clear the VX over-voltage quickly (within a few charge pump clocks). In the unlikely event that VX over-voltage is detected because of over-voltage at VOUT (for example, due to a second power source in the system), the PE25200 attempts to discharge VX—and thus VOUT—through the switching action and the flying capacitors for an unlimited period of time. While in this VX over-voltage recovery state, some of the normal fault detectors—such as load current detectors—do not operate. As a result, do not use VX over-voltage to recover from a system-caused VOUT over-voltage condition.

ILOAD Short Circuit and Overcurrent Protection

The two ILOAD fault detection flags operate by sensing the current being drawn from VIN. The short circuit flag (ILOADSC) is a fast-acting fault with a high-trip threshold designed to capture instantaneous fault levels, such as a dead short occurring at VOUT. The over-current protection flag (ILOADOC) can be considered as a longer-term average current type of measurement. As a result, the trip point can be set closer to the nominal 10A maximum output load. The over-current protection trips if the PE25200 is operated outside the recommended operating conditions.

The PE25200 reaction to the ILOADSC and ILOADOC faults is the same. The PE25200 enters a controlled shutdown sequence that includes pre-charge. When the pre-charge is complete and after a minimum cooldown time of 40 ms, the PE25200 enters a normal soft-start sequence and attempts to restart. Some persistent fault conditions could prevent the charge pump from restarting successfully, such as a hard fault to GND at VOUT, which would trigger ILOADSC.

Figure 28 shows the flow for a persistent fault case. The fault initially triggers the recovery/pre-charge step. Then, if the charge pump remains enabled, the PE25200 attempts to soft start again. If the fault still holds VOUT low, the PE25200 enters a *hiccup* mode in which the soft-start timeout trips, causing the cooldown/pre-charge phase to restart. The loop in Figure 28 repeats for as long as the fault is present and the PE25200 remains enabled.

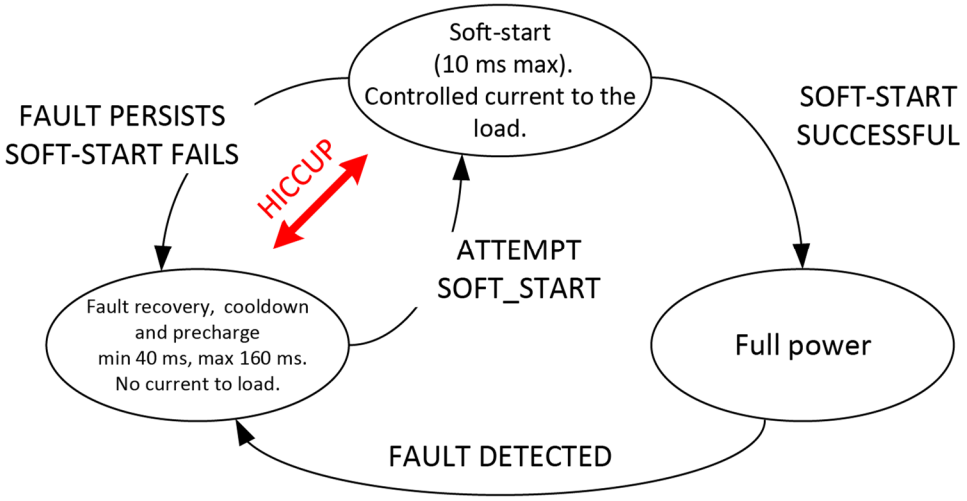


Figure 28. Pre-charge Hiccup Mode for Some Persistent Fault Types

VOUT Short Circuit and VOUT Under-voltage Protection

The VOUT short circuit and VOUT under-voltage fault detectors work in the same way. They compare the measured value at VOUT with the expected value derived from VIN so that VOUT is compared with VIN/2 or VIN/3, depending on the MODE pin setting. The VOUT short circuit fault is designed to operate very quickly, but only when VOUT is substantially below 60% of the target voltage. The VOUT under-voltage fault is designed to be slower and represent more of an average value. The VOUT under-voltage flag trips when VOUT falls below 80% of the target (V_{UVP}).

The VOUT short circuit detector is designed to operate in parallel with the ILOADSC fault to provide more independence from the external component values. For example, the result of a dead short to GND at VOUT while PE25200 is operating at 10A depends partly on the inductor between VX and VOUT. It is possible that VOUT reaches the VOUTSC threshold sooner than ILOADSC reaches the short circuit current limit, so supporting both fault detectors allows a better opportunity to stop the power going to the fault condition as soon as possible.

The VOUT under-voltage detector trips when VOUT falls below 80% of the target voltage. It is important that the external components are chosen so that the expected transient loads do not trip the V_{UVP} threshold. In effect, the application must ensure that the load dependency causes less than 20% deviation from the nominal VOUT.

When a VOUT short circuit or VOUT under-voltage occurs, the effect on the charge pump is similar, and the same for ILOADSC. The PE25200 enters a controlled shutdown sequence that includes pre-charge. When the pre-charge is complete—and after a minimum cooldown time of 40 ms—the PE25200 enters a normal soft-start sequence and attempts to restart.

VREG Under-voltage Protection

The VREG under-voltage fault condition is potentially serious. Many of the charge pump controls and fault detection flags use the VREG supply internally. For this reason, VREG must not be externally loaded to ensure that VREG under-voltage is not triggered by external circuit load.

When VREG is pulled below the under-voltage trip voltage—approximately 3V—the charge pump shuts down immediately, PGOOD is pulled low, and no further power is supplied to the load. The internal VREG regulator has an internal short circuit current limit, so that the VREG fault itself does not damage the PE25200, but the effects of stopping the supply to the load in an unplanned way could be serious. The PE25200 is designed to survive the immediate shutdown, but not all the effects of the shutdown are controlled by the PE25200 itself. For example, the inductor can cause a voltage spike when the load current is abruptly cut off. The voltage spike depends on the external inductor, the load capacitance, and the load current at the instant of shutdown. Consider the PE25200 absolute maximum ratings for the end application so that a VREG short can be handled without exceeding the device ratings.

The VREG under-voltage fault is *persistent* in that the PE25200 remains disabled for as long as VREG is held below the under-voltage threshold. When the fault clears, the PE25200 samples the FF, SS, FTUNE, SYNCSEL and MODE pins again to obtain the chip configuration, then enters pre-charge and a soft-start before allowing PGOOD to go high to signal that full power operation is possible.

Soft-start Timeout

When the PE25200 first tries to supply power to the load, it uses a soft-start circuit so that the power level is limited. Using a soft start has no significant side effects if the start-up is *normal*.

If the PE25200 starts up into a fault, the soft-start helps to manage the power supplied to the fault and limits the power dissipation in the PE25200. In normal, fault-free, operation, the soft-start timeout is invisible if the soft-start current—which you configure using the SS pin—can ramp VOUT to the target voltage within 10 ms. If a fault occurs, the soft-start timeout occurs when VOUT does not ramp to the target voltage within the expected time. In this case, the soft-start timeout stops power to the load, and the PE25200 enters a controlled shutdown sequence that includes pre-charge. When the pre-charge is complete, and after a minimum cooldown time of 40 ms, the PE25200 attempts the soft-start sequence again, as shown in Figure 28.

PGOOD Low Detection

In a standalone PE25200 implementation, only one driver of the PGOOD signal is likely to exist. When the PE25200 is ready for full power, PGOOD goes high and stays high for as long as the single PE25200 remains enabled and fault-free.

Capacitor Imbalance

The PE25200 implements proprietary algorithms to handle capacitor imbalance in real-world solutions. Because the PE25200 is a charge pump-based DC-DC device, it uses four flying capacitors. In a real-world solution, the flying capacitor components are not ideal and likely not identical. The PE25200 can work with extremes of capacitance values, such as phase 1 capacitors at +20% of nominal value and phase 2 capacitors at -20% of nominal value. The proprietary algorithms allow full power to be supplied to the load and help to prevent capacitor imbalance from inducing large ripple at the VX pin (and higher ripple at VOUT).

Component Selection

This section describes the PE25200 required components.

Flying Capacitors

The PE25200 requires two sets of flying capacitors: the “CB” and “CA” capacitors. The CB capacitors connect between the C*B (C1B, C2B) and P*B (P1B, P2B) pins while the CA capacitors connect between the C*A (C1A, C2A) and P*A (P1A, P2A) pins. Both the CA and CB capacitors are important components for efficiency and must be placed as close to the PE25200 as possible.

The steady state voltage across the CB capacitors is 2* V_{OUT} for divide-by-3 mode and 1* V_{OUT} for divide-by-2. The steady state voltage across the CA capacitors is 1* V_{OUT} for both divide-by-3 and divide-by-2 modes. To take ripples and spikes into account, choose the capacitors so that the component voltage rating is higher than the steady state voltage. For example, for 15V V_{IN} and divide-by-3 operation, choose CB capacitors with a voltage rating of 16V, and CA capacitors with a 10V rating.

The capacitance value at the applied voltage across the capacitors has a direct impact on the maximum efficiency that can be achieved. The nominal capacitance value typically drops as the voltage across the capacitor increases, depending on the voltage coefficient of the selected capacitors. Low-voltage coefficient components are preferable to ensure enough capacitance at the applied steady state voltage.

When selecting the capacitor values for maximum efficiency, take the switching frequency into consideration so that the self-resonant frequency (SRF) of the capacitors is higher than the maximum charge pump switching frequency.

At maximum power, the PE25200 could reach a junction temperature of up to 125 °C at 85 °C ambient. This can heat the surroundings of the die and potentially the flying capacitors. The choice of the temperature rating of the capacitors is dependent on the temperature gradient across the board and the placement of the capacitors with respect to the die.

Vx Capacitor

The Vx capacitor connects between the VX pin and the board-level power ground. The steady state average voltage across the Vx capacitor is equal to V_{OUT}. Typically, adiabatic charge pump operation results in approximately 400 mV of ripple at VX under high load, which you must consider when choosing the voltage rating for the Vx capacitor. Set the Vx capacitor rating to exceed the Vx over voltage protection (V_{XOVP}) value so that the on-chip device protection circuits can activate before damage is caused to the Vx capacitor. This increases system robustness to fault situations. The Vx capacitor reduces the voltage ripple at VX, but it can also cause higher charge redistribution loss and reduced efficiency. Optimize the Vx capacitor value around those criteria. The current recommended value is 3 µF at the applied voltage.

Lx Inductor

The Lx inductor connects Vx to V_{OUT}, and the load. V_{OUT} is a filtered version of Vx. Lx reduces the charge distribution loss when switching between the two PE25200 complementary switching phases. The higher the inductance value, the lower the charge distribution loss, but also the higher the voltage ripple on Vx. Choose an optimum value of Lx to minimize the charge distribution loss while supporting acceptable voltage ripple at Vx and V_{OUT}. The recommended inductance value is 10 nH.

The Lx inductor must support the full load output current. For robust system design, the Lx inductor must support the ILOAD output current limit (I_{LIM}) of 12A. This allows the on-chip protection circuits to activate before causing inductor damage if a fault occurs. The path from Vx to V_{OUT} through the Lx inductor must be achieved with minimum parasitic resistance because losses in the inductor or in the system-level routing have a direct impact on the system efficiency.

Output Capacitor

The output capacitor reduces the ripple applied to the load at VOUT. The higher the capacitor value, the lower the ripple at VOUT. Increasing the output capacitor value increases the soft-start duration and could cause the PE25200 to timeout during soft start. The PE25200 supports a range of soft-start currents—by configuring the SS pin—but it is essential that the chosen soft-start current can charge the chosen output capacitor value within the soft-start timeout duration. The soft-start current must charge the chosen output capacitor value within the soft-start timeout duration. The soft start timeout value is based on being able to reliably charge 100 µF to 5V using a 0.5A soft-start current.

Input Capacitor

The input capacitor connects V_{IN} and GND. It reduces the ripple on V_{IN} when the PE25200 switches. To reduce any parasitic inductance effects, place the input capacitor as close to the PE25200 as possible. The voltage rating of the capacitor must be as high as the absolute maximum voltage rating for the system and consider the effect of the capacitor voltage coefficient to determine the effective capacitance value at the applied V_{IN}.

Application Information

A single-device evaluation kit (EVK) applications board was used to obtain the results in this datasheet.

- Figure 29 shows the applications board schematic.
- Table 13 lists the key recommended passive components critical to achieving similar performance.
- Figure 30 shows the assembled device board.

Application Schematic

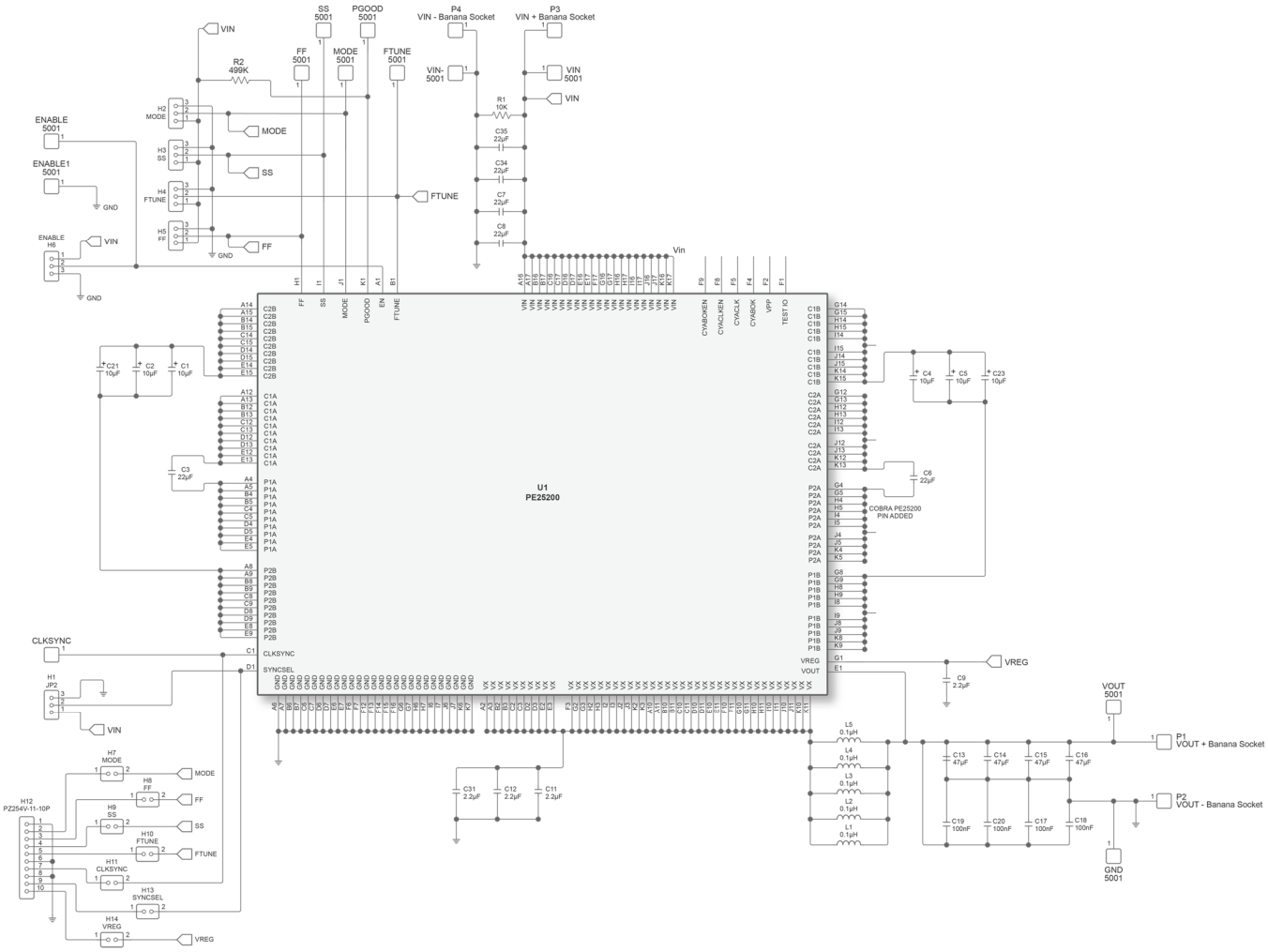


Figure 29. Device Board (EVK) Application Schematic

Application Circuit Part List

Table 13. Recommended Parts

Ref. number	Value	Quantity	Part code
CA	22 µF	×1	GRM21BD71A226ME44L
CB	10 µF	×3 in parallel	GRM21BC71C106KE11L
CVX	2.2 µF	×2–3 in parallel	GRM155C71A225KE11D
LX	100 nH	×5 in parallel = 20 nH with sufficient current	LQM2MPZR10MJH
CIN	22 µF	×4 in parallel	GRM31CC81E226ME11L

Evaluation Board

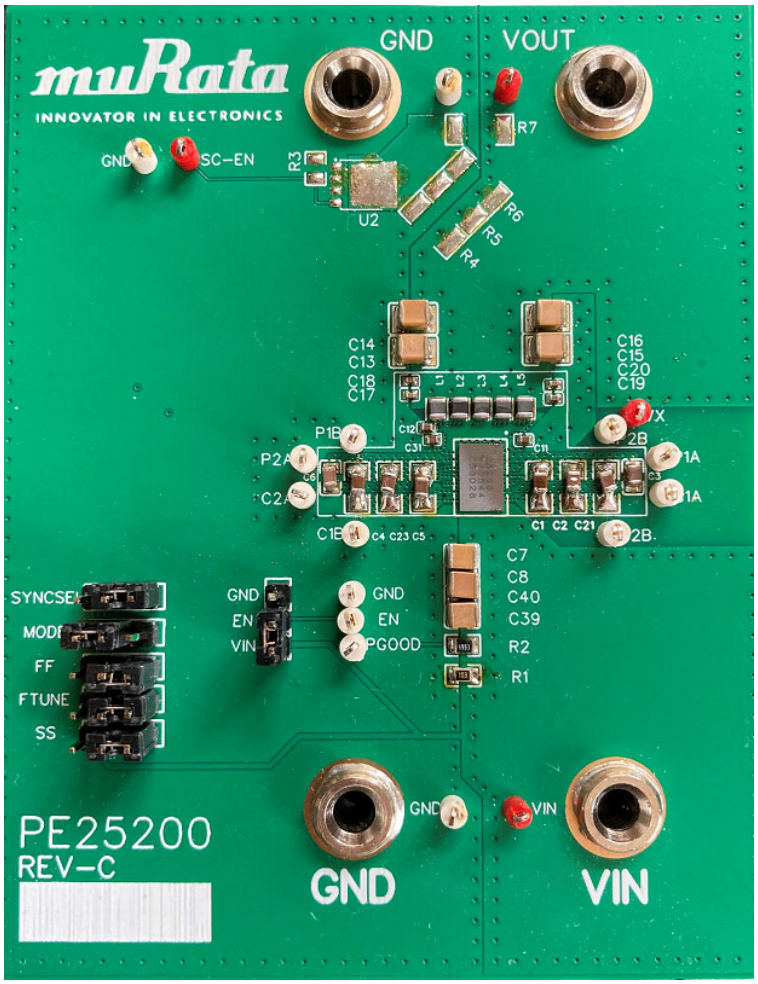


Figure 30. Device Board (EVK)

Figure 31 shows the relationship between the thermal conditions over time and the resulting behavior of the PGOOD signal.

The junction temperature of the device increases until it reaches the temperature threshold of typically 150°C, at which point the PGOOD signal collapses and does not recover until the temperature has dropped below the 125 °C threshold.

The PGOOD signal recovers to its normally 'high" state and remains there if the device's maximum junction temperature is not reached. The difference in the temperature limits determines the thermal hysteresis, which directly influences the time taken for the PGOOD signal to recover again after it drops out.

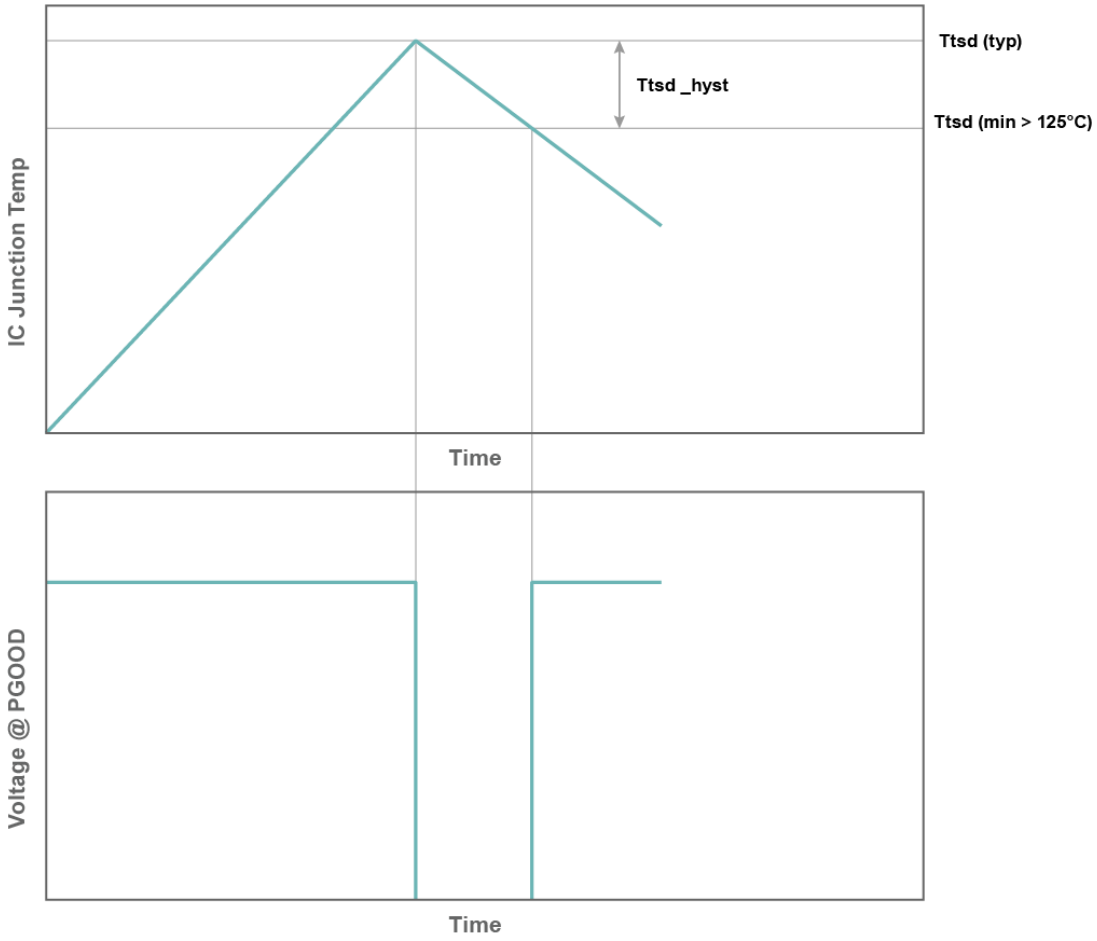


Figure 31. General Relationship Between the Junction Temperature, Thermal Shutdown, Hysteresis, and PGOOD Signal

Packaging Information

This section provides the following packaging data:

- Moisture sensitivity level (MSL)
- Package drawing
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The PE25200 moisture sensitivity level rating for the 6.850 mm × 4.450 mm × 0.492 mm WLCSP is MSL1.

Package Drawing

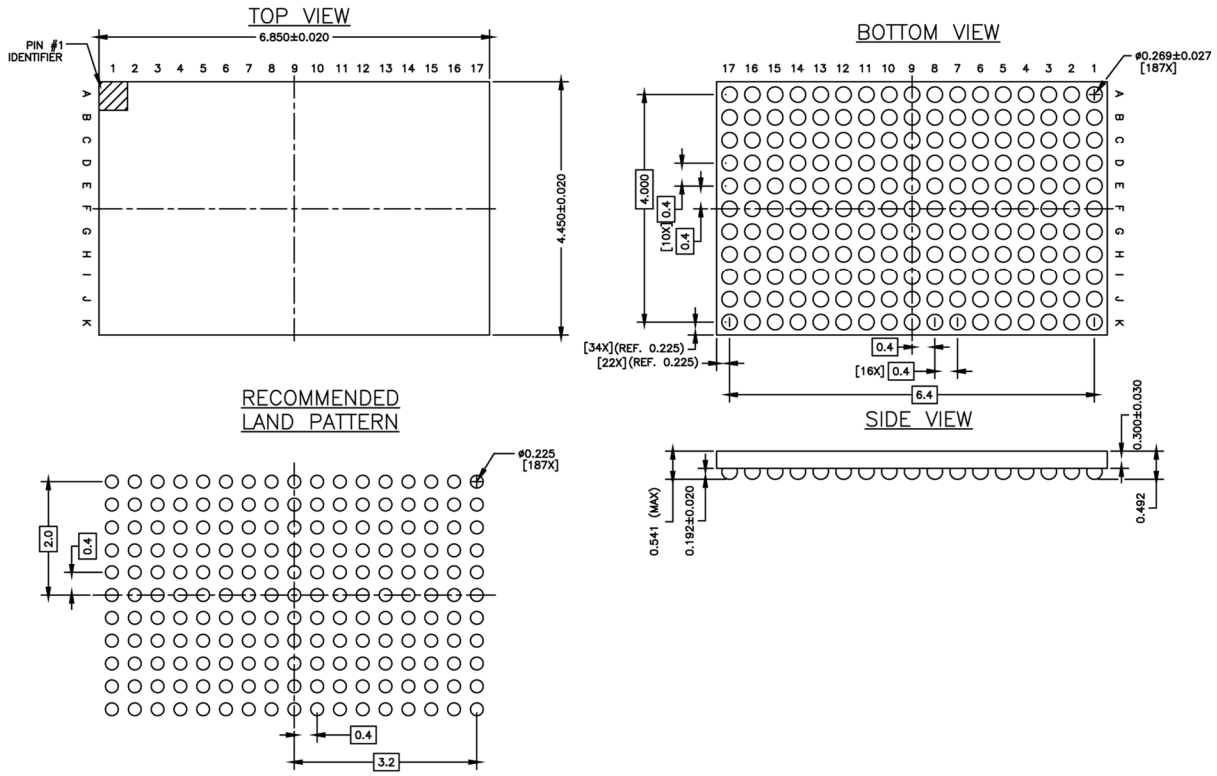
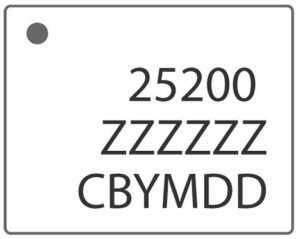


Figure 32. PE25200 Package Outline Drawing

Top-marking Specification



● = Pin 1 indicator
PPPPP = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
CB = Supplier code
Y = Last digit of assembly year (2019 = 9)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

Figure 33. PE25213 Package Marking Specification

Tape and Reel Specification

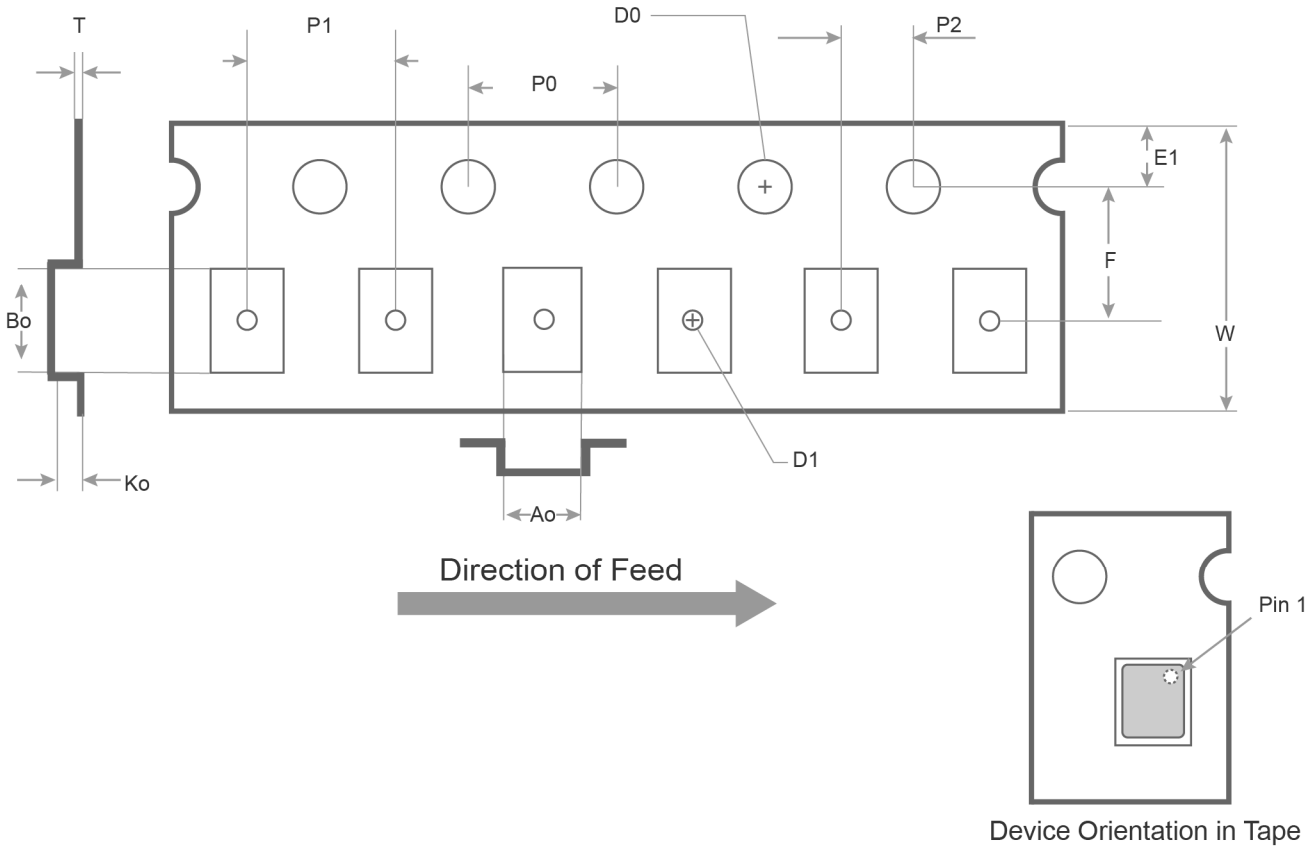


Figure 34. Tape and Reel Specifications for the 6.850 mm × 4.450 mm × 0.492 mm WLCSP

Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 14. Tape and Reel Dimensions

Carrier tape dimensions					
Pocket	**Nominal**	**Tolerance**	**Pocket**	**Nominal**	**Tolerance**
Ao	4.85	±0.05	D1	1.50	±0.25
Bo	7.13	±0.05	D0	1.50	+0.10/-0
Ko	0.63	±0.05	E1	1.75	±0.10
P1	8.00	±0.10	P0	4.00	±0.10
W	16.00	+0.30/-0.10	P2	2.00	±0.10
F	7.50	±0.10	T	0.25	±0.02

Ordering Information

Table 15. Order Codes and Shipping Methods

Order code	Description	Packaging	Shipping method
PE25200A-X	45W Charge Pump Divide-by-2 or -3	WLCSP on tape and reel	500 Units/T&R
EK25200-HDI-FG	45W Charge Pump EVK	PCB Board	1 Unit

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

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