PE25203

Document Category: Product Specification

Divide-by-2 and -3, 4A Charge Pump, Capacitor Divider

General Description

The PE25203 is an ultra-high efficiency charge pump that is configurable to divide down an input voltage by two or three and delivers up to 4A with peak efficiency up to 99%.

The PE25203 supports an input voltage range of 5.7V to 10V in divide-by-2 mode and 8.4V to 15V in divide-by-3 mode. The PE25203 is primarily used to convert a two- or three-cell battery input to a 1S output for the downstream regulator to improve overall system efficiency and extend the run time.

The PE25203 offers a unique auto-switch mode to change the divide-down ratio during operation to avoid a downstream under-voltage lockout (UVLO) event at heavy system loading during a low-battery condition.

The PE25203 comes in a 4.545 mm × 2.715 mm 47-pin WLCSP package. The pinout is designed to be fully compatible with Type III PCB design.

Features

- Proprietary architecture enables industry leading efficiency with an ultra-low 1-mm profile solution
- Wide input voltage range, from 5.7V to 15V, supports two- or three-cell mobile computers and 12V-bus point-of-load applications
- Peak efficiency of 99%
- Pin-selectable cycle skipping mode for improved light-load efficiency
- Dynamically configurable divide-by-2 or -3 modes under load
- Low EMI fixed-frequency operation under heavy load conditions
- Fully protected input under-voltage, output over-current and thermal shutdown

Applications

- Two-cell and three-cell lithium platforms
- Ultrabook and notebook computers
- Full-size tablet computers
- Ultra-thin form factor designs
- 12V_{IN} point-of-load designs in networking and telecommunications

Efficiency

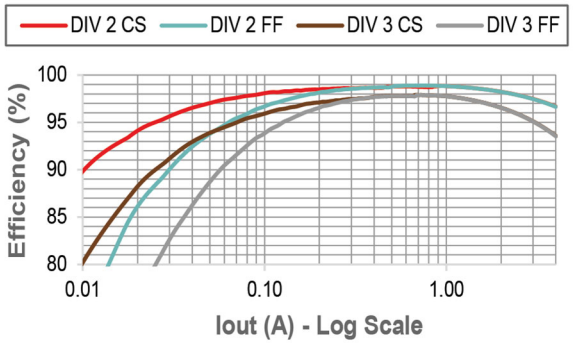

Figure 1. Typical efficiency with V_{IN}=7.7V in divide-by-2 and V_{IN}=11.55V in divide-by-3, fixed frequency (FF) and cycle skip (CS) modes

Application

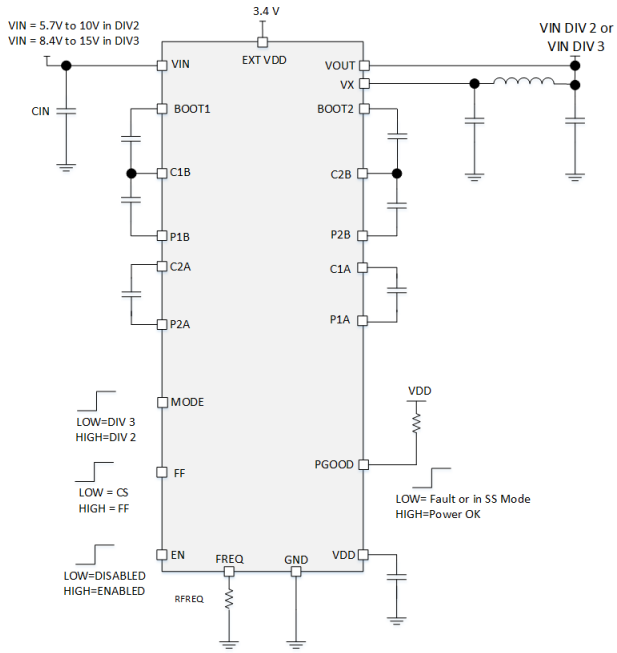

Figure 2. Application Schematic

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Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from ESD damage, do not exceed the ratings listed in Table 1.

Table 1. PE25203 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Input voltage, divide-by-3 mode	–	30	V
Input voltage, divide-by-2 mode	–	20	V
Output voltage V_{OUT}	–	10	V
V_{DD} external	–	10	V
Storage temperature	-65.0	150.0	°C
Junction temperature	-40.0	150.0	°C
Operating bump or lead temperature	–	260.0	°C
FREQ, FF	–	VDD+0.3	V
EN, MODE, PGOOD	–	VIN+0.3	V
Human body model, all pins[1]	–	1500	V
Charged device model, all pins[2]	–	1000	V

Notes:
1. Human Body Model, all pins (Joint JEDEC/ESDA Human Body Model (JS-001-2017))
2. Charged Device Model, all pins (Joint JEDEC/ESDA Charged Device Model (JS-002-2018))

Recommended Operating Conditions

Table 2 lists the PE25203 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE25203 Recommended Operating Conditions

Parameter	Min	Max	Unit
Input voltage (V_{IN}) range, relative to GND, in divide-by-3 mode	8.4	15	V
Input voltage (V_{IN}) range, relative to GND, in divide-by-2 mode	5.7	10	V
Junction temperature range (T_J)	-40.0	125.0	°C

Package Thermal Characteristics

Table 3 lists the PE25203 thermal characteristics.

*Table 3. PE25203 Package Thermal Characteristics**

Parameter	Conditions	Min	Typ	Max	Units
Maximum junction temperature	Measured at maximum ambient temperature (T_A) and maximum power dissipation	–	–	150.0	°C
Junction-to-Case Top Thermal Resistance (ΘJA)	JEDEC JESD51-12-01 and JESD15-3	10.4	–	–	°C/W
Junction-to-Board Thermal Resistance (ΘJB)	JEDEC JESD51-12-01 and JESD15-3	6.75	–	–	°C/W
Junction-to-Air Thermal Characterization (ΨJA)	–	33.9	–	–	°C/W

Note: * The package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-12. See also pSemi Application Note 57: *Thermal Characterization*.

Electrical Specifications

Table 4 lists the PE25203 key electrical specifications at the following conditions, unless otherwise specified:

- V_{IN} = 5.7V to 10V, MODE = V_{IN}, T_J = -40 °C to +125 °C, Frequency = GND
- V_{IN} = 8.4V to 15V, MODE = GND, T_J = -40 °C to +125 °C, Frequency = GND

Table 4. PE25203 Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage range						
Input voltage range	V_{IN}	MODE = Logic High (V_{OUT} = V_{IN}/2)	5.7	–	10	V
		MODE = Logic Low (V_{OUT} = V_{IN}/3)	8.4	–	15	
V_{IN} under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{IN} rising [MODE = logic high (V_{OUT} = V_{IN}/2)]	–	–	5.69	V
		V_{IN} rising [MODE = logic low (V_{OUT} = V_{IN}/3)]	–	–	8.39	
V_{IN} under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	–	–	150	–	mV
External V_{DD} input range	–	–	3.4	–	5	V
Transition from external V_{DD} to internal V_{DD} threshold	–	–	–	3.16	3.39	V
Output current						
Maximum output current	I_{LOAD}	–	4	–	–	A
Output current limit	I_{LIMIT}	–	4.1	–	–	A
Supply current						
External V_{DD} supply current	–	External V_{DD} = 3.4V full load	–	175	–	µA
Shutdown supply current	–	EN = GND at 25 °C	–	–	1	µA
Operating supply current	–	External V_{DD} = 3.465V, I_{LOAD} = 0A, FF = HIGH (at maximum V_{IN} = 15V DIV3)	–	–	3.6	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Full load switching frequency typical setting[1]	F_{SW}	Frequency range FREQ = 505 kΩ to 82.5 kΩ (1)	200	–	1000	MHz
		FREQ = 505 kΩ	–	200	–	kHz
		FREQ = GND	180	200	220	
		FREQ = 82.5 kΩ	–	1000	–	
Nominal output voltage	V_{O_NOM}	MODE = logic high	—	$V_{IN}/2$	–	V
		MODE = logic low		$V_{IN}/3$	–	
V_{OUT} under-voltage protection threshold	V_{UVP}	MODE = logic high (V_{OUT} = $V_{IN}/2$)	0.7* $V_{IN}/2$	0.8* $V_{IN}/2$	0.9* $V_{IN}/2$	V
		MODE = logic low (V_{OUT} = $V_{IN}/3$)	0.7* $V_{IN}/3$	0.8* $V_{IN}/3$	0.9* $V_{IN}/3$	
V_{OUT}_uvp glitch suppression	T_{UVP}	To trigger a fault, V_{OUT} must be less than V_{UVP} for longer than T_{UVP}.	–	1.6	–	µs
Vx over-voltage protection	V_{XOVP}	–	10.5	11.5	13	V
Thermal shutdown threshold	T_{TSD}	–	140	160	–	°C
Thermal shutdown hysteresis	T_{TSD_HYST}	–	–	25	–	°C
Maximum soft start timeout duration	–	–	–	10	–	ms
Soft start input current limit	I_{SS_IIM}	V_{OUT} shorted to GND	–	2.5	–	A
Power good threshold	$PGOOD_{TH}$	Measured after soft start completed without other faults	–	–	95	% of V_{OUT}
Power good pin						
Pull-down resistance	R_{PGOOD}	I_{SINK} = 15 mA	–	26	–	Ω
PGOOD rising threshold	–	–	–	1.3	–	V
PGOOD hysteresis	$PGOOD_{HYS}$	–	–	180	–	mV
Output leakage	–	V_{OUT} > $PGOOD_{TH}$	–	–	1	µA
Time for PGOOD detect	$PGOOD_{DETECT}$	Time from falling edge of PGOOD to V_{OUT} no longer able to support full load. No external capacitor on PGOOD.	–	10.0	–	µs
V_{DD} output voltage[2]	V_{DD}	See Note 2.	–	3.65	–	V
Logic levels EN, MODE, FF						
Input high voltage	V_{IH}	–	1.5	–	–	V
Input low voltage	V_{IL}	–	–	0.4	–	V
EN pint input current	I_{EN}	EN = 15V	–	11	–	µA
MODE pin input current	I_{MODE}	MODE = 5.5V	–	3	–	µA
FF pin input current	I_{FF}	FF = 3.6V	–	1	–	µA

Notes:

1. Because the device is a dual-phase charge pump, each phase of the charge pump runs at 50% of the frequency set by the FREQ pin.
2. External loading of V_{DD} is only verified using Figure 39. Do not load V_{DD} externally.

Pin Configuration

This section includes the PE25203 pin configuration information. Figure 3 shows the pin map of this device in a WLCSP package, and Table 5 lists the pin descriptions.

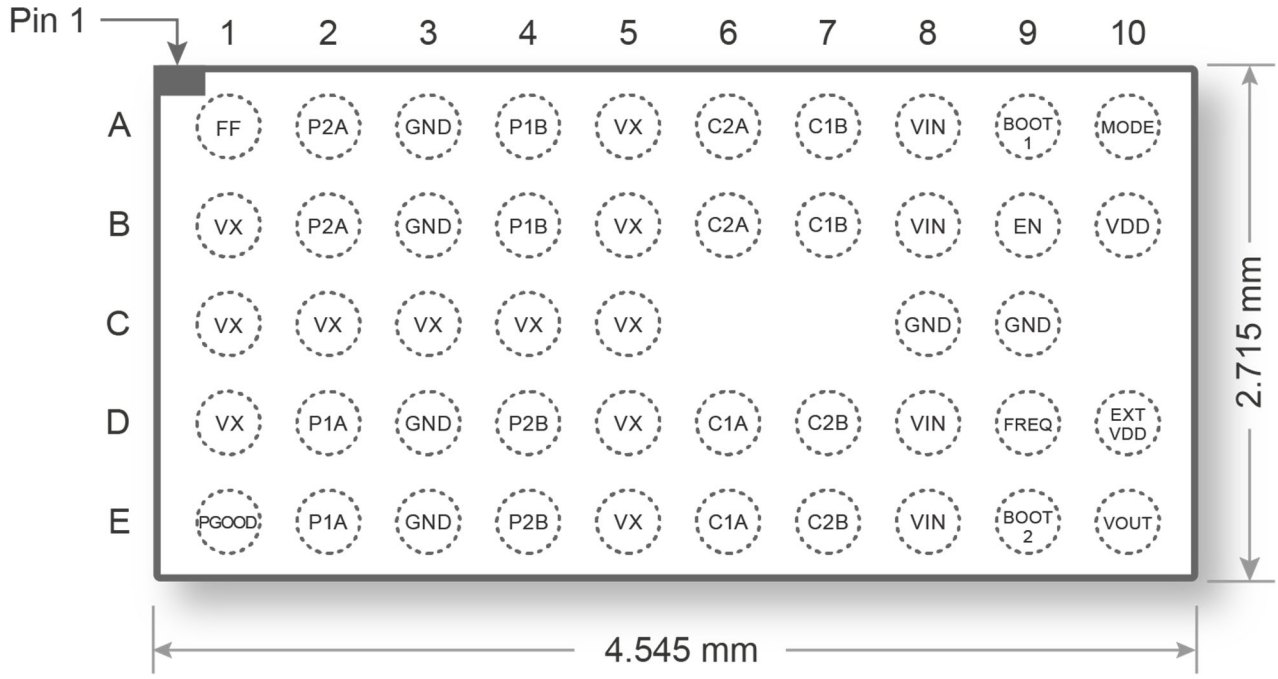


Figure 3. PE25203 Pin Configuration (Top View)

Pin Descriptions

Table 5. PE25203 Pin Descriptions

Pin No.	Pin Name	Description
A1	FF/CS	Selects the charge pump clock mode (logic high = fixed frequency, logic low = cycle skip). Read at IC power up. The value in this pin can be changed when EN = logic low.
A2, B2	P2A	Flying capacitor C2A phase node. Connect a fly capacitor between the C2A and P2A pins.
A3, B3, C8, C9, D3, E3	GND	Ground connection
A4, B4	P1B	Flying capacitor C1B phase node. Connect a fly capacitor between the C1B and P1B pins.
A5, B1, B5, C1, C2, C3, C4, C5, D1, D5, E5	VX	Charge pump output switching node. Connect to an external inductor.
A6, B6	C2A	Flying capacitor C2A terminal. Connect a fly capacitor between the C2A and P2A pins.
A7, B7	C1B	Flying capacitor C1B terminal. Connect a fly capacitor between the C1B and P1B pins.
A8, B8, D8, E8	VIN	Input voltage
A9	BOOT1	Bootstrap capacitor pin. Connect a 100 nF bootstrap capacitor between BOOT1 and C1B.
A10	MODE	Selects the charge-pump voltage-division ratio. Do not allow this pin to float. • MODE = logic high or V_{IN} or 3.6V for divide-by-2 mode. • MODE = logic low for divide-by-3 mode.
B9	EN	IC enable pin. A logic high enables the IC, and a logic low disables the IC.
B10	VDD	V_{DD} generated by the IC. Should be bypassed by a capacitor of 1 µF. Connect a capacitance to this pin even when powered by an external V_{DD}, typically 3.6V is generated on this pin.
D2, E2	P1A	Flying capacitor C1A phase node. Connect the fly capacitor between the C1A and P1A pins.
D4, E4	P2B	Flying capacitor C2B phase node. Connect the fly capacitor between the C2B and P2B pins.
D6, E6	C1A	Flying capacitor C1A terminal. Connect the fly capacitor between the C1A and P1A pins.
D7, E7	C2B	Flying capacitor C2B terminal. Connect the fly capacitor between the C2B and P2B pins.
D9	FREQ	Charge pump operating frequency select pin. The charge pump switching frequency is switching at 50% of the operating frequency set by this pin. Setting this pin to GND sets the operating frequency to 200 kHz. For other frequency selection, see Setting the Operating Frequency on page 17.
D10	EXT VDD	External V_{DD} input pin. In this mode, the IC is powered from the external V_{DD} instead of the internally generated V_{DD} on B10. The part does not need this to be supplied to operate, but if externally applied, it can increase the system efficiency. This pin can also be connected to the VOUT pin. If not used, connect it to ground.
E1	PGOOD	Open-drain power-good signal is enabled when V_{OUT} > 95% of the division ratio and no other faults are present. Must externally pull-up with a resistor value of 499 kΩ. A lower resistor value can reduce the system efficiency.
E9	BOOT2	Bootstrap capacitor pin. Connect a 100 nF bootstrap capacitor between the BOOT2 and C2B pins.
E10	VOUT	Output voltage sense. Connect to the other side of the VX inductor.

Functional Block Diagram

The PE25203 uses proprietary charge pump technology to deliver superior efficiency in a fully integrated WLCSP package.

The PE25203 provides a full set of protection features to ensure robust system operation that includes input under-voltage lockout (UVLO), thermal shutdown (TSD), over-current protection (OCP), output under-voltage protection (UVP), output over-voltage protection (VX OVP), and soft-start timeout (SST).

Figure 4 shows the PE25203 functional block diagram.

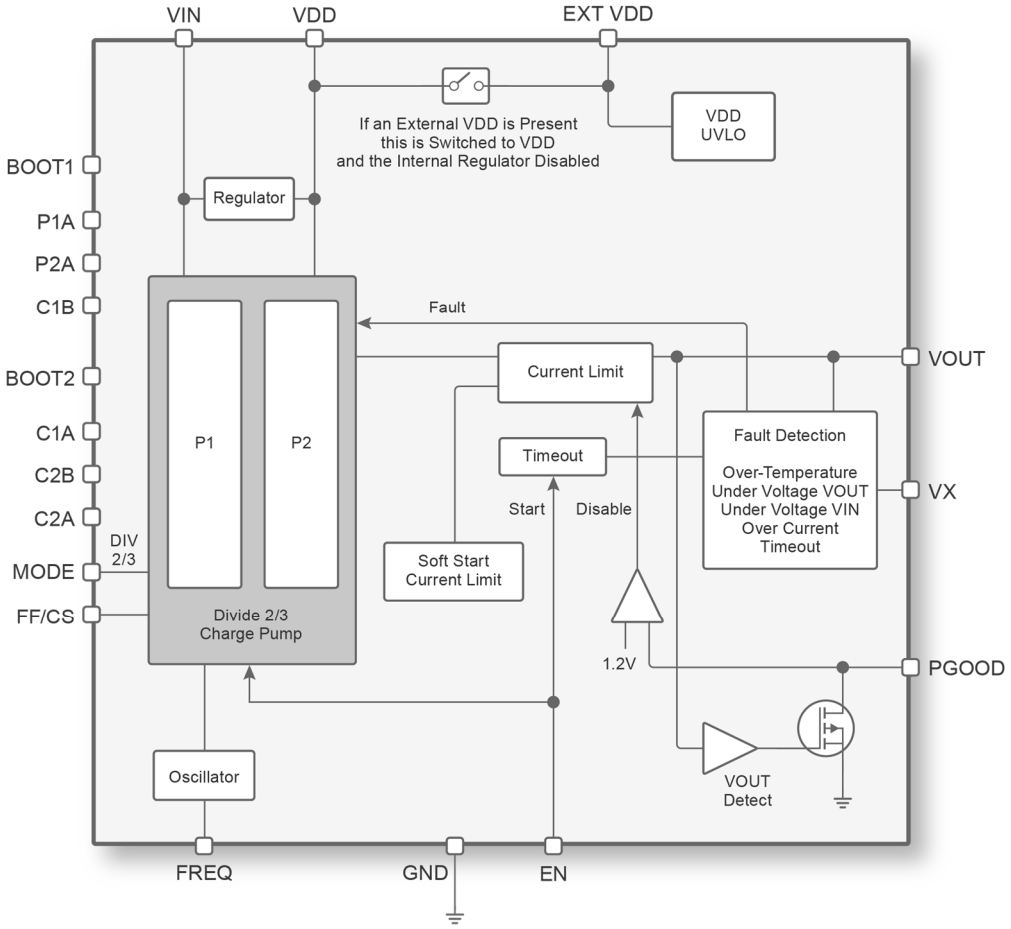


Figure 4. PE25203 Functional Block Diagram

Application Circuit

Figure 5 shows a typical application circuit configured to operate in divide-by-2 and divide-by-3 modes. For details about component values, see Application Information on page 25.

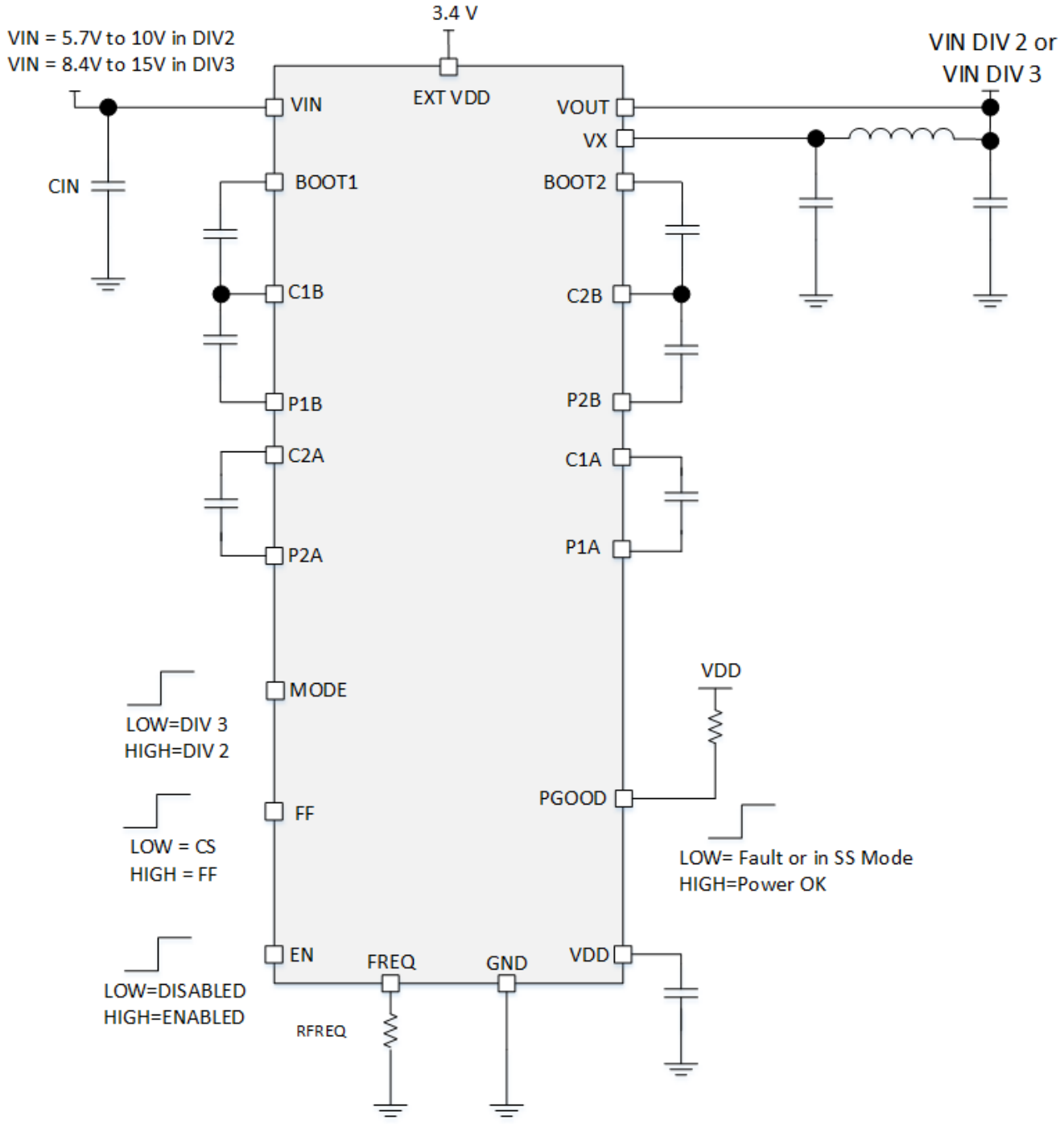


Figure 5. PE25203 Typical Application Circuit

Typical Performance Data

Figure 6–Figure 31 show the PE25203 typical performance data and were measured according to the capacitances defined in the application circuit (see Figure 5). In all cases, the figures show performance with FREQ=GND.

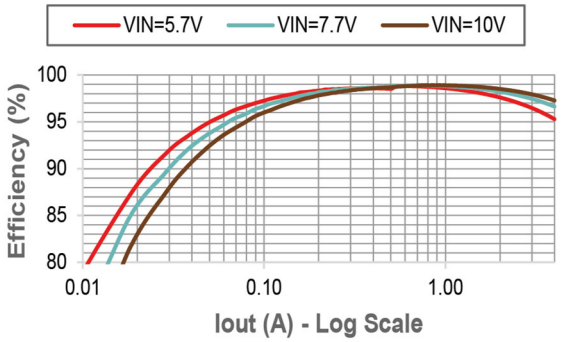


Figure 6. DIV 2 V_{IN} = 5.7, 7.7, 10V. Efficiency vs. load current, fixed frequency, 25 °C, 200 kHz, internal V_{DD}

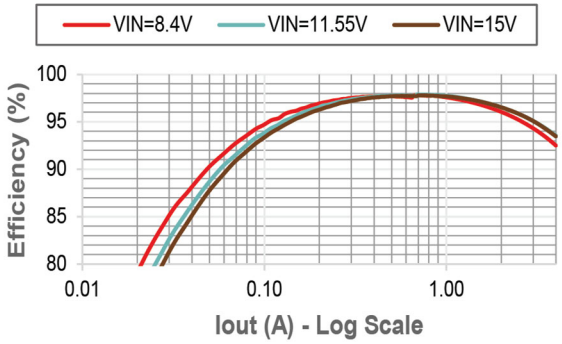


Figure 7. DIV 3 V_{IN} = 8.4, 11.55, 15V. Efficiency vs. load current, fixed frequency, 25 °C, 200 kHz, internal V_{DD}

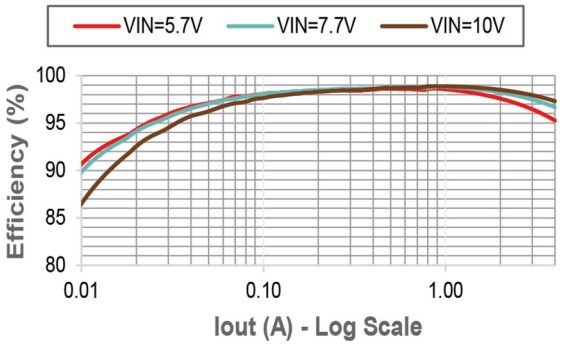


Figure 8. DIV 2 V_{IN} = 5.7, 7.7,10V. Efficiency vs. load current, cycle skip, 25 °C, 200 kHz, Internal V_{DD}

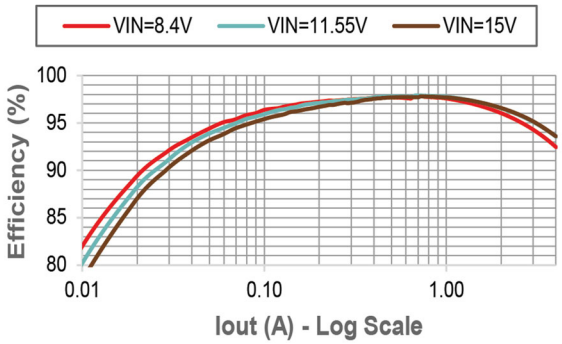


Figure 9. DIV 3 V_{IN} = 8.4, 11.55, 15V. Efficiency vs. load current, cycle skip, 25 °C, 200 kHz, internal V_{DD}

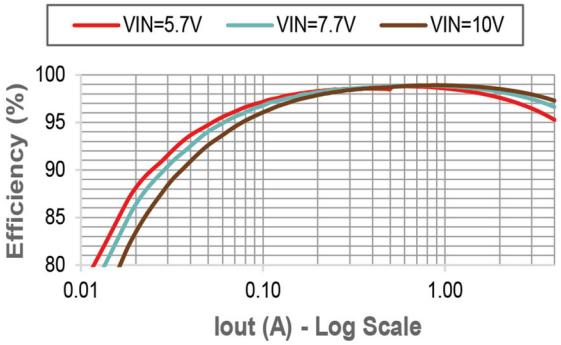


Figure 10. DIV 2 V_{IN} = 5.7, 7.7, 10V. Efficiency vs. load current, fixed frequency, 25 °C, 200 kHz, external V_{DD}

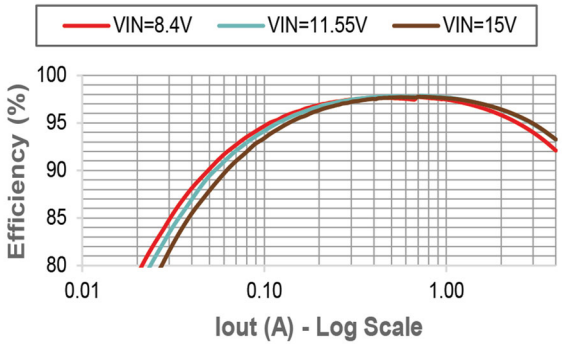


Figure 11. DIV 3 V_{IN} = 8.4, 11.55, 15V. Efficiency vs. load current, fixed frequency, 25 °C, 200 kHz, external V_{DD}

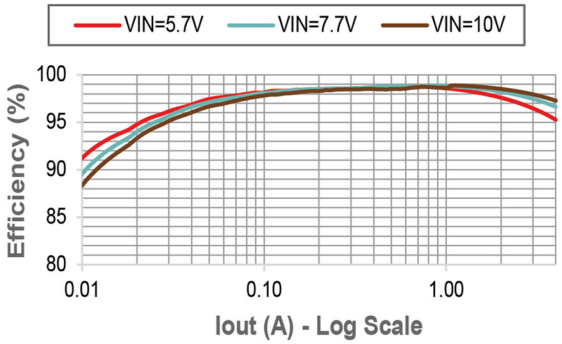


Figure 12. DIV 2 V_{IN} = 5.7, 7.7, 10V. Efficiency vs. load current, cycle skip, 25 °C, 200 kHz, external V_{DD}

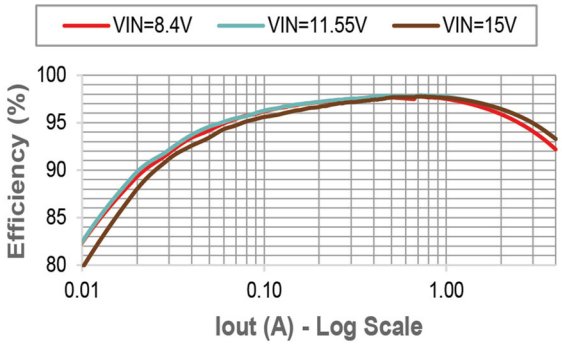


Figure 13. DIV 2 V_{IN} = 8.4, 11.55, 15V. Efficiency vs. load current, cycle skip, 25 °C, 200 kHz, External V_{DD}

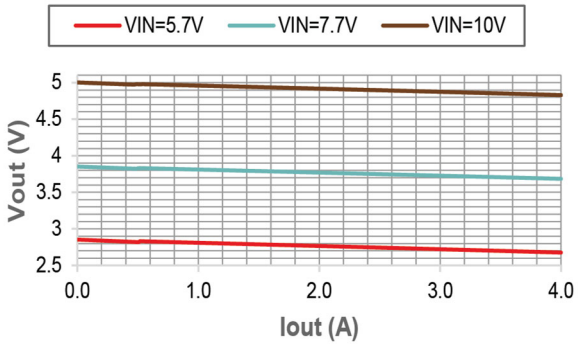


Figure 14. DIV 2 V_{OUT} vs. load current, fixed frequency, 25 °C, 200 kHz, internal V_{DD}

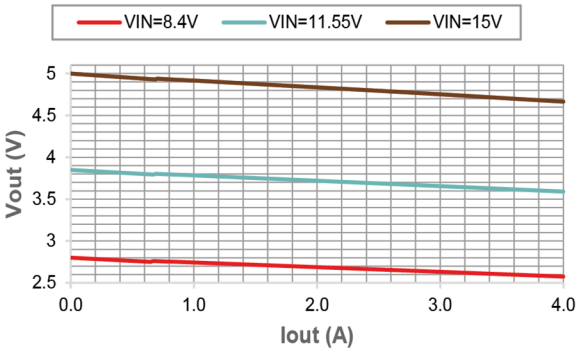


Figure 15. DIV 3 V_{OUT} vs. load current, 25 °C, fixed frequency, 25°C, 200 kHz, internal V_{DD}

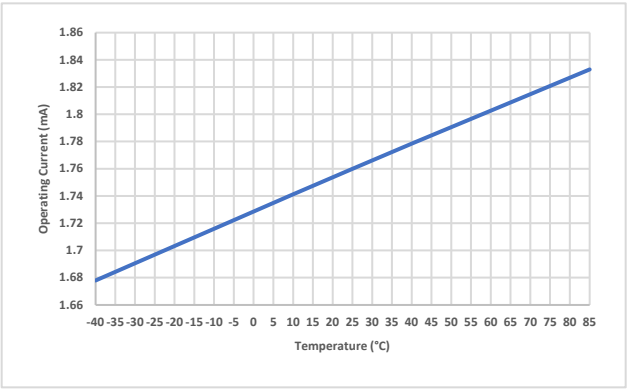


Figure 16. Operating current vs. temperature, DIV 2 V_{IN} = 7.7, cycle skip, 200 kHz, internal V_{DD}

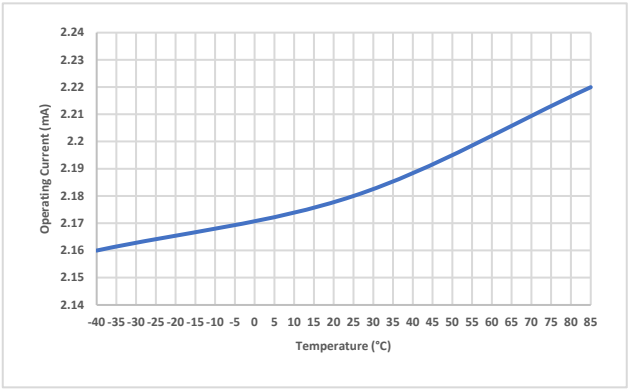


Figure 17. Operating current vs. temperature, DIV 3 V_{IN} = 11.55, cycle skip, 200 kHz, internal V_{DD}

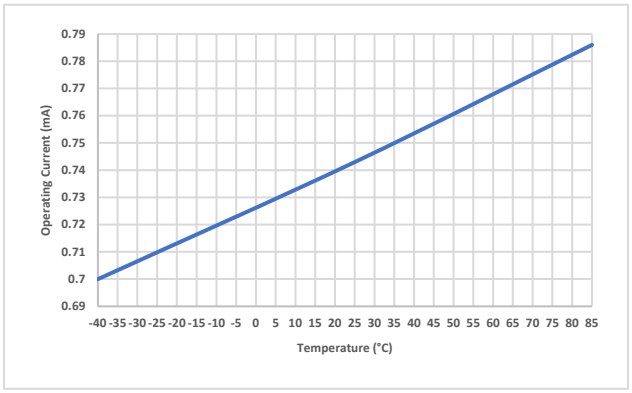


Figure 18. Operating current vs. temperature, DIV 2 V_{IN} = 7.7, cycle skip, 200 kHz, internal V_{DD}

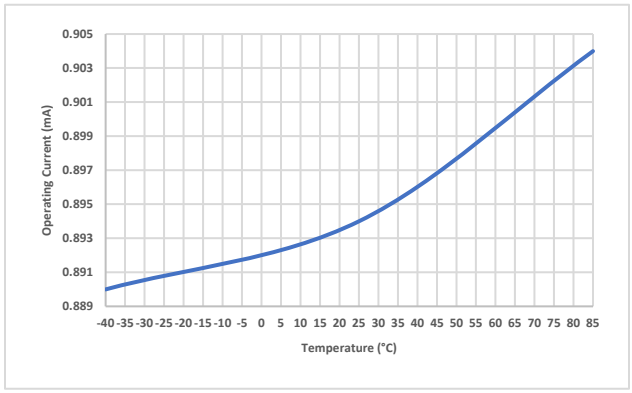


Figure 19. Operating current vs. temperature, DIV 3 V_{IN} = 11.55, cycle skip, 200 kHz, internal V_{DD}

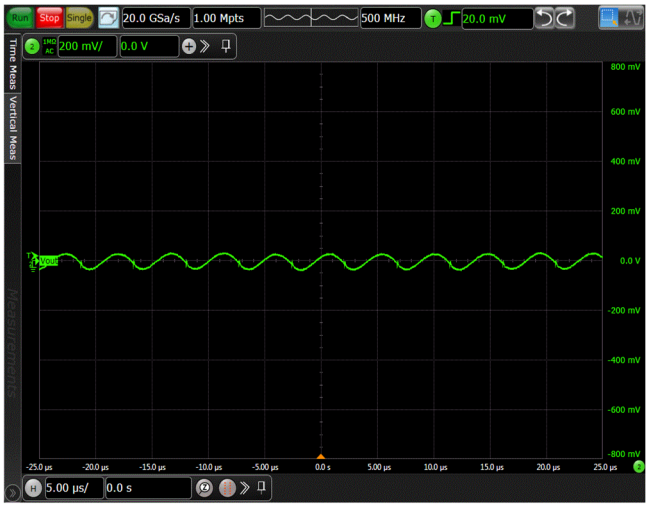


Figure 20. Divide-by-2 Ripple (@ I_{LOAD} = 4A), 7.7V

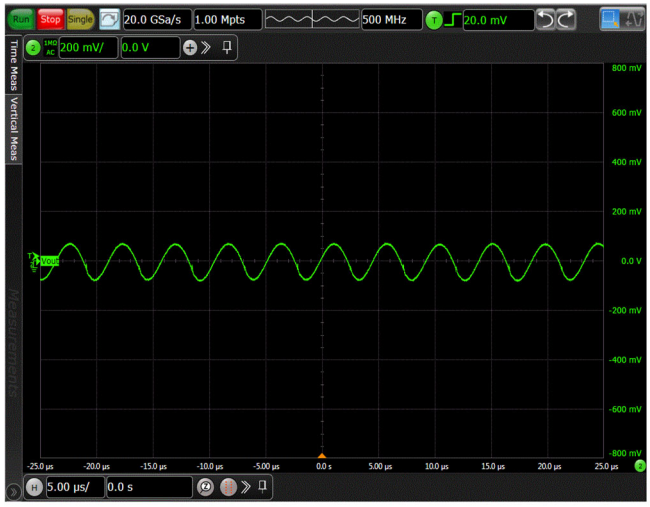


Figure 21. Divide-by-3 Ripple (@I_{LOAD} = 4A), 11.55V

Figure 22. DIV2 Start up, C_{LOAD} = 100 µF

Figure 23. DIV3 Start up, C_{LOAD} = 100 µF

Figure 24. Load transient (0.1A - 4A) V_{IN} = 7.7V DIV2 C_{LOAD} = 100 µF

Figure 25. Load transient (0.1A - 4A) V_{IN} = 11.55V DIV3 C_{LOAD} = 100 µF

Figure 26. Auto-switch MODE DIV3 to DIV2 transition, I_{OUT} = 1.5A

Figure 27. Auto-switch MODE DIV2 to DIV3 transition, I_{OUT} = 1.5A

Figure 28. Line transient 6-9V I_{LOAD} = 4A DIV2 C_{LOAD} = 100 µF

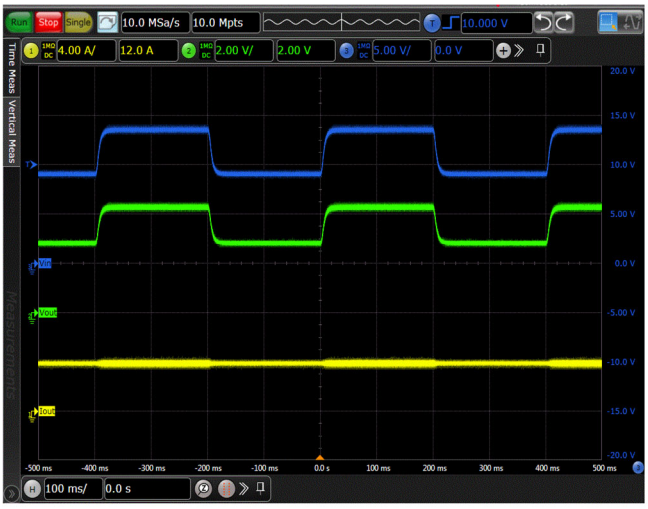


Figure 29. Line transient 9-13.5V I_{LOAD} = 4A DIV3 C_{LOAD} = 100 µF

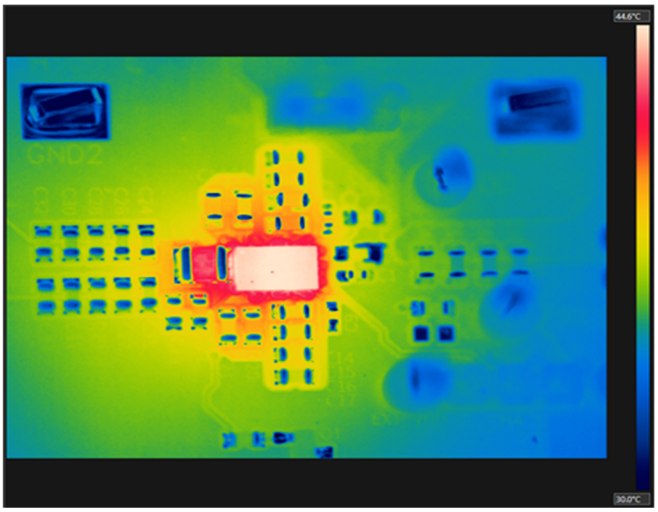


Figure 30. Thermal plot divide-by-2 I_{OUT}= 4A, (V_{IN} = 7.7V and V_{OUT} = 3.72V) P_{DISS} = 0.56W, top case temperature = 44.6 °C at T_A = 25 °C

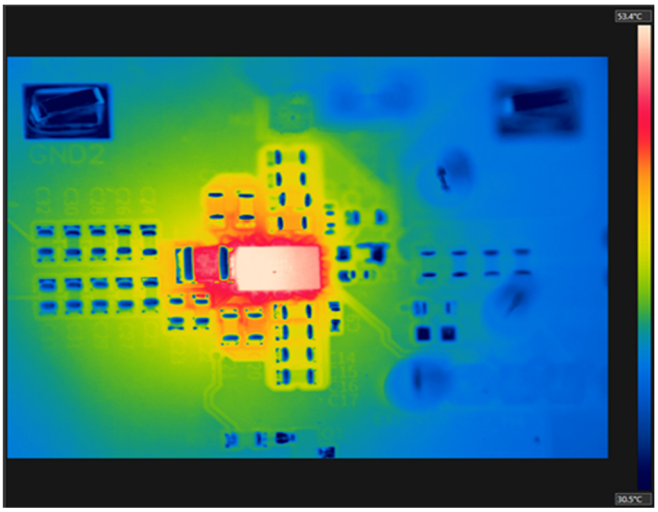


Figure 31. Thermal plot divide-by-3 I_{OUT}= 4A, (V_{IN} = 11.55V and V_{OUT} = 3.62V) P_{DISS} = 0.99W, top case temperature = 53.4 °C at T_A = 25°C

Detailed Description

The PE25203 is a dual-phase, charge pump-based, DC-DC converter that is designed to operate in either a fixed divide-by-2 or divide-by-3 mode. The output voltage range supported is from 2.85V to 5.0V with load currents of up to 4A and up to 20W delivered to the external load. The charge pump can be configured to operate over a range of frequencies using the FREQ pin to allow easier optimization of EMI vs. efficiency for the target application.

Voltage Division and MODE Pin

The device configuration is set by connecting the MODE pin to a voltage greater than 1.2V or less than 0.4V. This pin can be driven dynamically to change between divide-by-2 and divide-by-3 mode.

If the ability to change the MODE is not required, connect it to ground for divide-by-3 or a voltage higher than 1.2V for divide-by-3 mode. To minimize quiescent current, connect MODE to VIN in divide-by-2 mode.

The MODE pin can be driven dynamically to change division ratios. For more on the limitations when in this mode, see Driving the Voltage Division Pin Dynamically on page 15.

Table 6. MODE Pin

MODE Pin	Division Ratio
<0.4V	Divide-by-3
>1.2V	Divide-by-2

Drive the MODE pin low or high. By default, the MODE pin is pulled down with an internal resistor.

The PE25203 implements all the power switches and switch control to operate in divide-by-2 or divide-by-3 mode. The same PCB design can support either mode. If only operating in divide-by-2 mode, it is possible to achieve small efficiency improvements if the C1B/C2A, and C2B/C1A pins are shorted to each other at the PCB level.

These shorts operate in parallel with internal power switches in the PE25203, decreasing the switch impedance and slightly reducing losses as a result. The C1B/C2A and C2B/C1A pins are placed adjacent to each other on the chip pin-out to help make this board-level connection easier for exclusive divide-by-2 applications.

Driving the Voltage Division Pin Dynamically

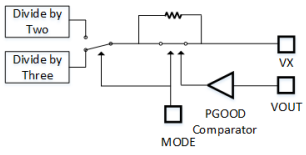
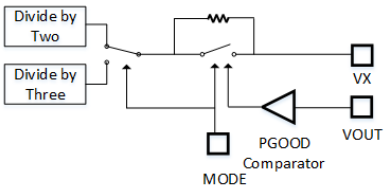
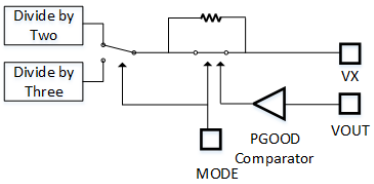
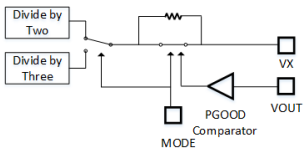
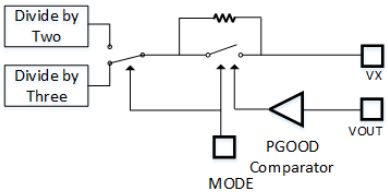
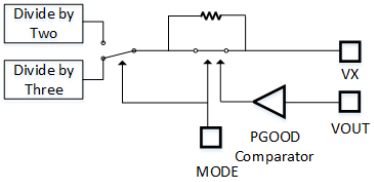
The MODE pin can be driven during operation to change the division ratio. This can be useful to extend the operating life of an application with a battery stack of three-cells. As the input voltage decays, the device can be switched from divide-by-3 mode to divide-by-2 mode. As the cell stack charges, the device can be switched from divide-by-2 mode to divide-by-3 mode.

To change from divide-by-3 mode to divide-by-2 mode, the MODE pin should be switched from logic low to logic high. To change from divide-by-2 mode to divide-by-3 mode, switch the MODE pin from logic high to logic low.

Before the transition, the device operates normally in divide-by-2 MODE or divide-by-3 MODE, depending on the logic level on the MODE pin. In this state, the PE25203 can supply 4A output current.

During the transition, the charge pump frequency is switched to a fixed frequency at 200 kHz per phase, and the FETs in the charge pump are driven in a higher impedance mode. In the Table 7 diagrams below, this is represented by an output resistor.

Table 7. Dynamic Changeover Stages of Operation

Transition	Before Transition	During Transition	After Transition
Divide-by-3 to Divide-by-2			
Divide-by-2 to Divide-by-3			

When the charge pump frequency is switched to the fixed frequency of 100 kHz, the MODE pin change is delayed for a period of about 50 µs. Depending on the load on the output during this time, a small dip in output voltage can be seen before the output starts to transition.

When the output is transitioning, the device supplies both the current to charge the output capacitor and the current to supply the downstream load. Because of this, the rate of rise and decline of the output voltage is dependent on the downstream load and output capacitance.

If the device is held in the transition region for a prolonged time at high load currents, it is possible for it to reach the over-temperature threshold and switch off in a fault mode. During the transition, limit the maximum load to 1.5A.

When changing from divide-by-2 to divide-by-3 mode, the only discharge path available from the output capacitor is through the load as a passive discharge. If the output is not loaded, during the transition from divide-by-2 to divide-by-3 mode, the charge pump switches to lowest switch frequency setting and waits for the output to gradually discharge.

Over-temperature Detection and Behavior

If the PE25203 enters over-temperature, it switches off as it cools down below the over-temperature threshold and then restarts.

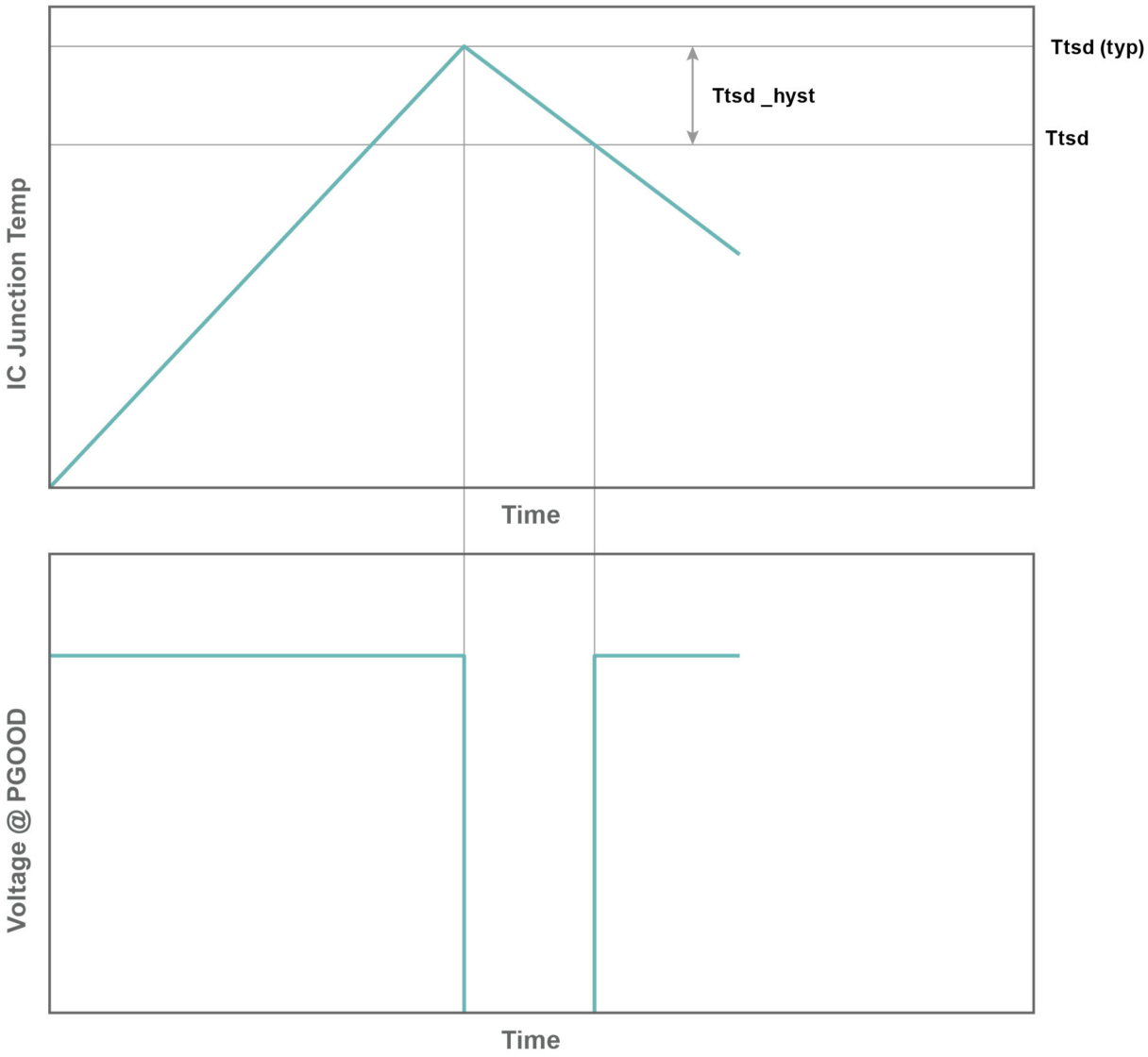


Figure 32. Over-temperature Behavior

Setting the Operating Frequency

The FREQ pin can be used to set the PE25203 operating frequency. To save a resistor, the FREQ pin can also be connected to GND to oscillate at a nominal 200 kHz. This is the frequency of oscillation at the VX pin and the charge pump frequency per phase switches at 50% of this value.

To adjust the frequency, connect an 82.5 kΩ–505 kΩ resistor between the FREQ pin and GND. Figure 33 shows the V_X switching period versus the resistance value set at the FREQ pin.

To find the required V_X switching period in µs, use the following equation:

$$V_X \text{ switching period} = (0.0093 * \text{resistance value in k}\Omega) + 0.2254$$

Using a resistor value of 505 kΩ in the equation above results in the following:

$$V_X \text{ switching period} = (0.0093 * 505) + 0.2254 = 4.92\ \mu s\ (203\ kHz)$$

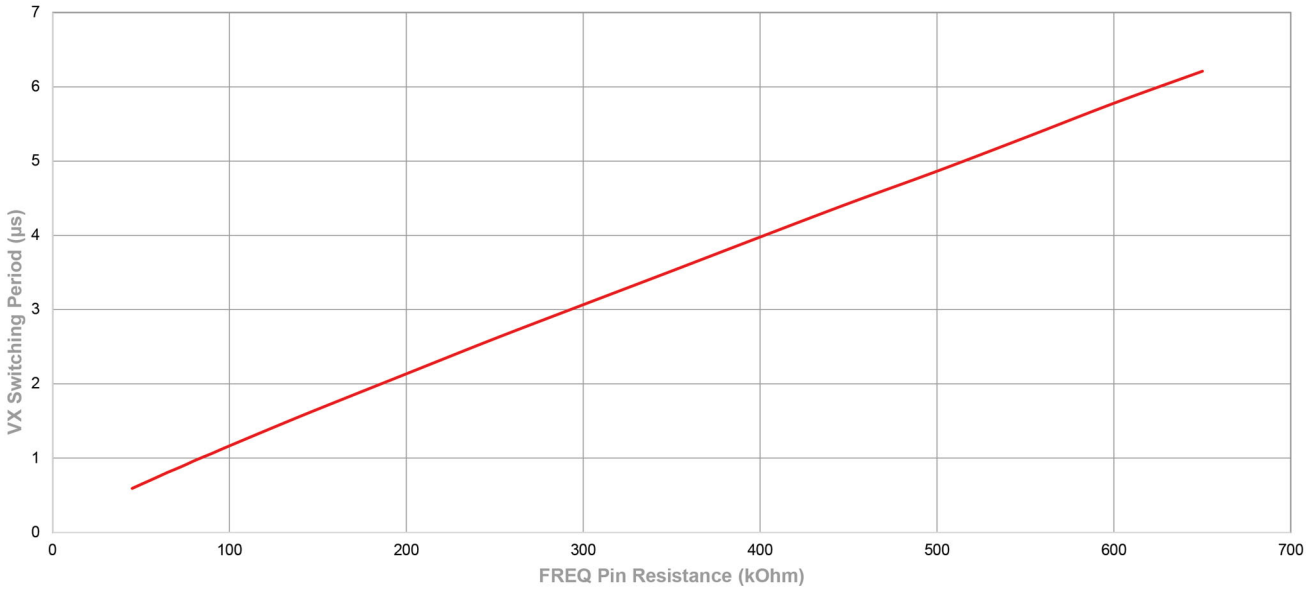


Figure 33. V_X Switching Frequency vs. Resistance on the FREQ Pin

Startup – EN, VIN, and VDD Relationship

The PE25203 has an enable input pin, EN, which was designed to be compatible with typical low voltage digital I/O levels so that an external controller can easily drive it. EN can also be connected to the V_{IN} pin, however, if external power sequencing or control is not required.

In the event the EN pin is held low until V_{IN} has reached its nominal voltage, the PE25203 follows the initialization sequence shown in Figure 34.

The internally regulated supply voltage (V_{DD}) is nominally set around 3.6V and is derived from V_{IN} or external V_{DD} if it is present.

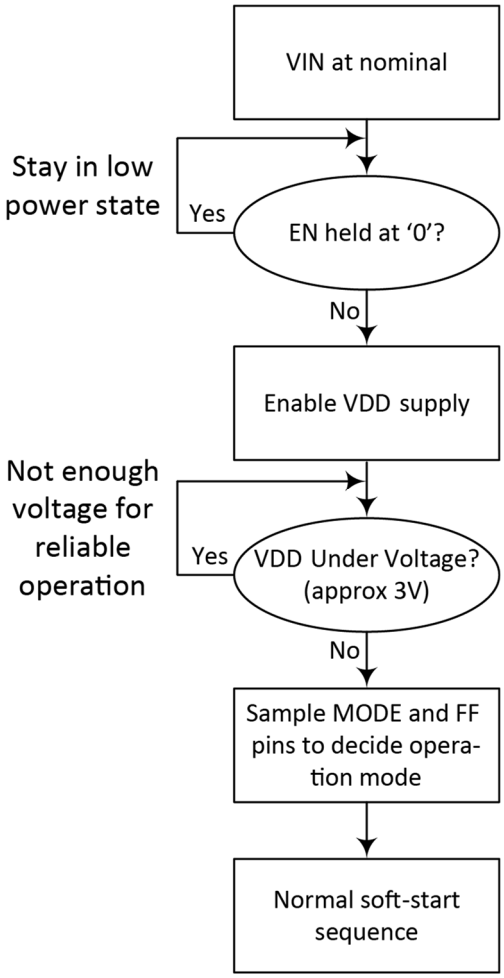


Figure 34. EN-controlled Startup Flow

During the initial startup and soft start sequence, the state of the MODE pin is initially sampled, and any changes are ignored until the device is in normal operation and the PGOOD pin is high.

Soft Start

In soft start, the PE25203 operates in a high resistance mode to ensure that it exits the soft-start phase and transitions to full power switching mode when the V_{OUT} voltage has reached 95% of the target voltage. The PGOOD tri-states, and the external resistor pulls PGOOD high at the same time, assuming that no other faults are present. Use the PGOOD pin as a power sequencing signal to enable the downstream converters connected to the PE25203 output.

Do not apply a load to the PE25203 during soft start, or this can cause failure in startup or prolong the startup duration.

In the event of a fault situation in which V_{OUT} is shorted, after the timeout period the PE25203 enters a cooldown period before it attempts to restart.

Figure 35. Soft-start Waveform into a Discharged Output Voltage

Figure 36. Soft Start into a Pre-charged Load

Figure 35 shows how the PE25203 leaves the soft-start mode and enters full power. Throughout the soft start, the PE25203 operates the charge pump in a fixed-frequency mode of 200 kHz, regardless of how the FREQ pin is configured.

Soft-start Timeout

When the PE25203 first tries to supply power to the load, it uses a soft-start circuit so that the power level is limited. Using a soft start has no significant side effects if the start-up is “normal.”

In the event of the PE25203 starting up into a fault, the soft start helps to manage the power being supplied to the fault and limits the PE25203 power dissipation. In normal, fault-free operation, the soft-start timeout is invisible if the soft-start current can ramp V_{OUT} to the target voltage of 95% of the division ratio within 10 ms. In the event of a fault, the soft-start timeout occurs when V_{OUT} does not ramp to the target voltage within the expected time. In this case, the soft-start timeout causes power to the load to be stopped, and the PE25203 enters a controlled shutdown sequence. When the soft-start sequence is complete—and after a cooldown time of approximately 40 ms—the PE25203 attempts the start-up again.

Figure 37 shows the flow for a persistent fault case. The fault initially triggers the recovery step, and then—assuming the charge pump remains enabled—the PE25203 attempts to soft start again. Assuming that V_{OUT} is still held low by the fault, the PE25203 goes into a *hiccup* mode in which the soft-start timeout trips cause the cooldown phase to restart. The loop in Figure 37 repeats for as long as the fault is present and the PE25203 remains enabled.

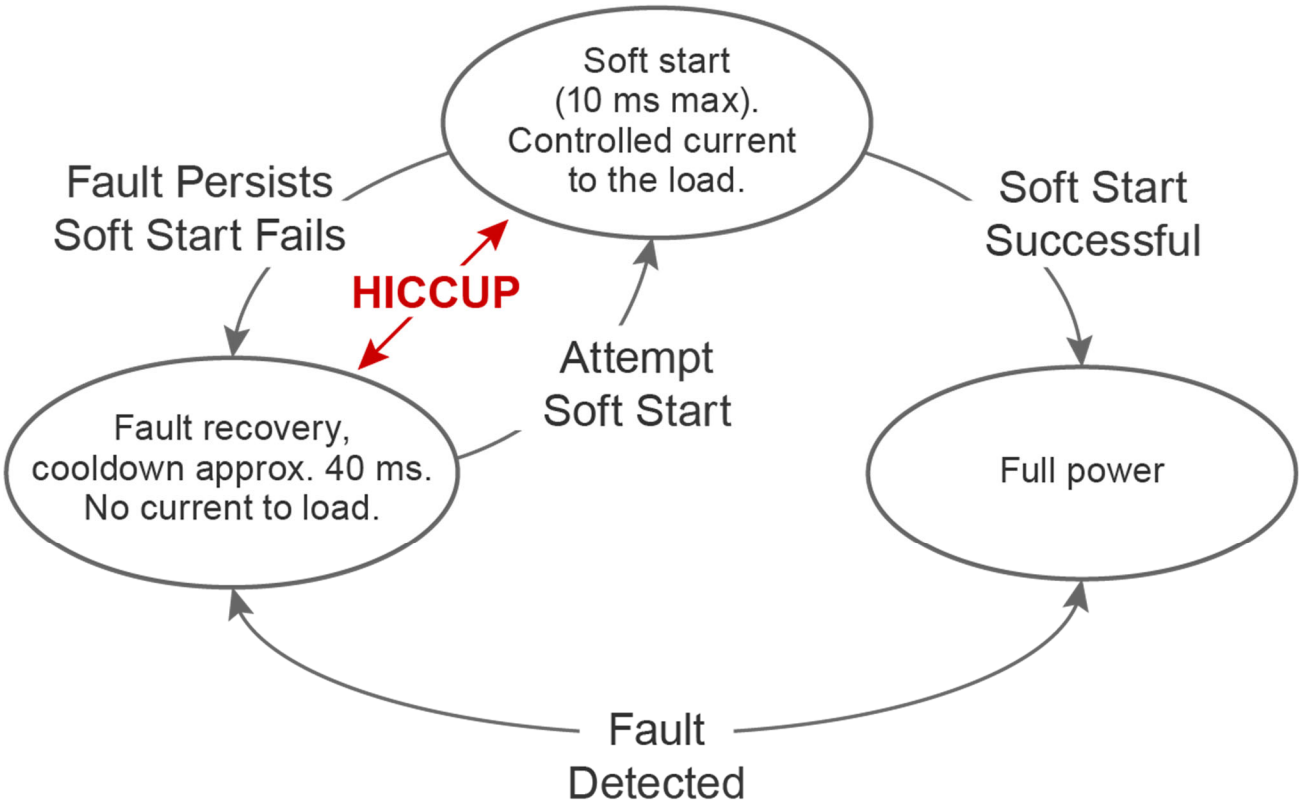


Figure 37. Hiccup Mode for Some Types of Persistent Faults

Protection Modes

To protect both the system and the PE25203 internal circuitry, multiple fault detection circuits are built in.

Table 8 lists a summary of the various protection modes.

Table 8. Protection Modes

Detector	Persistent Fault*	Response Time	Effect of Fault on the PE25203
V_{IN} under-voltage	Yes	ns	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown and stays off until the V_{IN} voltage exceeds the under-voltage lockout threshold.
V_{OUT} under-voltage	No	ns	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown. After a cooldown period of about 40 ms, the PE25203 attempts to soft start again.
VX over-voltage	Yes	µs	PGOOD goes low. The PE25203 disconnects from V_{IN} so that no further power passes from V_{IN} to the load. A load must be present to discharge the output. When the V_X voltage falls below the V_{XOVP} threshold, the power stage fully turns off through a soft shutdown and the device restarts.
I_{LOADSC} current	No	ns	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown. After a cooldown period of approximately 40 ms, the PE25203 attempts to soft start again. For details, see ILOAD Short Circuit and Over-current Protection on page 24.
V_{OUT} short circuit	No	µs	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown. After a cooldown period of approximately 40 ms, the PE25203 attempts to soft start again.
I_{LOADOC}	No	µs	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown. After a cooldown period of approximately 40 ms, the PE25203 attempts to soft start again. For details, see ILOAD Short Circuit and Over-current Protection on page 24.
Over-temperature thermal shutdown	Yes	µs	PGOOD goes low. The PE25203 power stage is turned off through a soft shutdown and stays off until the die temperature has reduced below the thermal shutdown level minus hysteresis.
V_{DD} under-voltage	Yes	µs	PGOOD goes low. The PE25203 power stage is turned off immediately. This is an uncontrolled shutdown. The charge pump remains off until the internal VDD recovers.
Soft-start timeout	No	µs	If V_{OUT} does not reach the target voltage inside the soft-start timeout period of 10 ms, the PE25203 goes into the cooldown state for approximately 40 ms before it attempts to soft-start again.
PGOOD held—or set—low when expected high	Yes	µs	From full power, the PE25203 initially returns to a limited load current soft-start mode. If the PGOOD signal is held low for less than the soft-start timeout period, the PE25203 returns to full power operation. If PGOOD=0 exceeds the soft-start timeout, the PE25203 loops through soft-start, cooldown, soft-start, or cooldown until PGOOD is allowed to go high.

V_{OUT} over-voltage in divide-by-2 to divide-by-3 transition	Yes	–	In dynamic switchover from a divide-by-2 to divide-by-3 and the output is not loaded during the transition. Then the PE25203 stays at the reduced clock frequency mode indefinitely until the output is discharged.
Note: * A persistent fault keeps the PE25203 in a fault state for as long as the fault is present. A non-persistent fault does not prevent the PE25203 from re-enabling after the fault recovery time has been applied.			

PGOOD Operation

The PE25203 has an open drain *power good* pin, PGOOD. For correct operation, PGOOD must have an external pull-up to V_{IN}, V_{DD} or an external voltage >1.5V.

The PE25203 holds the PGOOD pin low whenever the charge pump is in soft-start, or when a fault condition is detected and being managed.

When the PE25203 allows PGOOD to be pulled high, the charge pump is ready to support the full load current.

The PGOOD pin of a disabled device is NOT pulled low. When EN=0, the PGOOD pin can be ignored.

V_{IN} Undervoltage and Thermal Shutdown Faults

The V_{IN} under-voltage and thermal shutdown faults are grouped together because the effect they have on the charge pump is similar. If either of these faults is present when the charge pump is first enabled, the charge pump starts to power-up but holds before any power—even soft-start current—is applied to the load. The charge pump holds in this state until both faults are clear, regardless of how long this takes. V_{IN} under-voltage and thermal shutdown faults are considered *persistent* because they hold the charge pump disabled until the fault clears.

In the case of V_{IN} under-voltage, it is unlikely that the charge pump can support the full load current when V_{IN}—and therefore V_{OUT}—is too low. This is not optimal for the PE25203 or for the load, so the charge pump waits for V_{IN} to improve/recover.

An over-temperature fault is only likely to occur when the PE25203 is dissipating too much internal power. This fault normally results from some other fault condition, or from choosing to operate the PE25203 with low efficiency and high-power levels. In the event of over-temperature, the PE25203 could start to drift out of guaranteed performance specifications which would not be optimal for the system. To recover from over-temperature, the PE25203 stops switching—so it stops dissipating power—and it starts to cool-down towards the ambient temperature.

When V_{IN} under-voltage or an over-temperature fault are detected during normal operation, the PE25203 enters a controlled shutdown sequence with an unlimited cooldown period (there is a typical cooldown time of approximately 40 ms). When the faults clear, the PE25203 goes through a normal soft-start sequence and attempts to start-up.

V_X Over-voltage Protection

The V_X over-voltage fault detector is intended to protect both the PE25203 and the output load from over-voltage conditions. To ensure that over-voltage at V_X does not propagate to V_{OUT}, the V_X over-voltage detection circuit is designed to operate quickly. V_X over-voltage faults are treated differently from most of the other fault flags.

The first response is to disconnect the PE25203 power stage from V_{IN}. The path for power from V_{IN} to V_{OUT} will be opened to remove one source of the over-voltage. The charge pump will not continue to clock (and a fixed-frequency mode will be temporarily forced regardless of the FF pin connection). Clocking the charge pump without a connection to V_{IN} will create a path from V_X to GND which will act to discharge V_X. It is likely that V_X will discharge very rapidly and as a result the V_X fault will be cleared quickly.

To complete the recovery from the V_X over-voltage, the PE25203 goes into a controlled shutdown sequence. When the soft-start sequence is complete—and after a cooldown time of approximately 40 ms—the PE25203 attempts to restart.

The initial response to the V_X over-voltage of disconnecting V_{IN} and continuing to clock will continue—with no time limit—for as long as the V_X over-voltage fault is detected. In most cases this is expected to clear the V_X over-voltage quickly (within a few charge pump clocks). In the unlikely event that V_X over-voltage is detected because of over-voltage at V_{OUT} (for example due to a second power source in the system) the PE25203 attempts to discharge V_X (and hence V_{OUT}) through the switching action and the flying capacitors for an unlimited period. While in this V_X over-voltage recovery state, some of the normal fault detectors (for example load current detectors) will not operate and as a result using a V_X over-voltage to recover from a system-caused V_{OUT} over-voltage is not recommended.

I_{LOAD} Short Circuit and Over-current Protection

The I_{LOAD} fault detection flags both operate in the same way by sensing the current being drawn from VIN. The short circuit flag (I_{LOADSC}) is a fast-acting fault with a high trip threshold and is designed to capture instantaneous fault levels (for example, from a dead short occurring at V_{OUT}). The over-current protection flag (I_{LOADOC}) can be considered as a longer-term average current type of measurement. As a result, the trip point can be set closer to the nominal 4A maximum output load. The over-current protection trips when the PE25203 is operated outside the recommended operating conditions.

The reaction to both I_{LOADSC} and I_{LOADOC} faults is the same. The PE25203 enters a controlled shutdown sequence. When the soft-start sequence is complete—and after a cooldown time of approximately 40 ms—the PE25203 attempts to restart. Persistent fault conditions can prevent the charge pump from restarting successfully, for example, in the event of a hard fault to GND at V_{OUT} (which would trigger I_{LOADSC}).

V_{OUT} Short Circuit and Under-voltage Protection

The V_{OUT} short circuit and under-voltage fault detectors work in similar ways. They compare the measured value at V_{OUT} with the expected value derived from V_{IN} (so V_{OUT} is compared with $V_{IN}/2$ or $V_{IN}/3$, depending on the MODE pin setting). The V_{OUT} short circuit fault is designed to operate very quickly, but only when V_{OUT} is substantially below the target voltage (60% of the target). The V_{OUT} under-voltage fault is designed to be slower and represent more of an averaged value. The V_{OUT} under-voltage flag trips when V_{OUT} drops below 80% of the target (V_{UVP}).

The V_{OUT} short circuit detector is designed to operate in parallel to the I_{LOADSC} fault to give more independence from the external component values. For example, the result of a direct short to GND at V_{OUT} while the PE25203 is operating at 4A depends partly on the inductor between V_X and V_{OUT}. It is possible that V_{OUT} could reach the V_{OUTSC} threshold sooner than I_{LOADSC} reaches the short circuit current limit, so supporting both fault detectors provides a better opportunity to stop the power from going to the fault condition as soon as possible.

The V_{OUT} under-voltage detector trips when V_{OUT} drops below 80% of the target voltage. It is important that the external components are chosen so that the expected transient loads do not trip the V_{UVP} threshold. In effect, the application must ensure that the load dependency causes less than 20% deviation from the nominal V_{OUT}.

If the V_{OUT} short circuit or under-voltage occurs, the effect on the charge pump is similar, and the same as for I_{LOADSC}. The PE25203 enters a controlled shutdown sequence. When the soft-start sequence is complete—and

after a cooldown time of approximately 40 ms—the PE25203 goes through a normal soft-start sequence and attempts to restart.

V_{DD} Under-voltage Protection

The V_{DD} under-voltage fault condition is potentially serious. Much of the charge pump control and many of the fault detection flags use the V_{DD} supply internally. For this reason, V_{DD} must not be externally loaded to ensure that V_{DD} under-voltage is not triggered by external circuit load.

When V_{DD} is pulled below the under-voltage trip voltage—approximately 3V—the charge pump is shut down immediately, PGOOD is pulled low, and no further power is supplied to the load. The internal V_{DD} regulator has an internal short circuit current limit—so that the V_{DD} fault itself does not damage the PE25203—but the effects of stopping the supply to the load in an unplanned way could be serious. The PE25203 is designed to withstand the immediate shutdown, but not all the effects of the shutdown are controlled by the PE25203 itself. For example, the inductor can cause a voltage spike as the load current is abruptly cut off. The voltage spike depends on the external inductor, the load capacitance, and the load current at the instant of shutdown. Consideration of the PE25203 absolute maximum ratings must be made in the end application so that a V_{DD} short can be managed without exceeding the device ratings.

The V_{DD} under-voltage fault is “persistent” in that the PE25203 remains disabled for as long as V_{DD} is held below the under-voltage threshold. When the fault clears, the PE25203 samples the FF and MODE pins again to get the chip configuration, then enters a soft start sequence before allowing PGOOD to go high to flag that full-power operation is possible.

Capacitor Imbalance

The PE25203 implements proprietary algorithms to handle capacitor imbalance in real-world solutions. Because the PE25203 is a charge pump-based DC-DC device, it uses four flying capacitors. In any real-world solution, the flying capacitor components will not be ideal and will certainly not be identical. The PE25203 can work with extremes of capacitance values (for example, phase 1 capacitors at +20% of nominal value and phase 2 capacitors at -20% of nominal value). The proprietary algorithms allow full power to be supplied to the load and help prevent capacitor imbalance from inducing large ripple at the V_X pin (and hence also higher ripple at V_{OUT}).

Application Information

The PE25203 is a charge pump-based DC-DC ratiometric converter. It is a high-efficiency bus converter in which the output follows the input by a fixed ratio of divide-by-2 or divide-by-3. Because of its architecture, there are differences from conventional inductive buck converters.

Application Schematic

Figure 38 shows a typical application circuit with details of links, corresponding modes of operation, and suggested component values.

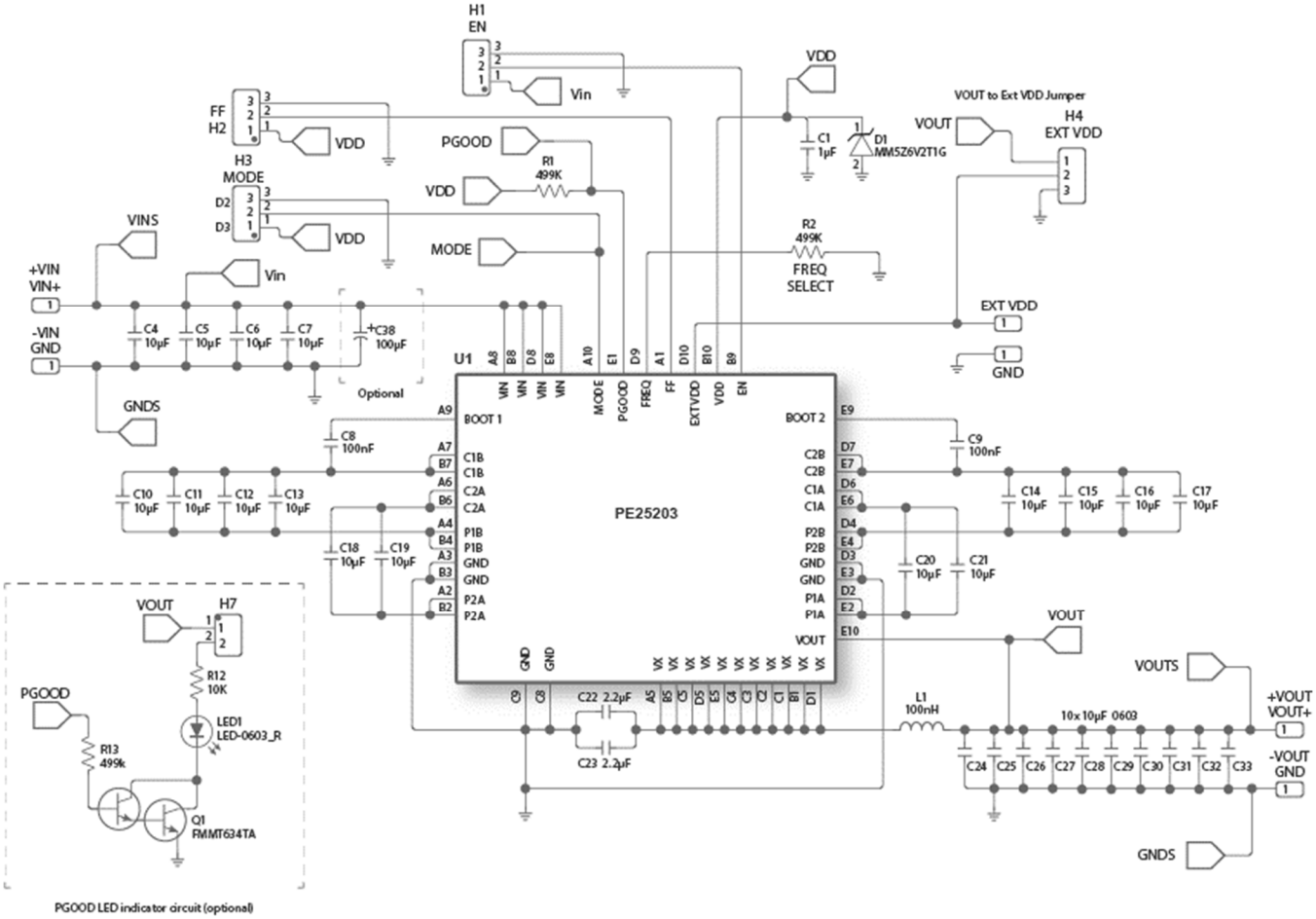


Figure 38. Detailed Application Schematic Circuit

Application Circuit Part List

Table 9 lists the pSemi recommended parts.

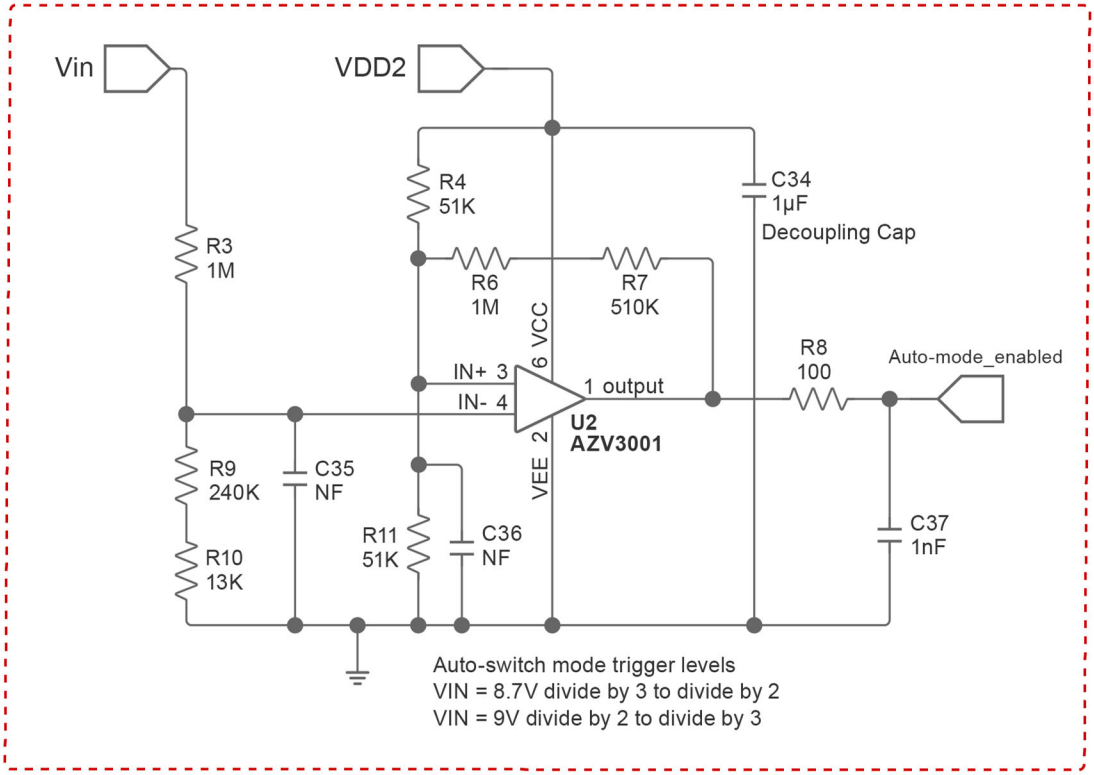
Table 9. pSemi Recommended Parts

Ref. No.	Value	Part Size	Part Number
C1	1 µF 6.3V X7R or better	0402	GRM155R70J105KA12D
C4,C5,C6,C7,C10,C11,C12, C13,C14,C15,C16,C17,C18, C19,C20,C21	10 µF 25V X5R or better	0603	GRM188R61E106KA73D
C8,C9	100 nF 100V X5R or better	0402	GRM155R62A104KE14D
C22, C23	2.2 µF 25V X5R or better*	0402	GRM155C81C225ME15D (X6S) GRM155R61E225KE11D (X5R)
C24,C25,C26,C27,C28,C29, C30,C31,C32,C33	10 µF 6.3V X5R	0603	GRM188R60J106ME47D
D1	Diode Zener 6.2V 500 MW	SOD523	MM5Z6V2T1G
L1	100 nH	2.5 mm x 2 mm x 1.2 mm	TFM252012ALMAR10MTAA
R1,R2	499 kΩ	0603	RC0603FR-07499KL
U1	Divide-by-2 and -3, 4A charge pump, capacitor divider	4.545 mm × 2.715 mm x 0.576 mm	PE25203

Note: * X5R for applications with maximum $T_A \leq 85$ °C, and X6S for applications with maximum $T_A > 85$ °C but ≤ 105 °C.

Auto-switch Mode Circuit

Figure 39 shows the circuit implemented to achieve the auto-switch mode ratio of the PE25203 evaluation kit (EVK).



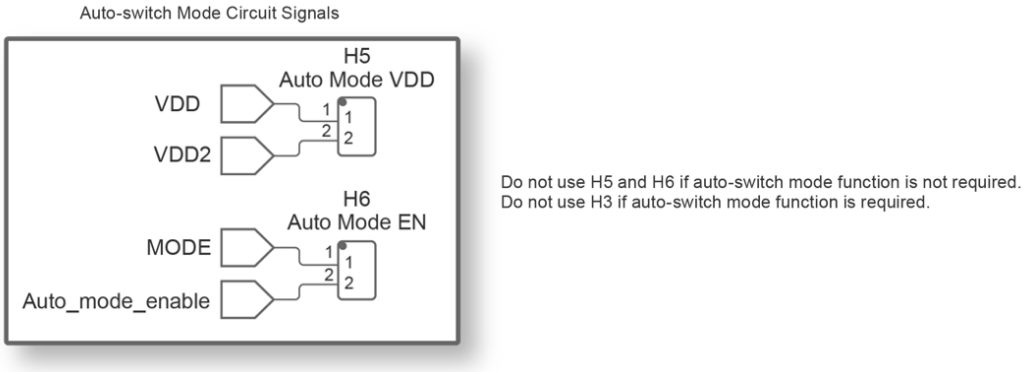


Figure 39. Optional Auto-switch Mode Circuit

Evaluation Board

Figure 40 shows the PE25203 evaluation board.

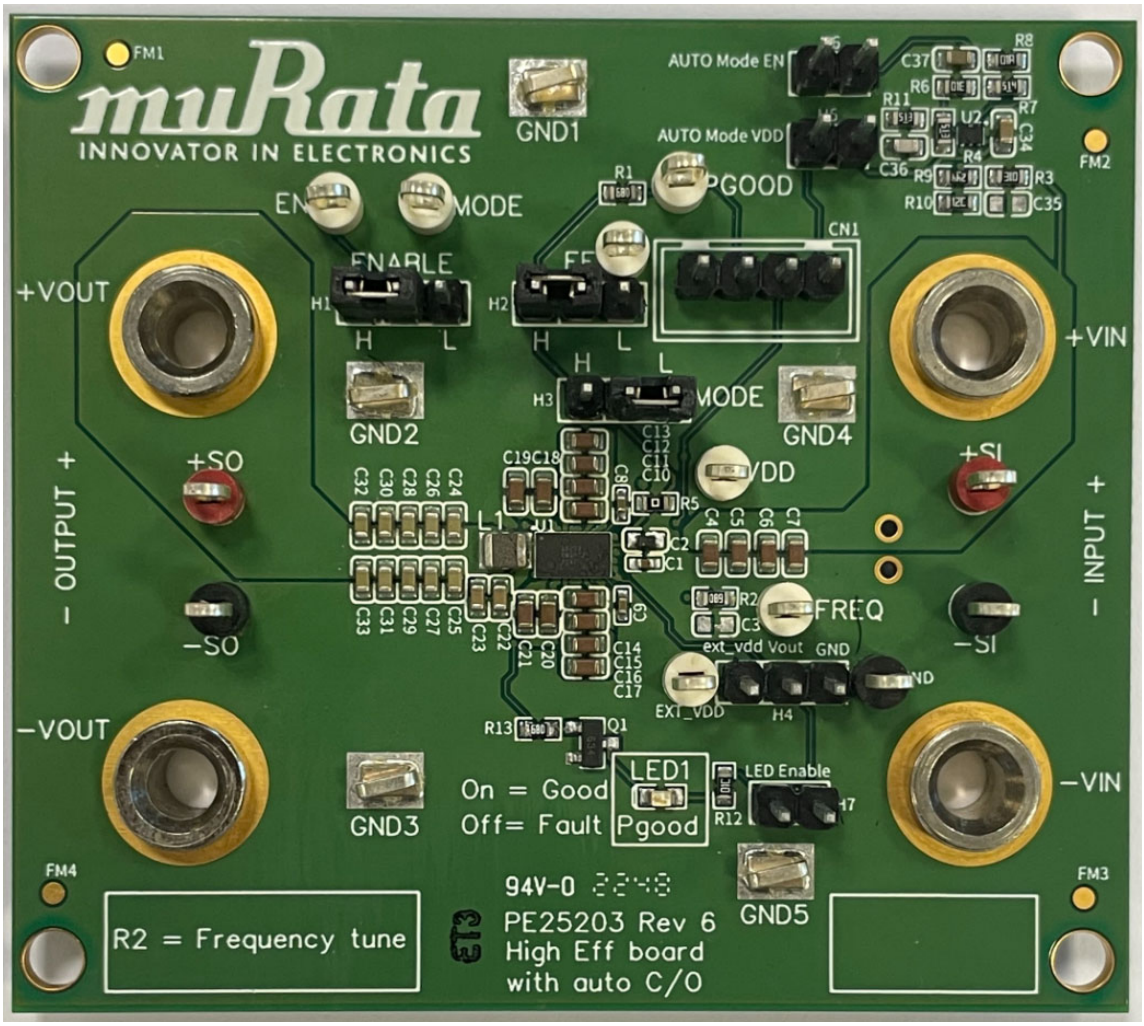


Figure 40. PE25203 Evaluation Board

Component Selection

This section describes components required by the PE25203.

Flying Capacitors

The PE25203 requires two sets of flying capacitors: the “CB” and “CA” capacitors. The CB capacitors are connected between the C*B (C1B, C2B) and P*B (P1B, P2B) pins while the CA capacitors are connected between the C*A (C1A, C2A) and P*A (P1A, P2A) pins. Both the CA and CB capacitors are important components for efficiency and must be placed as close to PE25203 as possible.

The steady state voltage across the CB capacitors is 2* V_{OUT} for divide-by-3 mode and 1* V_{OUT} for divide-by-2. The steady state voltage across the CA capacitors is 1* V_{OUT} for both divide-by-3 and divide-by-2 modes. Choose the capacitors so that the component voltage rating is higher than the steady state voltage to take ripples and spikes into account. For example, for 15V V_{IN} and divide-by-3 operation, CB capacitors with a voltage rating of 16V and CA capacitors with a 10V rating would be good choices.

The capacitance value at the applied voltage across the capacitors has a direct impact on the maximum efficiency that can be achieved. The nominal capacitance value typically drops as the voltage across the capacitor increases, depending on the voltage coefficient of the selected capacitors.

The recommended effective capacitance for CB and CA capacitors must have a typical value of 10 µF for nominal voltages. pSemi recommends that both CA and CB have similar effective capacitance under biased conditions within your operating voltage range.

While selecting the capacitor values for maximum efficiency, the switching frequency must also be considered so that the self-resonant frequency (SRF) of the capacitors is higher than the maximum charge pump switching frequency.

At maximum power, the PE25203 could reach a junction temperature of up to 125 °C at 85 °C ambient. This can heat the surroundings of the die and potentially the flying capacitors. The choice of the temperature rating of the capacitors is dependent on the temperature gradient across the board and the placement of the capacitors with respect to the die.

V_X Capacitor

The V_X capacitor is connected between the VX pin and the board level power ground. pSemi recommends setting the V_X capacitor rating to exceed the V_X over-voltage protection (V_{XOVP}) value that the on-chip device protection circuits activate before damage is caused to the V_X capacitor. This increases system robustness to fault situations. The V_X capacitor function is to reduce the voltage ripple at VX, but it can cause higher charge redistribution loss as well and reduction of efficiency. The value of the V_X capacitor must be optimized around those criteria.

The recommended effective capacitance used for V_X capacitors should have a typical value of 2.5 µF for nominal voltages.

L_X Inductor

The L_X inductor connects VX to VOUT (and the load). V_{OUT} is a filtered version of V_X. L_X is used to reduce the charge distribution loss when switching between the two complementary switching phases used by the PE25203. The higher the inductance value, the lower the charge distribution loss, but also the higher the voltage ripple on V_X. An optimum value of L_X should be chosen to minimize the charge distribution loss while supporting acceptable voltage ripple at VX and VOUT. The recommended inductance value is 100 nH.

The L_X inductor must support the full load output current. For robust system design, pSemi recommends that the L_X inductor be capable of supporting the I_{LOAD} output current limit (I_{LIM}) of 5.5A. This allows the on-chip protection circuits to activate before causing inductor damage in the event of a fault situation. The path from VX to VOUT through the Lx inductor must be achieved with minimum parasitic resistance because losses in the inductor or in the system-level routing could have a direct impact on the system efficiency.

Output Capacitor

The output capacitor reduces the ripple applied to the load at VOUT. The higher the capacitor value, the lower the ripple at VOUT. Increasing the output capacitor value increases the soft-start duration and could cause the chip to timeout during soft start. It is essential that the soft-start current charge the chosen output capacitor value within the soft-start time out duration.

The recommended effective capacitance used for C_{OUT} capacitors must have a typical value of 40 µF for nominal voltages.

V_{DD} Capacitor

The recommended effective capacitance used for the V_{DD} capacitor must have a typical value of 0.5 µF for 3.6V, which is the typical voltage of V_{DD}.

Input Capacitor

The input capacitor is connected between VIN and GND. It is used to reduce the ripple on VIN as the PE25203 switches. To reduce any parasitic inductance effects, place the input capacitor as close to the chip as possible. The voltage rating of the capacitor must be as high as the absolute maximum voltage rating for the system and the effect of the capacitor voltage coefficient must be considered to determine the effective capacitance value at the applied V_{IN}.

The recommended effective capacitance used for C_{IN} capacitors must have a typical value of 7 µF or higher for nominal voltages.

Note: The recommended effective capacitance values from this section are for the components used in Table 9. For the optimized value selection based on your application, contact pSemi.

Layout Example

Figure 41–Figure 44 show a Type-III PCB layout example using a 4-layer board. The trace width and spacing is 0.1 mm/0.1 mm. The size of the vias is a 0.2 mm hole and a 0.1 mm pad.

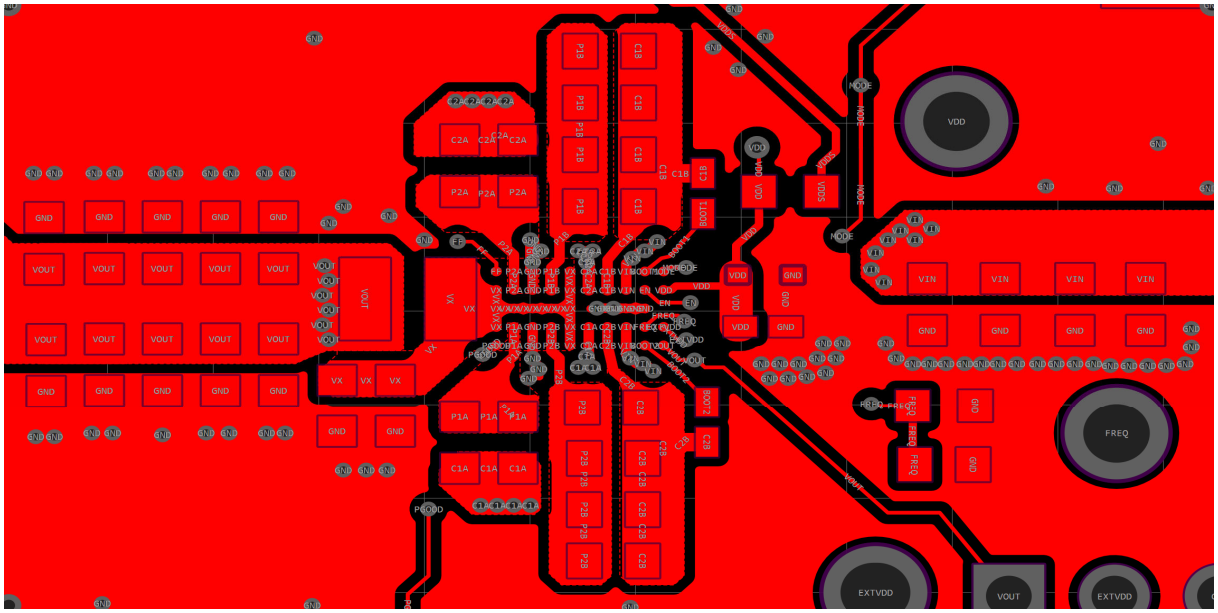


Figure 41. Top Layer

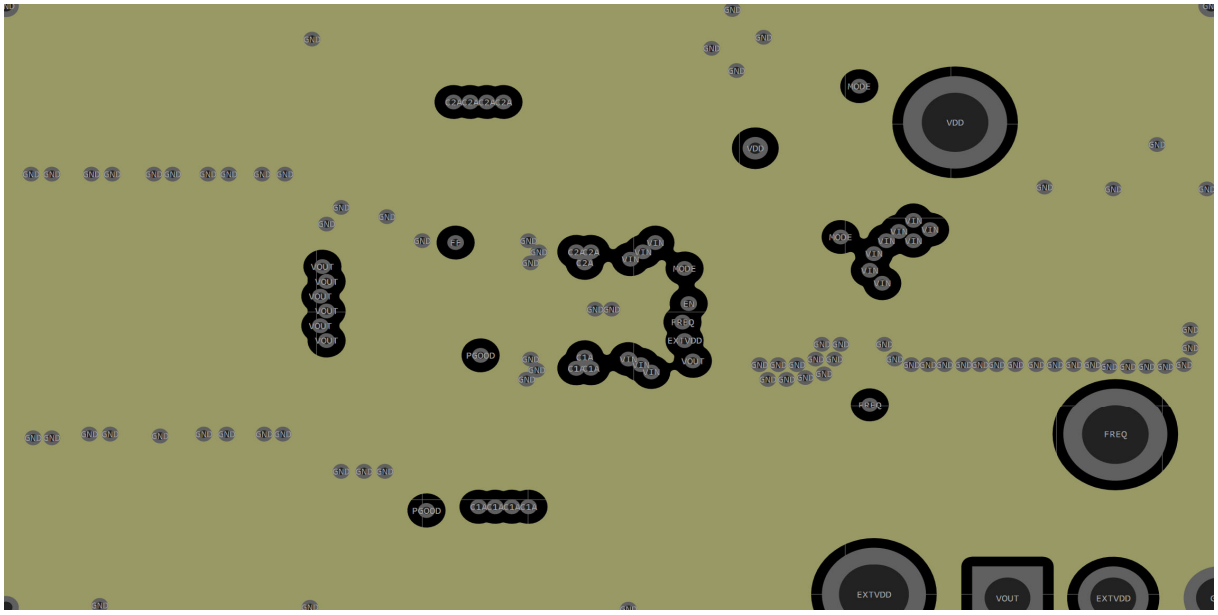


Figure 42. Inner Copper Layer 1

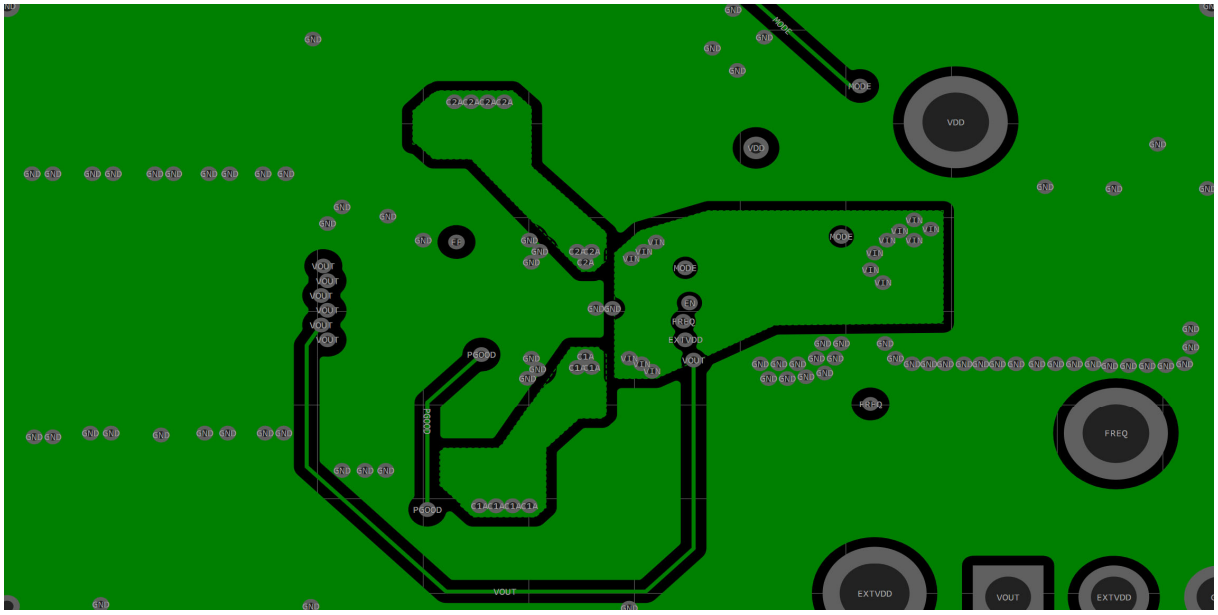


Figure 43. Inner Copper Layer 2

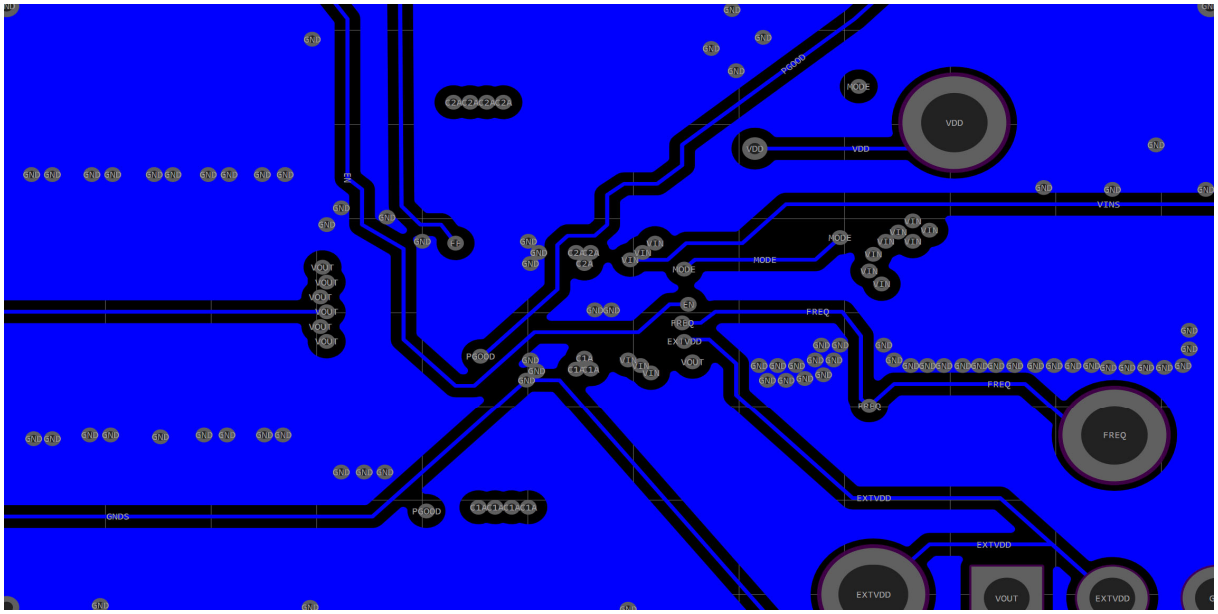


Figure 44. Bottom Copper Layer

Packaging Information

This section provides packaging data, including the following:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The moisture sensitivity level (MSL) rating for the PE25203 in the 2.715 mm × 4.545 mm WLCSP is MSL 1.

Package Drawing

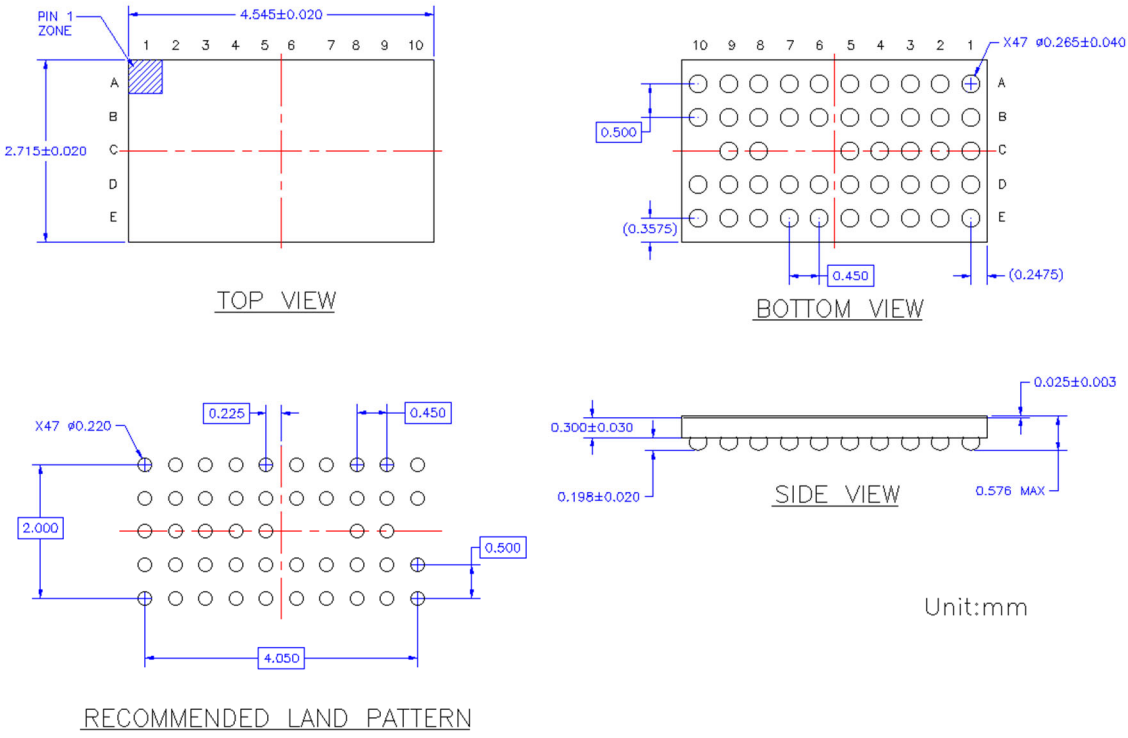


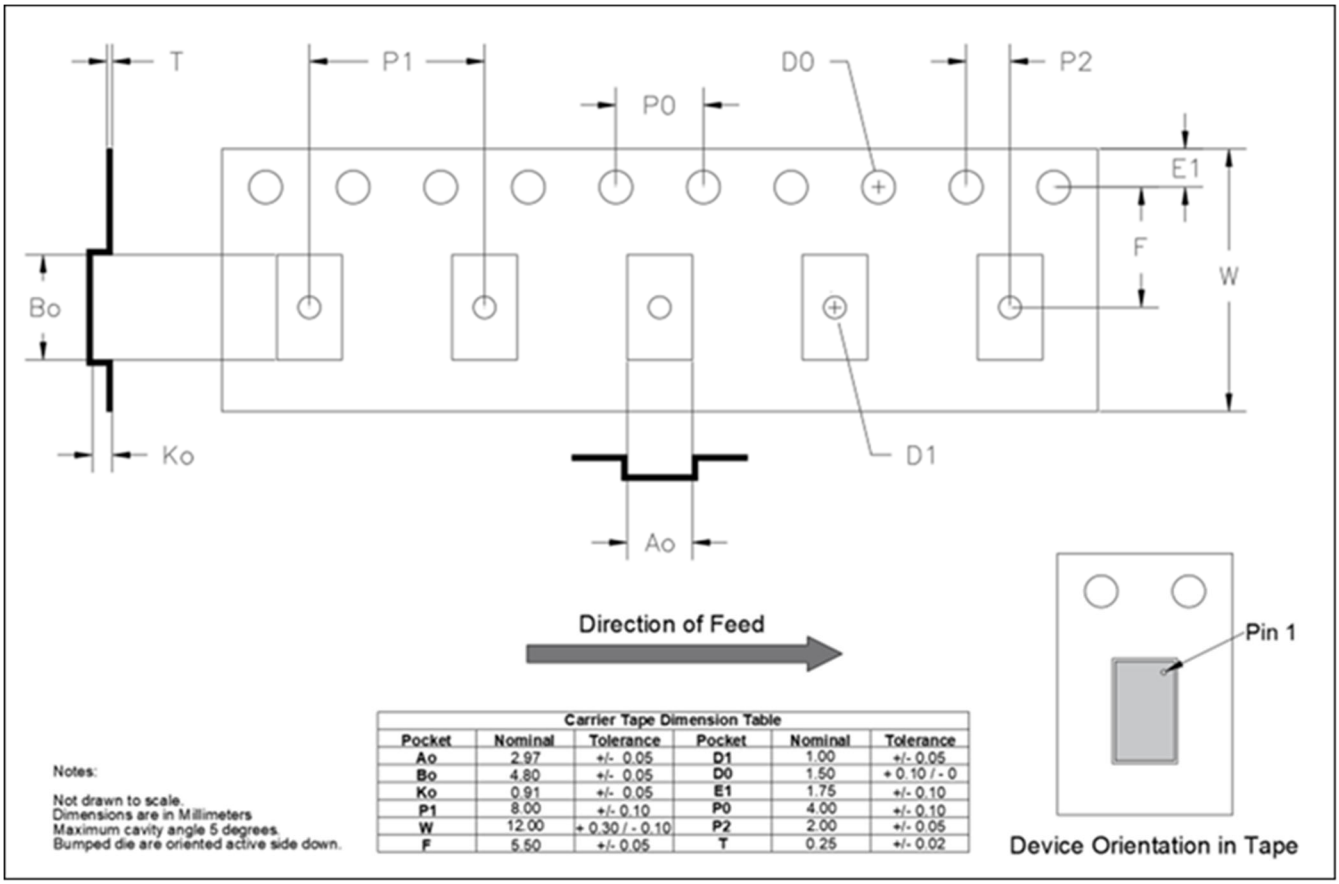
Figure 45. PE25203 Package Outline Drawing

Top Marking Specification

● = Pin 1 indicator
PPPPP = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
YY = Last two digits of assembly year (2022 = 22)
WW = Assembly Work Week (01,02,03,...,52)

Figure 46. PE25203 Package Marking Specifications

Tape and Reel Specification



Carrier Tape Dimension Table

Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	2.97	+/- 0.05	D1	1.00	+/- 0.05
Bo	4.80	+/- 0.05	D0	1.50	+ 0.10 / - 0
Ko	0.91	+/- 0.05	E1	1.75	+/- 0.10
P1	8.00	+/- 0.10	P0	4.00	+/- 0.10
W	12.00	+ 0.30 / - 0.10	P2	2.00	+/- 0.05
F	5.50	+/- 0.05	T	0.25	+/- 0.02

Notes:

Not drawn to scale.
Dimensions are in Millimeters
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Figure 47. Tape and Reel Specifications for 6.850 x4.450 x 0.492 mm WLCSP

Ordering Information

Table 10 lists the PE25203 order codes and shipping methods.

Table 10. Order Codes and Shipping Methods

Order Code	Description	Packaging	Shipping Method
PE25203A-V	4A Charge Pump Divide by 2 or 3	WLCSP on Tape and Reel	250 Units/T&R
PE25203A-R	4A Charge Pump Divide by 2 or 3	WLCSP on Tape and Reel	5000 Units/T&R
EK25203-01	PE25203 DC-DC Converter Evaluation Board	Populated PCB	1 Unit

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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