PE25204

Document Category: Product Specification

48V$_{IN}$, Divide-by-4, 6A Charge Pump, Capacitor Divider

General Description

The PE25204 is an ultra-high efficiency charge pump solution that divides down an input voltage by 4 and delivers up to 72W output at up to 96.8% peak efficiency. The PE25204 can also be used in parallel to increase output power. The PE25204 supports an input voltage range of 18V to 60V in divide-by-4 operation. It is available in a WLCSP package measuring 3.6 x 5.8 mm.

Features

Proprietary architecture enables industry-leading efficiency in an ultra-compact solution footprint and profile—96.8% peak efficiency and up to 72W per part.

- Parts can be operated in parallel for higher output power.
- Input voltage range of 18V to 60V supports 48V bus systems and 24V industrial supplies.
- Fixed divide-by-4 from input voltage to output voltage.
- Fully protected with input under-voltage, output short circuit detection, and thermal shutdown fault detection.

Applications

- Ultrabooks/notebook computers
- Data centers/servers
- Networking equipment
- Base stations
- Optical equipment
- Industrial applications

Efficiency

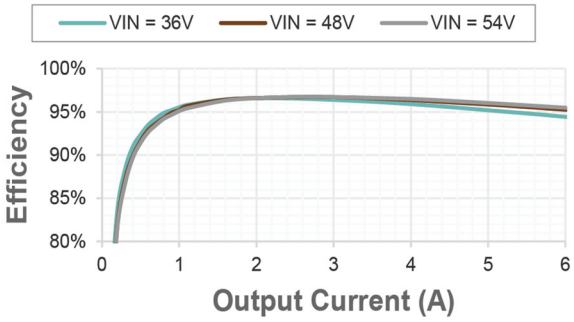


Figure 1. PE25204 Typical Efficiency 36, 48, 54V, T_A= 25 °C

Application

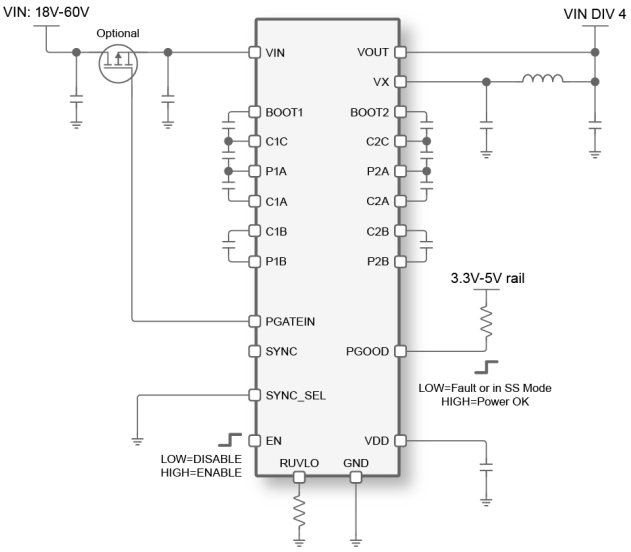


Figure 2. PE25204 Typical Application Circuit

Table of Contents

Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between operating range maximum and absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified below.

Table 1. PE25204 Absolute Maximum Ratings [1]

Parameter	Condition	Min	Max	Unit
RUVLO, SYNC, SYNC_SEL, PGOOD to AGND	–	-0.3	6	V
VIN	EN to AGND	-0.3	62	V
VOUT to PGND	VOUT to PGND	-0.3	18	V
EN to AGND	–	-0.9	V_{IN}+0.6	V
PGATE to AGND	–	-0.3	V_{IN}+0.6	V
VX,P1A,P1B,P2A,P2B to PGND	–	-0.3	18	V
VX to P1A,P1B,P2A,P2B	–	-0.3	18	V
C1A, C2A to PGND	–	-0.3	33	V
C1B, C2B to PGND	–	-0.3	49	V
C1C. C2C to PGND	–	-0.3	62	V
C1B to C2A	–	-0.3	33	V
C2B to C1A	–	-0.3	33	V
C1C to C2B	–	-0.3	33	V
C2C to C1B	–	-0.3	33	V
CBOOT1 to C1C, CBOOT2 to C2C	–	-0.3	6	V
VOUT to VX	–	-35	+35	V
VIN to C1C, C2C	–	-0.3	62	V
CBOOT1, CBOOT2 to VIN	–	-0.3	V_{IN}+6	V
VDD, VDDIO to AGND	Excludes VIN, BST1, BST2, BST3, BST4, LX1, LX2, LX3, LX4, C1A, C1B, CBOOT1, P1, C2A, C2B, CBOOT2, P2, VX	-0.3	6	V
AGND to PGND	–	-0.3	+0.3	V
ESD tolerance	HBM [2]	–	750	V
ESD tolerance	CDM [3]	–	500	V

Notes:

1. The above “Absolute Maximum Ratings” are stress ratings only; the notation of these conditions does not imply functional operation of the device at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human body model, per the JEDEC standard JS-001-2012.
3. Field induced charge device model, per the JEDEC standard JESD22-C101.

Recommended Operating Conditions

Table 2 lists the PE25204 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE25204 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{IN} input voltage range, relative to AGND or PGND	18	48	60	V
V_{OUT} output voltage range, relative to AGND or PGND	4.5	12	15	V

Package Thermal Characteristics

Table 3. PE25204 Package Thermal Characteristics [1] [2]

Parameter	Min	Typ	Max	Unit
Storage temperature	-55	–	150	°C
Junction temperature, T_J	-40	–	125	°C
Junction-to-ambient thermal resistance (ΘJA), soldered thermal pad, connected to ground plane	–	25.8	–	°C/W
Junction-to-top thermal characterization (ψJT)	–	0.89	–	°C/W
Junction-to-board thermal characterization (ψJB)	–	3.7	–	°C/W

Notes:

1. The package thermal characteristics and performance are measured and reported in a manner consistent with the JEDEC standards JESD51-8 and JESD51-12.
2. Junction-to-ambient thermal resistance (ΘJA) is a function not only of the IC, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, planes, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.

Electrical Specifications

Table 4 lists the PE25204 key electrical specifications at V_{IN} = 48V, GND = 0V, SYNC_SEL = GND and T_J = -40 to 125 °C, unless otherwise specified. Typical values are at T_A = 25 °C.

Table 4. PE25204 Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max [1]	Units
Input supply and top level						
Input voltage range	V_{IN}	–	18	48	60	V
Input voltage under-voltage lockout (UVLO) threshold	V_{UVLO_VIN}	V_{IN} rising RUVLO = 10 KΩ	–	15	15.5	V
Input voltage under-voltage lockout (UVLO) hysteresis	V_{UVLOH_VIN}	–	–	0.19	–	V
Shutdown supply current	I_{VIN_OFF}	EN = 0	–	70	–	nA
Output leakage	I_{VOUT_OFF}	EN = 0, max applied V_{OUT} = 18V	–	2	–	nA
Operating supply current	I_{VIN_NOSW}	No switching	–	0.3	–	mA
Thermal shutdown threshold [2]	T_{TSD_IN}	–	–	150	–	°C
Exit from thermal shutdown falling [2]	T_{TSD_OUT}	–	125	–	—	–
Thermal shutdown hysteresis [2]	T_{TSDH}	–	–	16	–	°C
PGATE pull-down current	I_{PGATE_PD}	Enable external P-type disconnect	42	–	60	µA
PGATE pull-up resistance	R_{PGATE_PD}	Disable external P-type disconnect	2	–	–	kΩ
PGATE pull-down voltage	V_{PGATE_PD}	–	9.5	–	–	V
DC-DC converter						
Output power delivered [2]	P_{OUT}	V_{IN} = 48V	72	–	–	W
Output current delivered [2]		SYNC_SEL=GND	6	–	–	A
Peak efficiency		–	–	96.8	–	%
Nominal output voltage	V_{OUT}	I_{OUT} = 0A	–	V_{IN}/4	–	V
Nominal clock frequency		Divided by 2 internally for charge pump frequency	–	545	–	kHz
Input SYNC frequency	f_{SYNC}	TA = +25 °C, I_{LOAD} = 6A [3]	300	–	600	kHz
Soft start timeout duration		–	–	100	–	ms
Soft start input current limit	I_{SS_IIM}	–	–	134	–	mA
Output over current fault	I_{OUT_SC}	–	8	–	12	A
Programmable input voltage under-voltage lockout (UVLO) range, V_{IN} rising.	V_{UVLO_PROG}	RUV = 10 kΩ, Accuracy: ±6%	–	–	15.7	V
		RUV = 38.3 kΩ, Accuracy: ±6%	–	–	59.6	
Programmable input voltage under-voltage lockout (UVLO) threshold conversion, V_{IN} rising	M_{UVLO_PROG}	–	1.46	1.51	1.55	V/KΩ

Programmable input voltage under-voltage lockout (UVLO) range, hysteresis	$V_{UVLO\_PROG\_H}$	V_{IN} rising – V_{IN} falling	–	0.9		V
Logic pins						
PGOOD pin leakage	I_{LEAK_PGOOD}	V_{PGOOD} = 3V to 5.5V			1	µA
PGOOD output pulldown low level	V_{POL_PGOOD}	I_{PGOOD} = +20 mA			0.25	V
PGOOD input high voltage	V_{IH_PGOOD}	–	1.05			V
PGOOD input low voltage	V_{IL_PGOOD}	–			0.55	V
PGOOD input hysteresis	V_{HYS_PGOOD}	–		0.4		V
PGOOD output initial wait time [2]	t_{WAIT_PGOOD}	Initial wait time from EN logic high to first valid PGOOD output	2.6			ms
EN input high voltage	V_{IH_EN}	T_A = -40 to 125 °C	2.6			V
EN input low voltage	V_{IL_EN}	T_A = -40 to 125 °C			0.60	V
EN input current	I_{EN}	V_{EN} = 48V, T_A = -40 to 125 °C		42		µA
EN input minimum off time	$T_{ENL\_OFF\_MIN}$	Minimum logic low duration for shutdown	70			µs
SYNC_SEL input resistance	$R_{SYNCSEL}$	T_A = -40 to 125 °C		108		k
SYNC_SEL input low voltage	$V_{IL\_SYNCSEL}$	T_A = -40 to 125 °C			0.4	V
SYNC_SEL input high voltage	$V_{IH\_SYNCSEL}$	T_A = -40 to 125 °C	1.10			V
SYNC input high voltage	V_{IN_SYNC}	SYNC_SEL pin open, T_A = -40 to 125 °C	1.1			V
SYNC input low voltage	V_{IL_SYNC}	SYNC_SEL pin open, T_A = -40 to 125 °C			0.5	V
SYNC input minimum on time	$t_{SYNCI\_ON\_MIN}$	SYNC_SEL pin open; minimum logic high duration to guarantee detection	220			ns
SYNC input minimum off time	$t_{SYNCI\_OFF\_MIN}$	SYNC_SEL pin open; minimum logic low duration to guarantee detection	300			ns
SYNC output pull-up voltage	V_{PUO_SYNC}	V_{SYNC_SEL} = 0V, I_{SYNC} = -20 mA	1			V
SYNC output pull-down voltage	V_{PDO_SYNC}	V_{SYNC_SEL} = 0V, I_{SYNC} = +20 mA			0.25	V
SYNC output pull-up impedance	R_{PUO_SYNC}	V_{SYNC_SEL} = 0V, I_{SYNC} = -20 mA		128	145	Ω
SYNC output pull-down resistance	R_{PDO_SYNC}	V_{SYNC_SEL} = 0V, I_{SYNC} = +20 mA		10	15	Ω

Notes:

1. Min/max specifications are 100% production-tested at T_A = 25°C, unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Guaranteed by design.
3. External component changes are necessary if operating outside default switching frequency.

Pin Configuration

This section provides the PE25204 pin configuration information. Figure 3 shows the pin map of this device in a WLCSP package. Table 5 lists the pin functions.

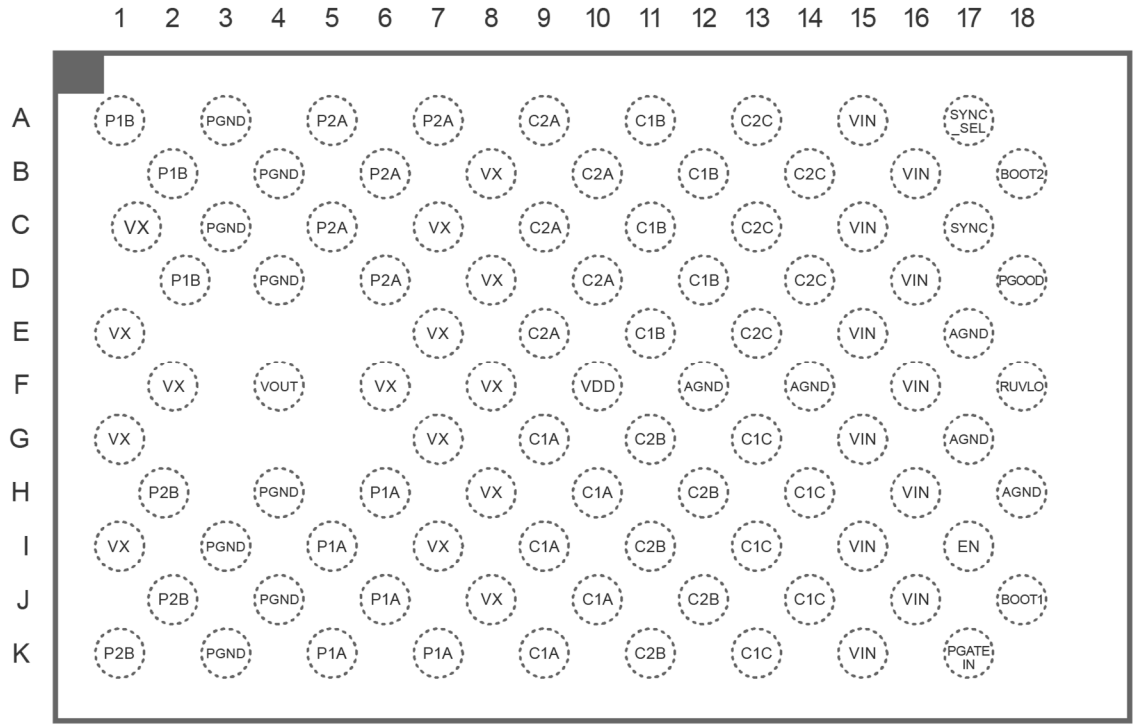


Figure 3. Pin Configuration (Top View)

Pin Descriptions

Table 5. PE25204 Pin Descriptions

Pin No.	Pin Name	Description
A1,B2,D2	P1B	Flying capacitor C1B phase node. Connect a fly capacitor between the C1B and P1B pins.
A3,B4,C3,D4,H4.J4,I3,K3,	PGND	Power ground. High current path.
A5,A7,B6,C5,D6	P2A	Flying capacitor C2A and C2C phase nodes. Connect fly capacitors between the C2A,P2A and theC2C,P2A pins
A9,B10,C9,D10,E9	C2A	Flying capacitor C2A terminal. Connect a fly capacitor between the C2A and P2A pins.
A11,B12,C11,D12,E11	C1B	Flying capacitor C1B terminal. Connect a fly capacitor between the C1B and P1B pins.
A13,B14,C13,D14,E13	C2C	Flying capacitor C2C terminal. Connect a fly capacitor between the C2C and P2A pins.
A15,B16,C15,D16,E15,F16, G15,H16,I15,J16,K15	V_{IN}	Input voltage from 18V to 60V.
A17	SYNC_SEL	When SYNC_SEL is open, an external clock input must be applied at the SYNC pin. When SYNC_SEL is connected to GROUND, an internal clock is fed to the SYNC pin as an output.
B8,C7,D8,E7,F8,G7,H8,I7, J8,F6,F2,C1,E1,G1,I1	VX	Charge pump output switching node. Connect to an external inductor.
B18	BOOT2	Bootstrap capacitor pin. Connect a 4.7-nF bootstrap capacitor between BOOT2 and C2C.
C17	SYNC	SYNC clock input or master-slave clock output for paralleled parts. The SYNC pin direction is set according to the SYNC_SEL pin.
D18	PGOOD	Active-high Power Good indicator. Connect a resistor from PGOOD to an external bus voltage between 3.3V and 5V. When used in a parallel configuration with other PE25204 devices, connect each PGOOD pin together. If PGOOD is left open, it pulls up to the internal VDD voltage of 1.2V. It is recommended if using PGOOD that an external pull-up is fitted.
E17,F12,F14,G17,H18	AGND	Analog ground
F4	V_{OUT}	Sense connection for the V_{OUT} connect to the output after Vx Inductor.
F10	VDD	Connect to a decoupling capacitor of 220 nF. This pin is connected to the internal power supply on the chip at 1.2V.
F18	RUVLO	Connect a 1% resistor between this pin and GROUND to program the operational V_{IN} under-voltage lockout. A resistor value between 10 kΩ and 38.3 kΩ programs the operational V_{IN} under-voltage lock-out between 15.7V and 59.6V in a linear manner. This resistor should be bypassed with a 1 nF capacitor to ground.
G9,H10,I9,J10,K9	C1A	Flying capacitor C1A terminal. Connect a fly capacitor between the C1A and P1A pins.
G11,H12,I11,J12,K11	C2B	Flying capacitor C2B terminal. Connect a fly capacitor between the C2B and P2B pins.
G13,H14,I13,J14,K13	C1C	Flying capacitor C1C terminal. Connect a fly capacitor between the C1C and P1A pins.
H2,J2,K1	P2B	Flying capacitor C2B phase node. Connect a fly capacitor between the C2B and P2B pins.
H6,I5,J6,K5,K7	P1A	Flying capacitor C1A and C1C phase nodes. Connect fly capacitors between the C1A,P1A and the C1C,P1A pins
I17	EN	IC enable pin. Logic high enables the device, logic low disables the device.

J18	BOOT1	Bootstrap capacitor pin. Connect a 4.7-nF bootstrap capacitor between BOOT1 and C1C.
K17	PGATE IN	V_{IN} -referenced gate-drive for an optional external P-type disconnect transistor between the V_{IN} pin and an input supply voltage. When used in a parallel configuration with other parts, connect each PGATE pin together. Otherwise, leave PGATE open.

Functional Block Diagram

Figure 4 shows the PE25204 functional block diagram.

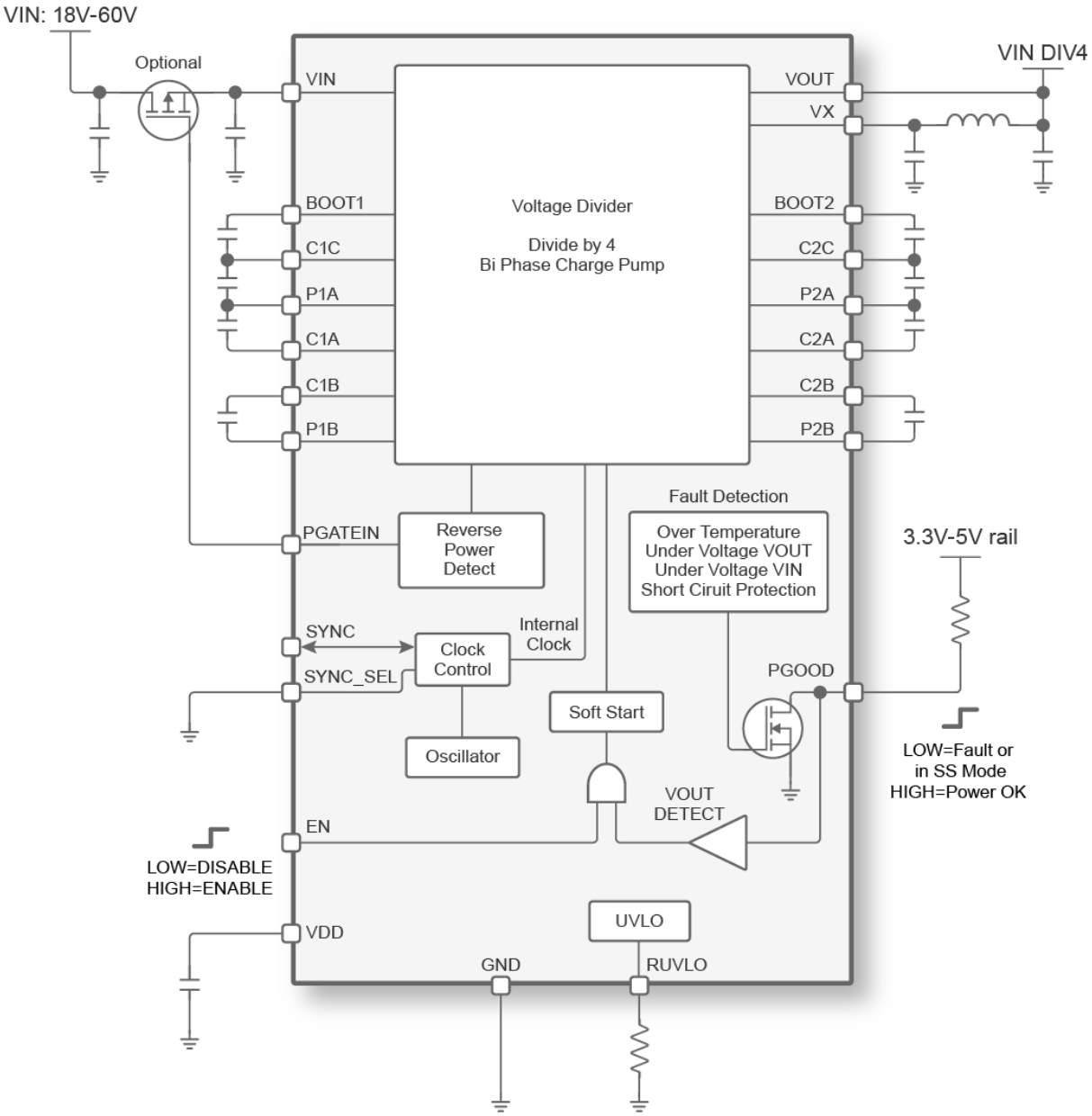


Figure 4. PE25204 Functional Block Diagram

Application Circuit

Figure 5 shows a typical application circuit. For more details about component values, see Applications Information on Page 25.

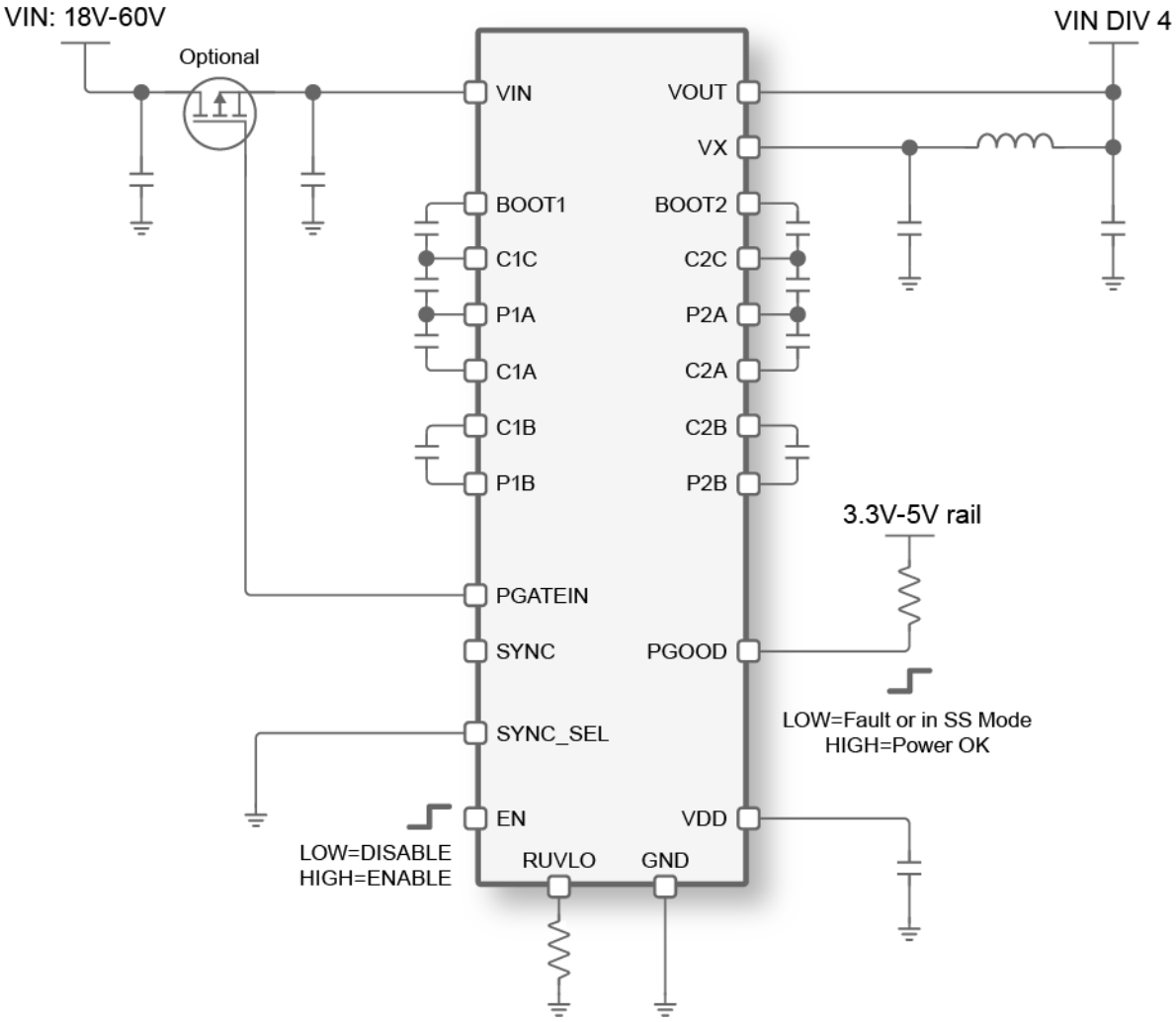


Figure 5. Simplified Application Circuit

Typical Performance Data

Figure 6–Figure 15 show the PE25204 typical performance data at ambient temperature = 25 °C with no airflow in all cases, unless otherwise specified.

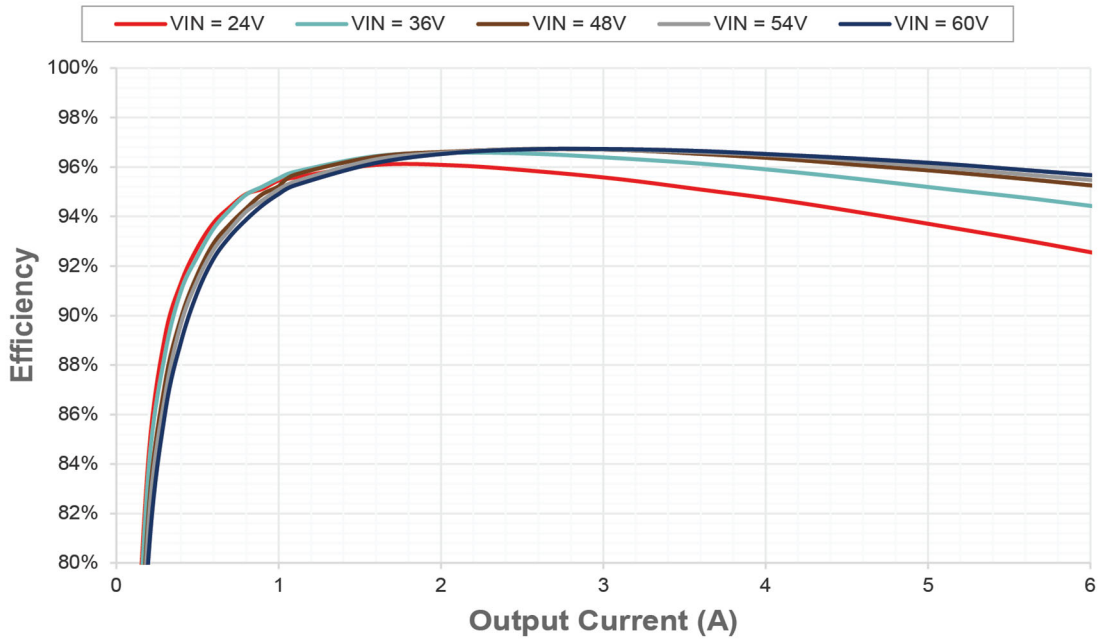


Figure 6. Efficiency vs. load current, V_{IN} = 24, 36, 48, 54, 60V, T_A = 25 °C

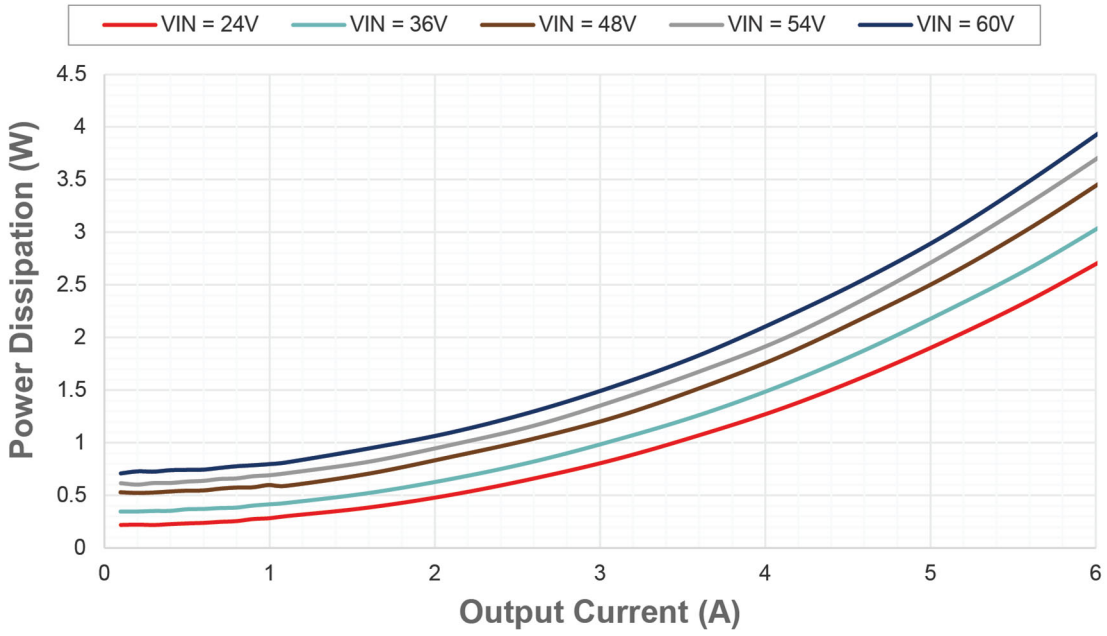


Figure 7. Power dissipation vs. load current, V_{IN} = 24, 36, 48, 54, 60V, T_A = 25 °C

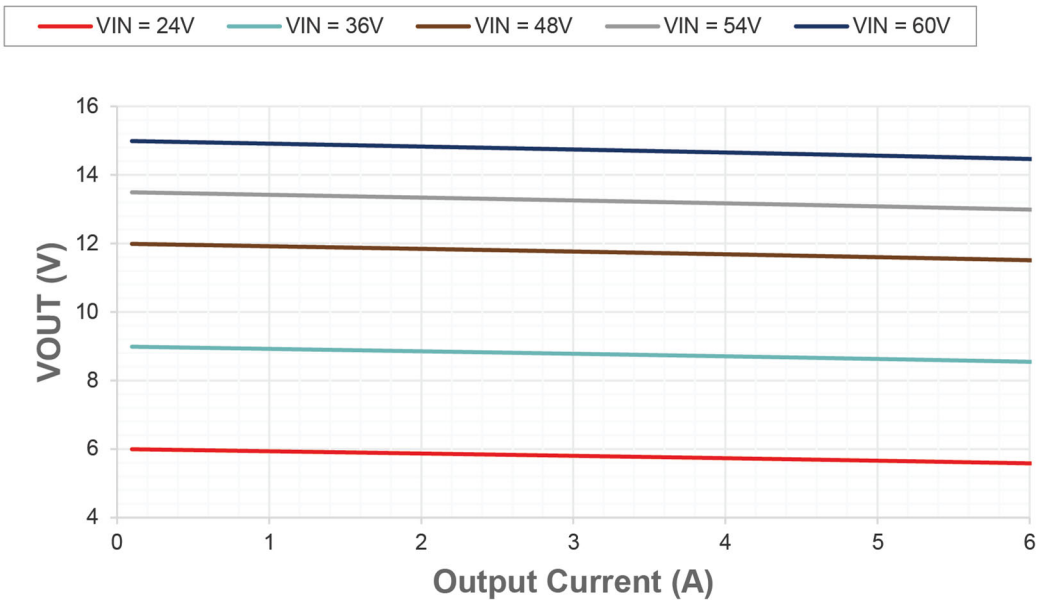


Figure 8. V_{OUT} vs. load current, V_{IN} = 24, 36, 48, 54, 60V, T_A = 25 °C

Figure 9. Power-up scope plot, no load, V_{IN}=48V, C_{LOAD} = 44 µF

Figure 10. Shutdown behavior with V_{OUT} loaded, V_{IN}=48V, C_{LOAD} = 44 µF

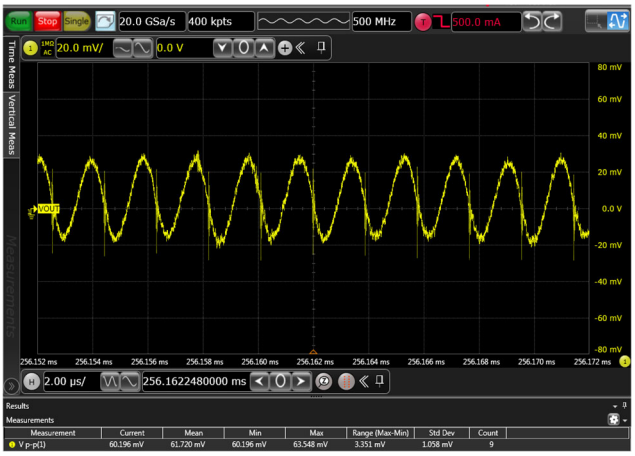


Figure 11. Output ripple, V_{IN} = 48V, I_{LOAD} = 6A

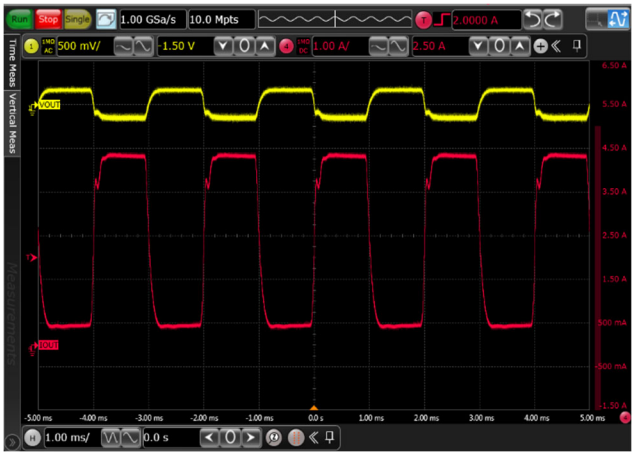


Figure 12. Transient response, V_{IN} = 48V, 0.5A–4.5A, 30A/ms, C_{LOAD} = 44 µF

Figure 13. Startup behavior with V_{OUT} loaded with 100Ω, within the soft-start timeout, V_{IN}=48V

Figure 14. Startup into a short circuit, V_{IN} = 48V. The device latches off after a short circuit until EN is cycled.

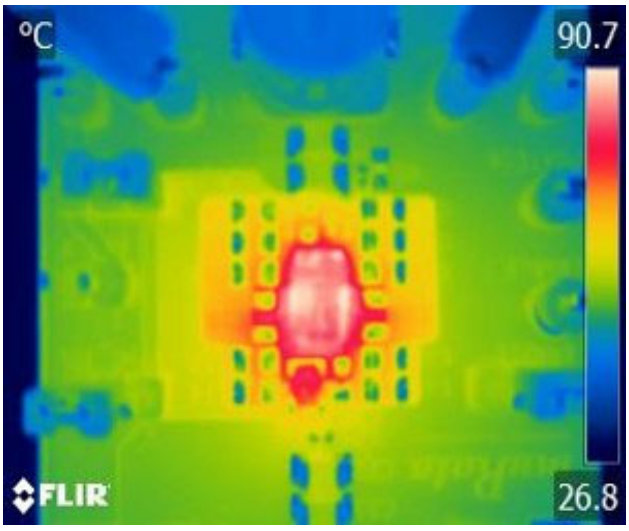


Figure 15. Thermal plot, V_{IN} = 48V and V_{OUT} = 11.49V, P_{DISS} = 3.29W, top case temperature = 90.7 °C at T_A = 25 °C

Detailed Description

The PE25204 is a divide-by-4, two-phase, charge pump-based DC-DC converter. The PE25204 is designed to operate in a fixed divide-by-4 mode, so any change in input voltage is reflected at the output.

The PE25204 can be powered from input voltage ranges from 18V to 60V. The under-voltage lockout is set using a resistor to ground from RUVLO.

The output voltage range supported is from 4.5V to 15V with load currents up to 6A.

The SYNC_SEL pin can be tied to ground or left floating. If tied to ground, the device uses an internal clock and this clock signal appears at the SYNC pin, which is the usual mode of operation for single device use. If left floating, the SYNC pin acts as an input, and this is used when multiple devices are used in parallel.

The pin configurations are sampled when the PE25204 starts up and before the charge pump stage is enabled. The configuration pins are not designed to be driven dynamically, so they must be in a fixed state at power up.

Enable (EN)

The PE25204 is enabled by an active-high EN input pin when a voltage greater than 2.6V is applied. The PE25204 is disabled when the voltage at the EN pin falls below 0.6V. The EN pin can be shorted to the V_{IN} pin to automatically enable the part with a minimal number of external components and PCB routing.

When using multiple PE25204s in parallel, connect all their EN pins to a single enable signal. Figure 9 and Figure 10 are scope plots that show the enable and disable behaviors.

Startup – EN, VIN Relationship

The PE25204 has an enable input pin, EN, which is designed to be compatible with typical low-voltage digital I/O levels so that it can be easily driven by an external controller. EN can also be connected to the VIN pin.

If external power sequencing or control is not required, tie EN to VIN so that it is not left open.

If the EN pin is held high until VIN has reached its nominal voltage (set by RUVLO), the PE25204 follows the initialization sequence in Figure 16.

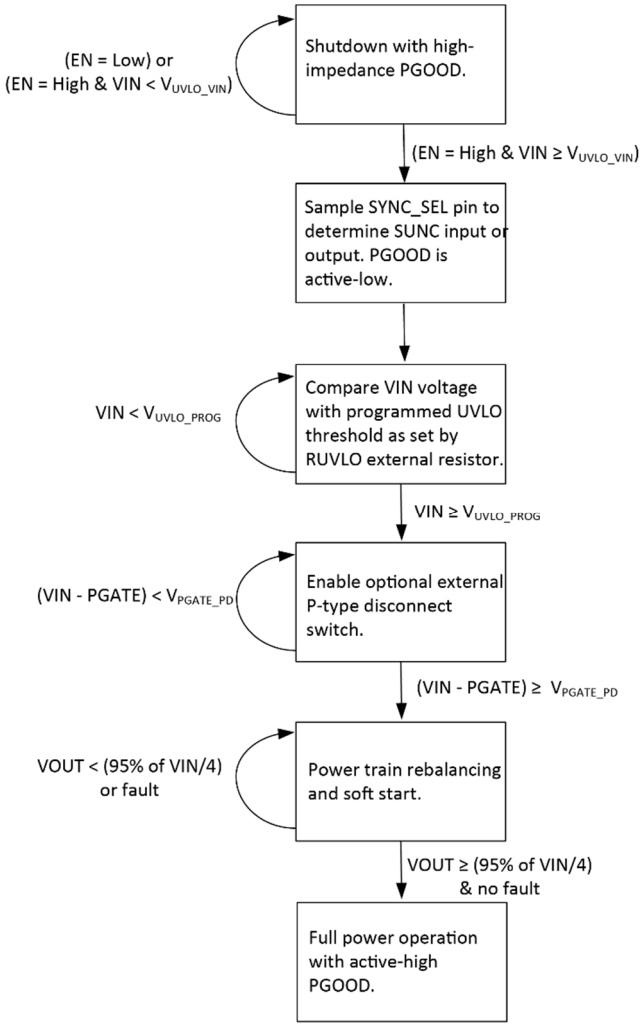


Figure 16. Initialization Sequence

Input Under-voltage Lockout (UVLO)

The PE25204 provides continuous monitoring of the V_{IN} input using a fixed under-voltage lockout threshold and an operational under-voltage lockout threshold. The PE25204 is enabled when the V_{IN} voltage rises above 15.2V typical, but both charge pump switching and the PGATE gate-drive to an external P-type disconnect switch remain disabled until the V_{IN} voltage exceeds the operational under-voltage lockout threshold. The operational under-voltage lockout threshold is externally programmable by an under-voltage resistor (R_{UV}) connected between the RUVLO pin and GROUND. An R_{UV} resistor value between 10 kΩ and 38.3 kΩ programs the operational V_{IN} under-voltage lock-out threshold in a linear manner. Do not short the RUVLO pin to GROUND. If the minimum operating voltage required is 18V, set R_{UV} = 10 kΩ.

When the V_{IN} voltage falls below the operational under-voltage lockout threshold plus additional 1.5V hysteresis, charge pump switching is disabled and the PGATE voltage pulls up to the V_{IN} voltage to disable the external P-type disconnect switch. The remaining circuitry within PE25204 remains enabled until the PE25204 is disabled by a logic low at the EN pin or by the V_{IN} voltage falling further below the fixed under-voltage lockout threshold plus 0.2V hysteresis.

Setting the Under-voltage Lockout

The under-voltage lockout of the device is set by resistor R_{UV}. Set the UVLO voltage to 18V–60V using this formula:

$$UVLO\ (V) = R_{UV}\ (k\Omega) * 1.51$$

The pSemi recommended resistors are 1% or better from the E96 series. Use the closest resistor to the value needed between 10 KΩ and 38.3 KΩ. pSemi also recommends bypassing this resistor with a 1-nF capacitor to ground. Figure 17 shows the relationship between UVLO and R_{UV}.

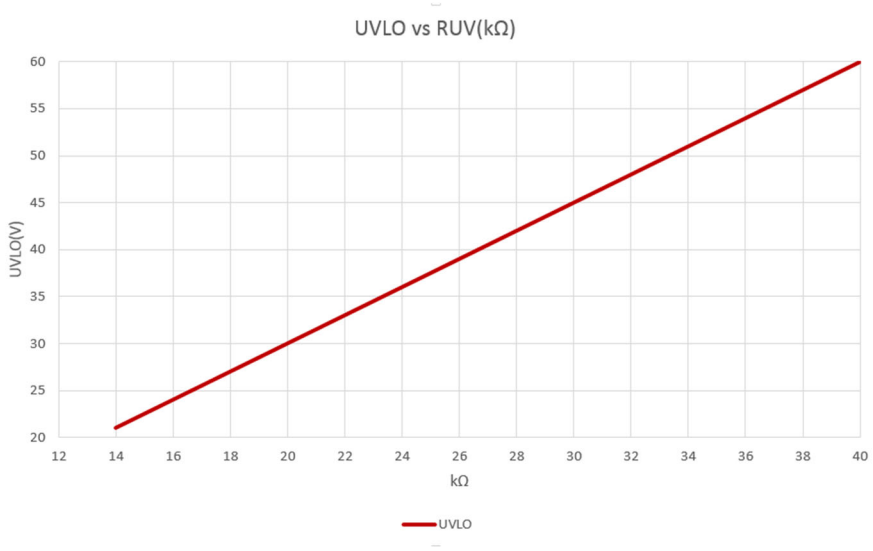


Figure 17. Relationship between UVLO and R_{UV}

(Optional) Input Disconnect (PGATE)

The PE25204 supports the addition of an optional input disconnect switch between the system input supply and the VIN pin to prevent reverse power flow through the part during operation. pSemi recommends a P-type FET with its source terminal connected to the VIN pin, its drain terminal connected to the system input supply, and its gate terminal connected to the PGATE pin. The PE25204 pulls PGATE up to VIN to disable the disconnect switch. To enable the disconnect switch, PGATE falls to at least 5V below VIN.

Power Good (PGOOD)

Power good (PGOOD) is an open-drain output that releases high after the output reaches above 95% of the voltage $V_{IN}/4$. After PGOOD asserts, the PE25204 stops soft-start and enables full power operation. The PE25204 monitors the PGOOD pin directly allowing an external capacitor to add filtering. When using multiple PE25204s in parallel, connect all their PGOOD pins together. In this case, all PE25204s must complete soft start before PGOOD is asserted and full power operation is allowed. In the event of a fault at one or more parallel PE25204s, the PGOOD pin is pulled low by the faulted PE25204(s).

Output Under-Voltage Protection (UVP)

The PE25204 protects against low output voltage such as that caused by an output short by de-asserting the PGOOD pin and latching the part off. The UVP fault is triggered when the output voltage falls below 80% of $V_{IN}/4$.

Latched Fault Reset

If the device enters a latched fault condition—which can occur by exceeding the soft-start timeout of 100 ms or by triggering a short circuit detect—the device must be reset by either:

- Pulling the EN pin trigger low for longer than 150 µs, or
- Switching the input supply off and on to re-trigger the UVLO condition.

Pre-charging and the Soft Start

The PE25204 is a high-power device. To protect the system and the internal circuitry of the PE25204, power is supplied to the output and the flying capacitors in a controlled soft-start sequence.

The soft-start current supplied to the load must be sufficient to ramp V_{OUT} to $V_{IN}/4$ V in less than the soft-start timeout duration. The soft-start current level is configured as 134 mA, and the soft-start timeout is 100 msec. During both the soft-start and pre-charge phases, do not load VOUT until the PGOOD pin goes high.

Pre-charge Operation

Before enabling the soft start switching sequence, the PE25204 pre-charges the internal flying capacitors to a balanced state based on the divider ratio. This ensures that when the soft-start phase commences, the voltage across the capacitors is at their nominal voltage and known state. The adaptive pre-charge system can take up to 5 msec of pre-charging time depending on the external voltages present on the circuit.

Soft-start Operation

After the pre-charge phase is completed, the device enters soft-start mode and charges the output capacitor at 134 mA typical value. It exits the state when the V_{OUT} voltage has reached within 95% of the target voltage, which is $V_{IN}/4$. The PGOOD pin is allowed to go high at the same time.

As the device goes through a soft-start sequence, do not apply full load currents to the device until the PGOOD pin is high. If a full load is connected before this, the device does not start up. Figure 18 shows the full start-up sequence. After enable goes high, the pre-charge phase begins as shown in the first slope of Figure 18. The second slope is the device operating in soft start mode.

Figure 18. Power-up Sequence

If the output capacitor is loaded, V_{OUT} might not reach the target during the soft-start phase. As a result, the system detects soft-start timeout, latches off the device, and then requires the EN pin to be toggled to restart. A similar situation can also happen if the charge pump has too much COUT capacitance.

PGOOD Operation

The power good pin is a bidirectional open drain pin. When the output voltage is above 95% of $V_{IN}/4$, the PGOOD pull-down FET is turned off to allow the external pull-up resistor to pull up the node. The PGOOD pin must be pulled up externally >1.05V from a digital I/O for correct operation. If another device or digital I/O is also pulling down on this pin, the PE25204 remains in soft-start mode and does not enter high-power mode.

During soft start, the power that the PE25204 can supply to a load is limited to roughly 134 mA. Keep the load current well below the soft-start current level to ensure that V_{OUT} can ramp to $V_{IN}/4$ less than 100 msec.

When the PE25204 allows PGOOD to be pulled high, the charge pump is ready to support the full load current.

The PGOOD pin of a disabled device is NOT pulled low if the device is not enabled. In effect, if EN=0, the PGOOD pin can be ignored.

In the event of an over-current detection over 15A, the PGOOD pin is pulled low, and the device is latched off until EN is toggled.

External/Internal Clock Modes and the SYNC_SEL Pin

In most applications, the PE25204 charge pump operates using an internal precision oscillator. Table 6 shows the SYNC pin table.

Table 6. SYNC Pin Table

SYNC_SEL Pin	SYNC	MODE
GND	Output	The internal clock is sent to the SYNC pin as an output.
Open circuit	Input	Apply an external clock to the SYNC input.

The charge pump is operated at half frequency of the SYNC pin input/output clock. Because the PE25204 internal components are optimized for efficiency with the internal oscillator frequency, injecting an external clock is not recommended for single-unit applications. If configured to use an external clock (SYNC_SEL=open circuit), and the external clock stops or is not present for some reason, an internal watchdog detects the missing clock and causes the PE25204 to swap back to use of the internal clock source. When the expected external clock source resumes, the PE25204 reverts to using the external clock.

If operating at low external synchronization frequencies, the flying capacitor values and the inductor values may need to be optimized for maximum efficiency. Please contact Applications for help with optimization.

If an external clock-in/out function is not being used in the application, it is recommended that the SYNCSEL pin is tied to GND. In this mode, the internal clock is present on the SYNC pin.

Internal Protections

The PE25204 is a high-power device. To protect the system and the internal circuitry of the PE25204, multiple fault detection circuits are built in. Table 7 lists the various protection modes.

Table 7. Protection Modes

Detector	Latched Off or Automatic Retry	Response Time	Effect of Fault
Over-temperature	Automatic retry	µs	PGOOD goes low and the power stage switches off until the temperature reduces below the hysteresis threshold. At this point, the device automatically restarts. To automatically restart, the device must restart into no load.
V_{IN} under-voltage	Automatic retry	µs	PGOOD goes low, and the charge pump is disabled until V_{IN} returns above the UVLO threshold and is enabled To automatically restart, the device must restart into no load.
ILOAD over-current	Automatic retry	µs	If the current exceeds the 8–12A over-current limit, PGOOD goes low, and the charge pump is disabled for a period of 1023 clock cycles to cool down. If the device is still over current after the cooldown period it automatically restarts.
ILOAD short circuit	Latched off	µs	If the load current exceeds 15A, the device is immediately latched off and shuts down. To restart the device, EN must be toggled.
Soft-start timeout	Latched off	µs	If V_{OUT} does not reach the target voltage of $V_{IN}/4$ within the soft start timeout period of 100 ms, the device shuts down and EN must be toggled to restart it.
PGOOD held low	Automatic retry	µs	If the charge pump is operating at full power and if PGOOD is pulled down externally, the device enters soft-start mode. If the PGOOD pin is held low for less than the soft-start period, the charge pump returns to full power operation. If the PGOOD pin is held low for longer than the soft-start duration, the charge pump completes a soft-start cycle before returning to normal operation and must not be loaded during this period.

VX over-voltage	Automatic retry	µs	If VX goes over-voltage the device enters a cooldown period for 1023 clock cycles before restarting the charge pump.
VOUT under-voltage	Automatic retry	µs	If the output of the device is under the V_{OUT} threshold, the PGOOD pin is pulled low. The device switches off and enters a cooldown period of 1023 clock cycles. After the cool down period the charge pump restarts into soft start mode.

V_{IN} Under-voltage and Thermal Shutdown Faults

The V_{IN} under-voltage and thermal shutdown faults are grouped together because the effect they have on the charge pump is similar. If either of these faults is present when the charge pump is first enabled, the charge pump starts to power up but holds before any power—even soft-start current—is applied to the load.

The charge pump holds in this state until both faults are clear, no matter how long this takes.

V_{IN} under-voltage and thermal shutdown faults are considered *persistent* because they hold the charge pump disabled until the fault clears.

In the case of V_{IN} under-voltage, it is unlikely that the charge pump can support the full load current when V_{IN}—and therefore V_{OUT}—is too low. Because it is not ideal for the PE25204 or the load to operate in this condition, the charge pump waits for V_{IN} to improve or recover.

An over-temperature fault is likely to occur only when the PE25204 is dissipating too much internal power, which normally results from another fault condition, such as an overload condition. In the event of over-temperature, the PE25204 could start to deviate from guaranteed performance specifications, which would not be ideal for the system. To recover from over-temperature, the power dissipation in the device must be reduced to allow the external heat sinking to reduce the internal die temperature.

When V_{IN} under-voltage or an over-temperature fault are detected during normal operation, the PE25204 enters a controlled shutdown sequence with an unlimited cooldown period (the minimum cooldown time is 5 ms). When the faults clear, the PE25204 enters a soft-start sequence.

Over-current Protection

Over-current protection operates by sensing the current draw from V_{IN}. The over-current protection trips when the PE25204 operates outside the recommended operating conditions. Typically, the device trips when the output current exceeds between 8A and 10A. Over-current protection has two separate protection methods:

- If the current exceeds the over-current protection threshold of 8-12A, then when triggered the device enters a cooldown period for 1023 cycles and automatically restarts. During this time the PGOOD pin is pulled low.
- If the current exceeds 15A, the device immediately shuts down and latches off. During this time, the PGOOD pin is pulled low. To restart the device, the EN pin must be toggled.

The PE25204 reacts to over-current faults by entering a controlled shutdown sequence. The device is then latched off until EN is toggled. After enable is toggled and the pre-charge is complete—and after a minimum cooldown time of 5 msec—the PE25204 enters a normal soft-start sequence and attempts to restart. Some persistent fault conditions could prevent the charge pump from restarting successfully, such as in the event of a hard fault to GND at V_{OUT}.

VOUT Under-voltage Protection

The VOUT under-voltage fault detector measures value at V_{OUT} with the expected value derived from $V_{IN}/4$. The V_{OUT} under-voltage fault is designed to be slow and represents an averaged value. The V_{OUT} under-voltage flag trips when V_{OUT} decreases below 80% of the target (V_{UVP}).

The V_{OUT} under-voltage detector trips when V_{OUT} reduces below 80% of the target voltage. It is important to choose external components so that the expected transient loads do not trip the V_{UVP} threshold. In effect, the application must ensure that the load dependency causes a less than 20% deviation from the nominal V_{OUT}.

When V_{OUT} under-voltage occurs, the PE25204 enters a controlled shutdown sequence and latches off until EN is toggled.

Soft-start Timeout

When the PE25204 first tries to supply power to the load, it uses a soft-start circuit so that the power level is limited. Using a soft start has no significant side effects if the start-up is *normal*.

If the PE25204 starts up into a fault, the soft start helps to manage the power being supplied to the fault and limits the PE25204 power dissipation. In normal, fault-free operation, the soft-start timeout is invisible if the soft-start current can ramp V_{OUT} to the target voltage within 100 ms. In the event of a fault, the soft-start timeout occurs when V_{OUT} does not ramp to the target voltage within the expected time. In this case, the soft-start timeout causes power to the load to be stopped and the PE25204 to enter a controlled shutdown sequence. The device then latches off, and EN must be toggled to restart it.

PGOOD Low Detection

In a single PE25204 operation, the PGOOD signal typically has only one driver. When the PE25204 is ready for full power, PGOOD goes high and stays high for as long as the PE25204 remains enabled and fault-free.

In parallel operation, the PGOOD signal must be connected in a wired OR configuration with the other devices. When all devices are ready for full power, the PGOOD signal goes high. In the event of a fault, the PGOOD signal is pulled low and switches off all the parallel devices. EN must then be toggled to restart the devices.

PGATE Reverse Charge Protection

Internal to the IC is a single disconnect switch, Q1, which is a standard FET, so it has a parasitic diode.

This diode stops current flowing from input to output when the FET is turned off, but it does not stop current flowing output to input. This is necessary because a charge pump is inherently bidirectional. The PGATE pin allows for the addition of an external FET, Q2, where the diode is placed in the standard back-to-back configuration for a true switch. This FET mimics the functionality of Q1 to create a true bidirectional on/off switch.

When the internal logic enables the internal switch, a pull-down from V_{IN} is triggered to switch the external FET on.

When the internal FET is turned off, the PGATE pin is pulled high to V_{IN}, thus turning off the Q2 FET.

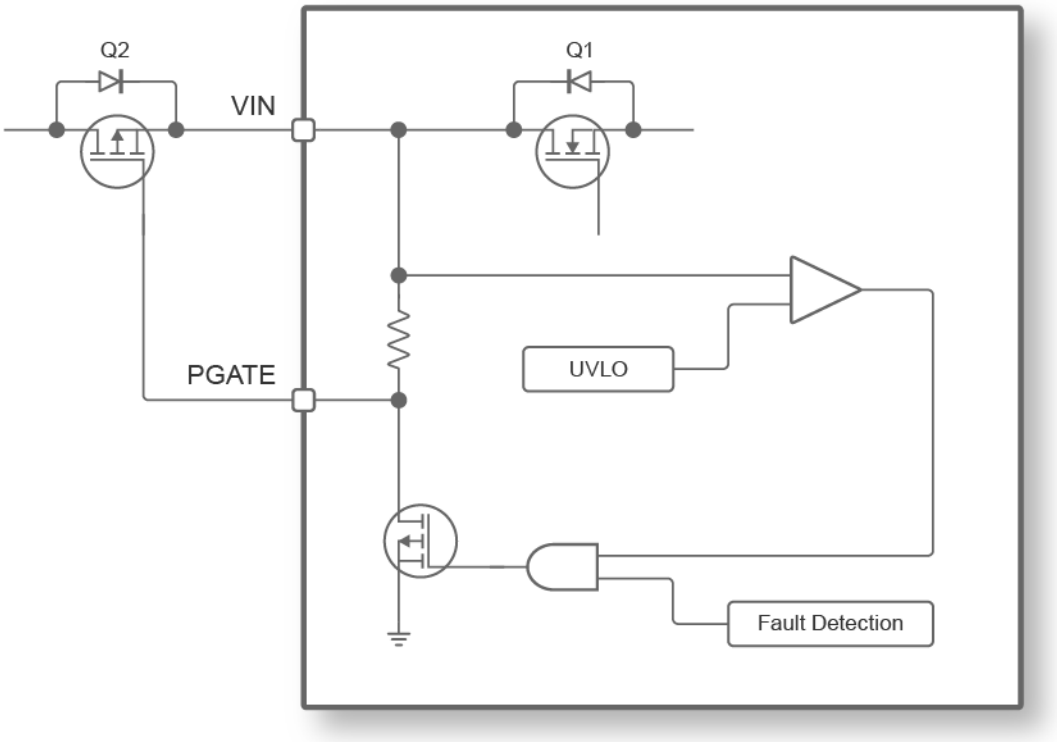


Figure 19. PGATE Operation Functional Diagram

In Figure 20, EN was connected to V_{IN}.

Figure 20. PGATE Power-up Behavior

When the unit is ready to start up, PGATE is pulled low to turn on the external FET Q2.

Applications Information

A charge pump-based DC-DC converter is an open-loop, high-efficiency bus converter that does not have output regulation capability. Because of its architecture, it differs somewhat from conventional inductive buck converters, and some of its behaviors differ from other buck converters. The PE25204 can be configured as an open-loop charge pump to divide the input voltage by 4.

Charge Pump Architecture Basics

A charge pump is a capacitive voltage converter configured by multiple switches and capacitors like those shown in Figure 21.

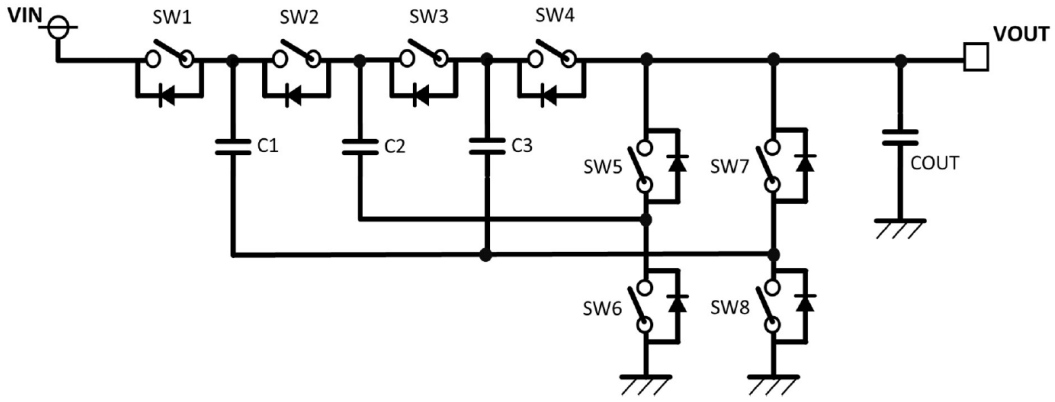


Figure 21. Divide-by-4 Charge Pump Configuration

A charge pump typically has two main switch states, or configurations. The PE25204 also has two main configurations, as shown in Figure 22 and Figure 23. Figure 22 shows the Phase One configuration, and Figure 23 shows the Phase 2 configuration.

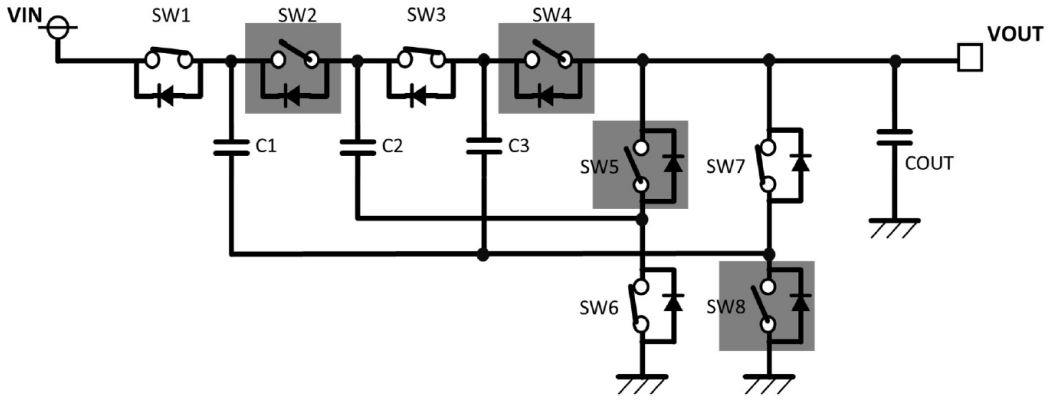


Figure 22. Divide-by-4 Charge Pump Phase One Configuration

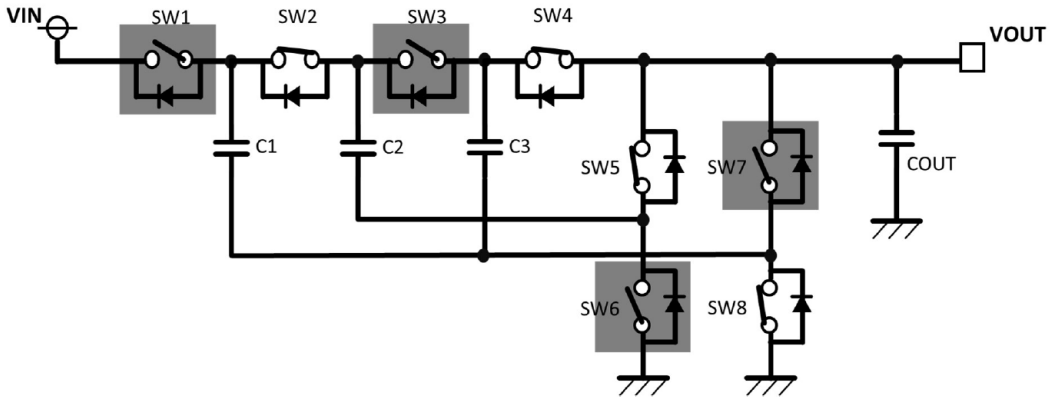


Figure 23. Divide-by-4 Charge Pump Phase Two Configuration

During Phase 1, the flying capacitor of C1 is connected between VIN and VOUT, and C2 and C3 are connected between VOUT and GND. In Phase 2, C1 and C2 are connected between VOUT and GND, and C3 is connected between VOUT and GND

Figure 24 shows these two states of capacitor connection and charged voltage relationship. After the charge pump finishes soft start, each capacitor has VIN/4, VIN*2/4 and VIN*3/4 voltage. This voltage is maintained to keep switching between Phase 1 and Phase 2.

To improve the charge pump efficiency, increase the flying capacitors' capacitances or minimize the switch resistance or parasitic resistance.

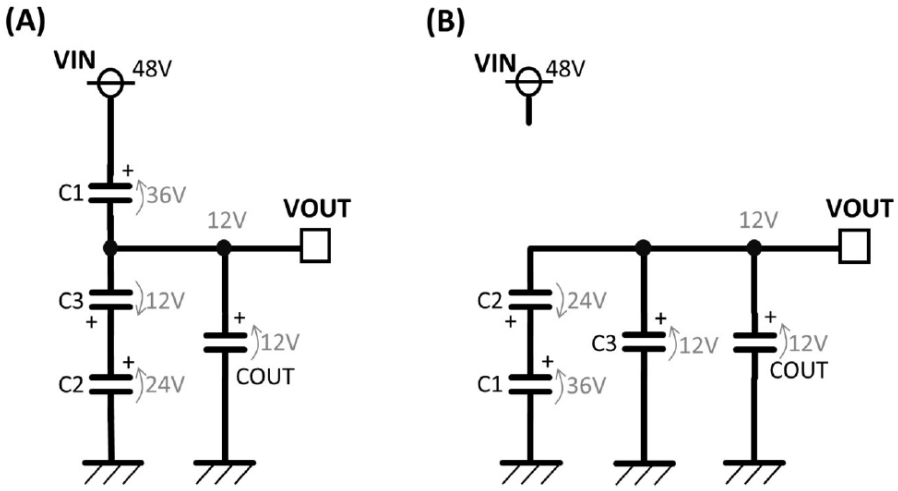


Figure 24. Divide-by-4 Charge Pump Capacitor Connection

Application Schematic

Figure 25 shows a PE25204 typical application circuit. For the recommended circuit part list, see Table 8.

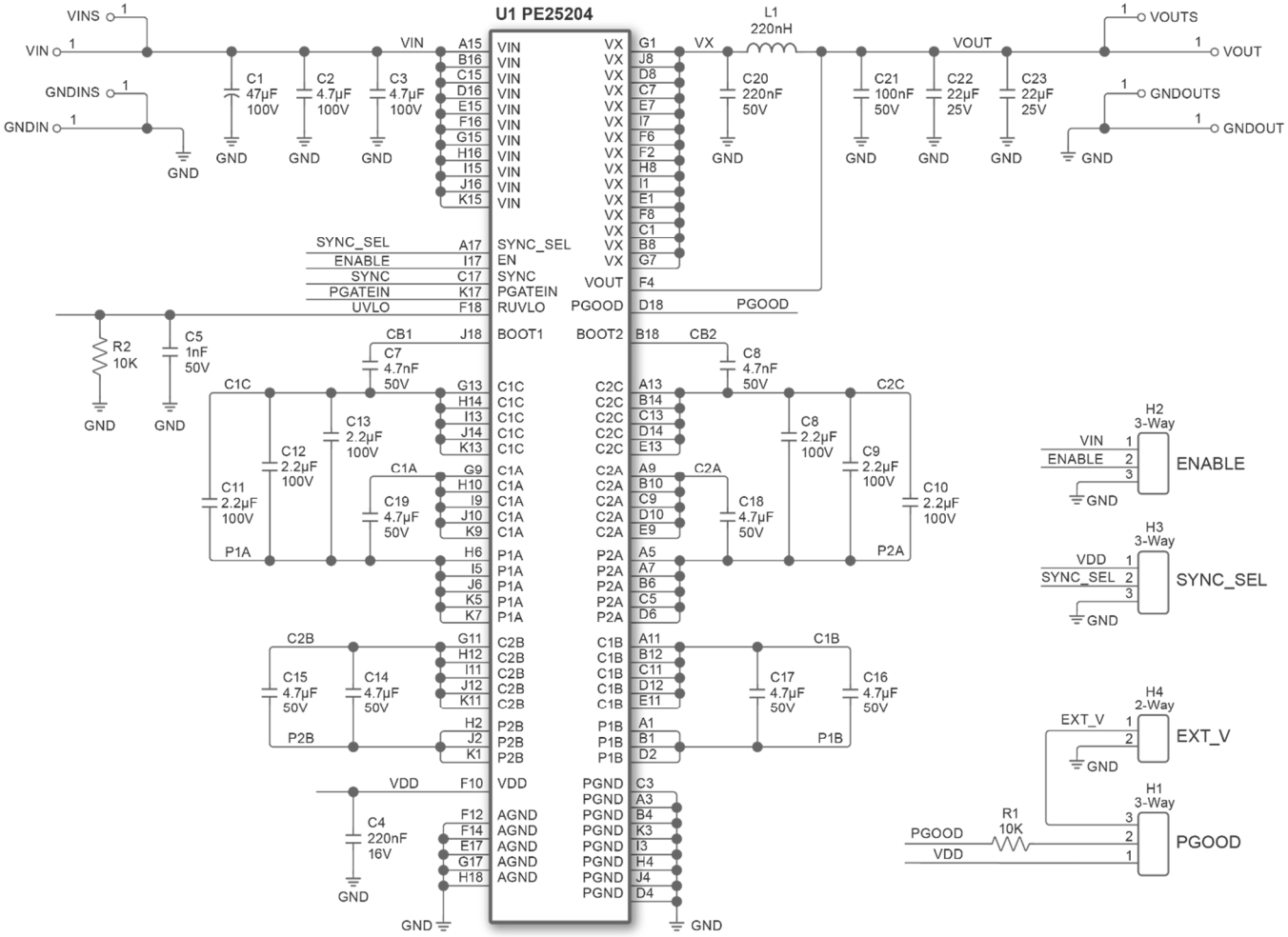


Figure 25. Application Schematic

Application Circuit Part List

Table 8 lists examples of the standard components. The components must be chosen by referring to system requirements such as voltage, temperature, and so on. The information in this table is under evaluation and subject to change.

Table 8. Application Circuit Part List

Reference	Value	Description	Part Number
C1	47 µF	CAP ALUM 47 µF 20% 100V SMD	UUX2A470MNL1GS
C2,C3	4.7 µF	4.7 µF ±20% 100V Ceramic Capacitor X7R 1206 (3216 Metric)	GRM31CZ72A475ME11D
C4	220 nF	0.22 µF ±10% 16V Ceramic Capacitor X7R 0402 (1005 Metric)	GRM155R71C224KA12D
C5	1 nF	CAP CER 1000 PF 50V C0G/NP0 0402	GRM1555C1H102JA01D
C6,C7	4.7 nF	CAP CER 4.7 nF 50V R 0402	GRM155R11H472KA01D
C8,C9,C10, C11,C12,C13	2.2 µF	CAP CER 2.2 µF 100V X7T 0805	GRM21BD72A225KE01D
C14,C15,C16, C17,C18,C19	4.7 µF	CAP CER 4.7 µF 50V X7S 0805	GRM21BC71H475KE11D
C20	220 nF	0.22 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GRM188R71H224KAC4D
C21	100 nF	0.1 µF ±10% 50V Ceramic Capacitor X7R 0402 (1005 Metric)	GRM155R71H104KE14D
C22,C23	22 µF	CAP CER 22 µF 25V X7S 1206	GRM31CC71E226ME15D
L1	220 nH	IND, SMD, fixed inductors 220 nH, 6000 mA, 10 mΩ, 1008 (2520 Metric)	HMLQ25201B-R22MSR-01
		Power Inductor (SMD), Wirewound, 220 nH, 5A, Shielded, 7.2 A, DFE252010F	DFE252010F-R22M=P2
U1	IC	PE25204 IC, PE25204, WLCSP-BGA, pSemi IC	PE25204
R1,R2	10 KΩ	10 KΩ RES, SMD, thick film, 10 KΩ, ±1%, 1/10W, 0603	RC0603FR-0710KL

Application Board Example

Figure 26 shows the PE25204 device evaluation board.

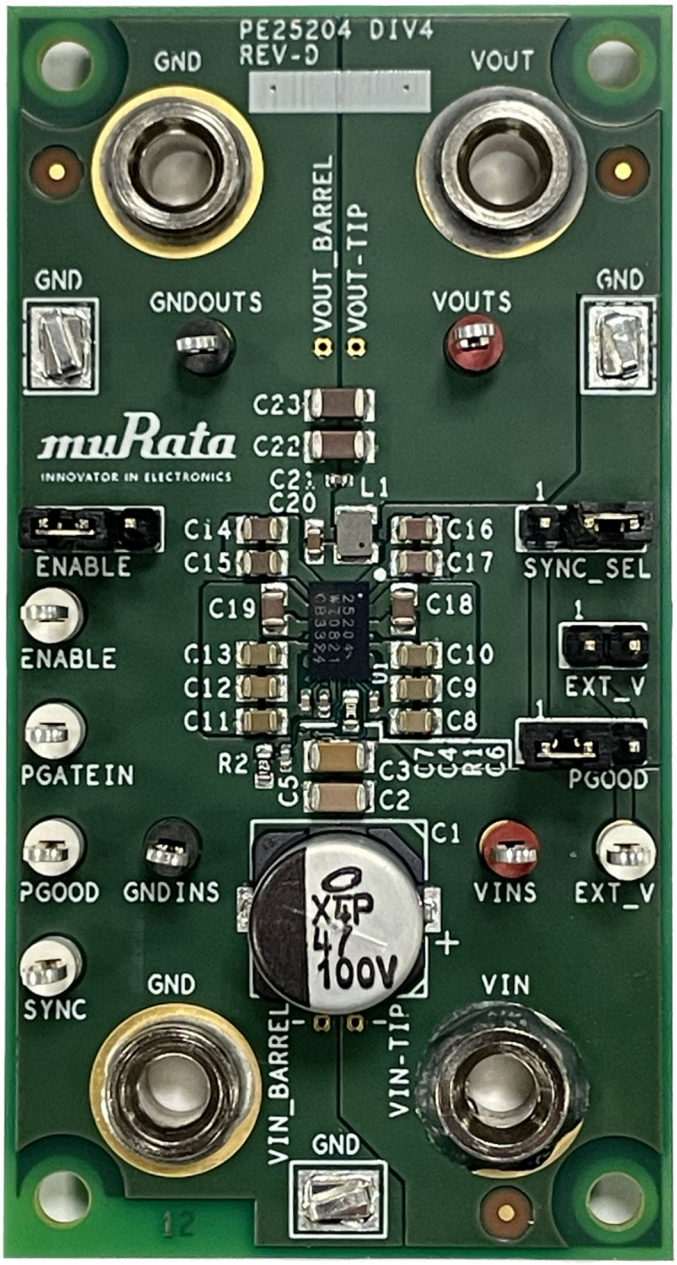


Figure 26. Application Board Example

Component Selection

This section describes the PE25204 required components.

Input Capacitors

The input capacitors connected between VIN and GND reduce the ripple on VIN when the PE25204 switches. Place the input capacitors as close to the chip as possible to reduce any parasitic inductance effects. The voltage rating of the capacitor must be higher than the absolute maximum voltage rating for the system, and the effect of the capacitor voltage coefficient must be considered to determine the effective capacitance value at the applied VIN. Because the charge pump is not a regulator, ripple voltage on VIN can affect the output voltage.

Output Capacitor

The output capacitor reduces the ripple applied to the load at VOUT. The higher the capacitor value, the lower the ripple at VOUT. Increasing the output capacitor value increases the soft-start duration and could cause the chip to time out during soft start. The soft-start timeout value is based on the device's ability to reliably charge the output capacitance within the soft-start period.

VX Capacitor

Place the capacitor before the L1 inductor close to the L1 inductor and the board level power ground.

Inductor Selection

Inductor L1 is 220 nH and must be placed as close as possible to the VX pin and the VX capacitor. The L1 inductor must have rating of at least 6A and a low resistance. All plots in this datasheet were taken using the HMLQ25201B-R22MSR-01 from Cyntec. Efficiency results can differ with other inductors.

Parallel Operation

The PE25204 can run in parallel in a multi-device configuration to increase output power as shown in Figure 31. In parallel operation mode, pay attention to the current and thermal balance.

Current and Thermal Balance

As with standard inductive DC-DC converters, in a parallel design a charge pump must ensure that the current and thermal loading is balanced. The PE25204 provides divided voltage of the input voltage at its output. The output voltage relates the input voltage, and the output voltage is not regulated. Therefore, the charge pump provides natural droop based on the equivalent output resistance (ROUT).

When the load is applied to the paralleled charge pumps, each output voltage of the devices starts to droop. The voltage droop from the ideal output voltage (V_{IN}/DIV) is decided by the following:

(ROUT + parasitic resistance) *ILOAD

For the charge pumps to load-share effectively, pay attention to the layout to reduce the parasitic resistance of the output power tracks.

The PE25204 is capable of over 6A or greater than 72W unless limited by other factors. Therefore, when in parallel operation, imbalance in the load-sharing caused by parasitic impedances can result in one module current limiting before another.

This effect can restrict the total amount of power available to the system. The power loss generated by the device results in heat rise in the module. To maintain load-sharing, the devices must share the same thermal structure.

Recommended Layout

Figure 27 through Figure 30 show the layers of the recommended layout.

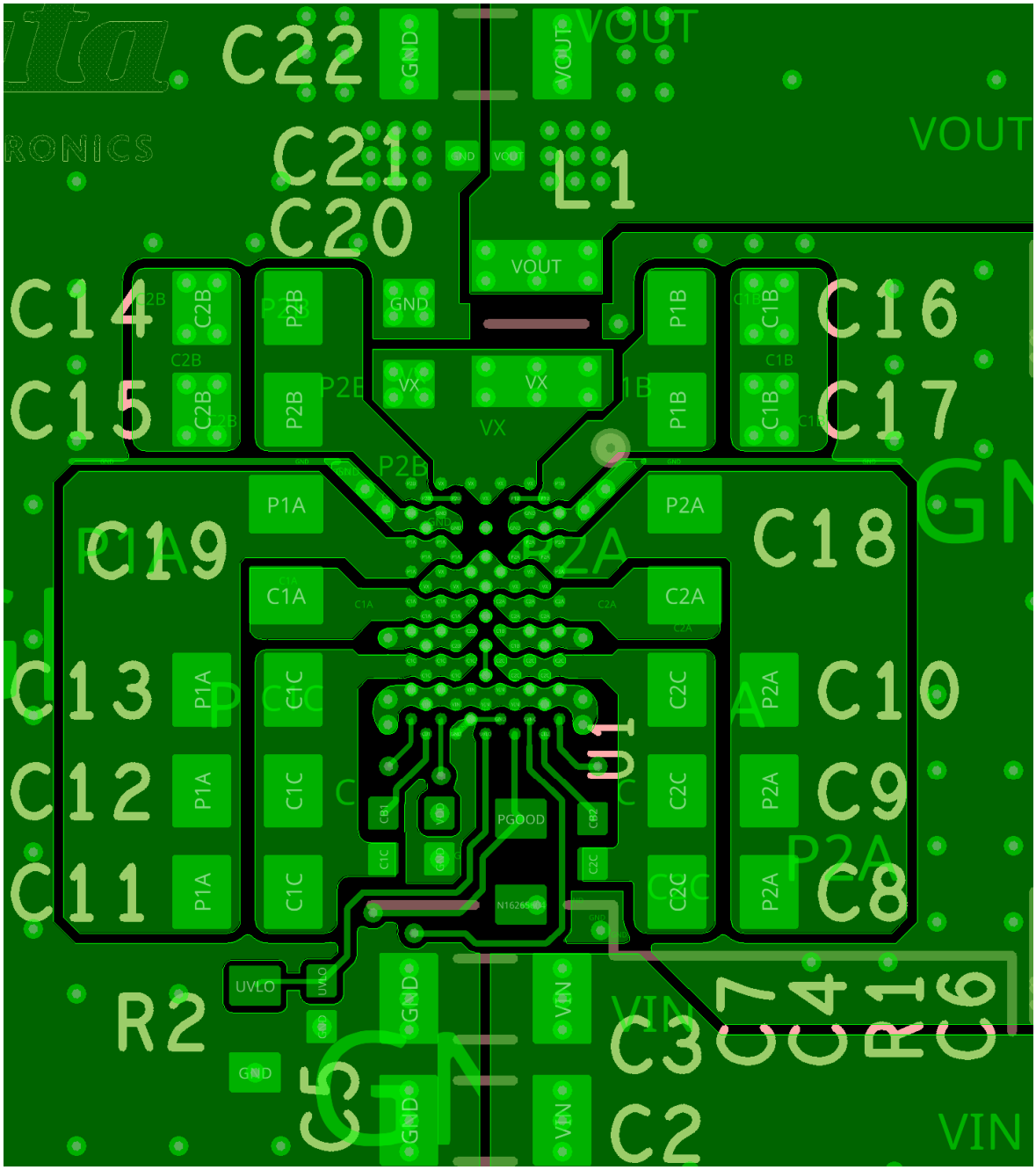


Figure 27. Top Layer

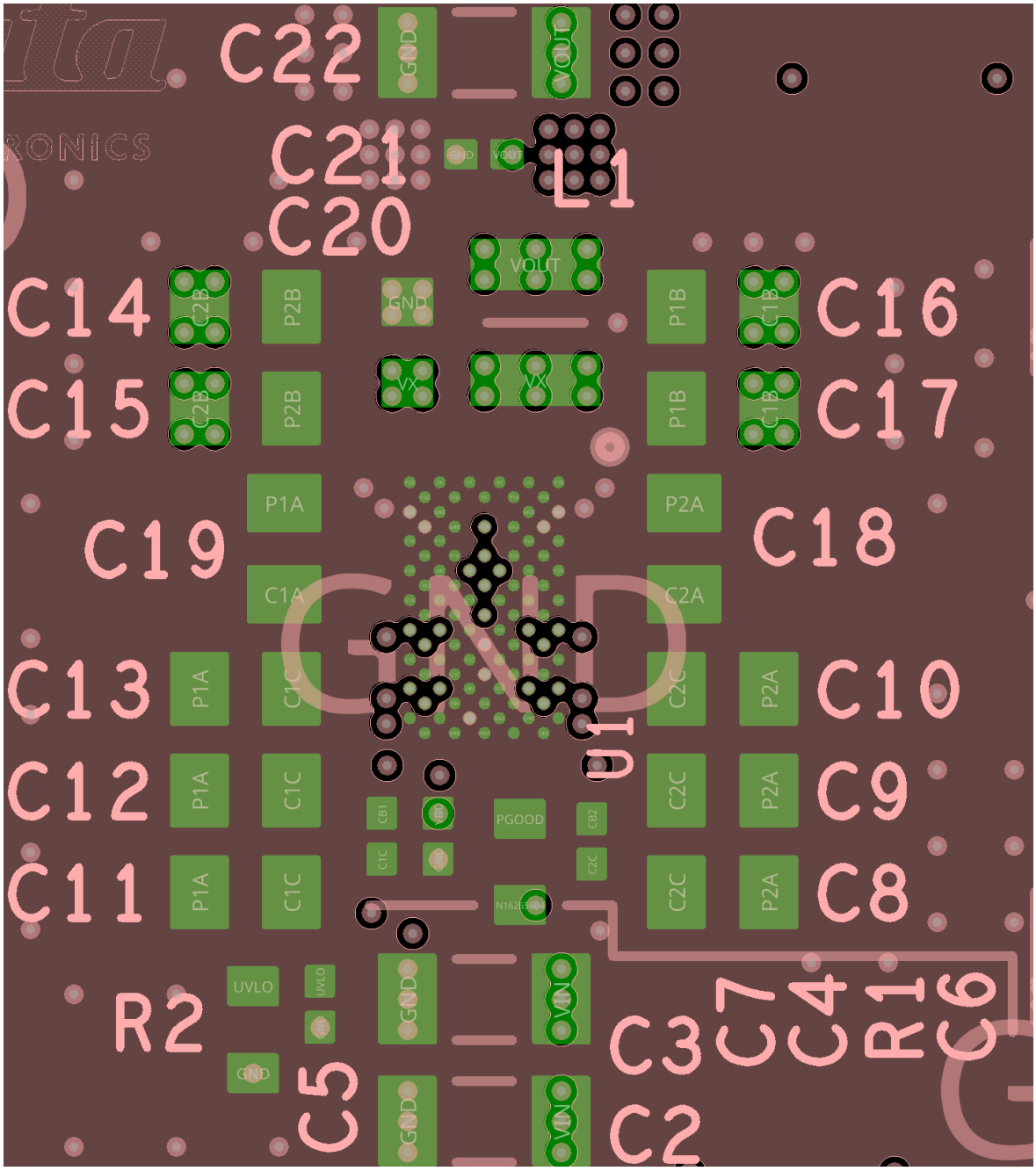


Figure 28. Inner Layer 1

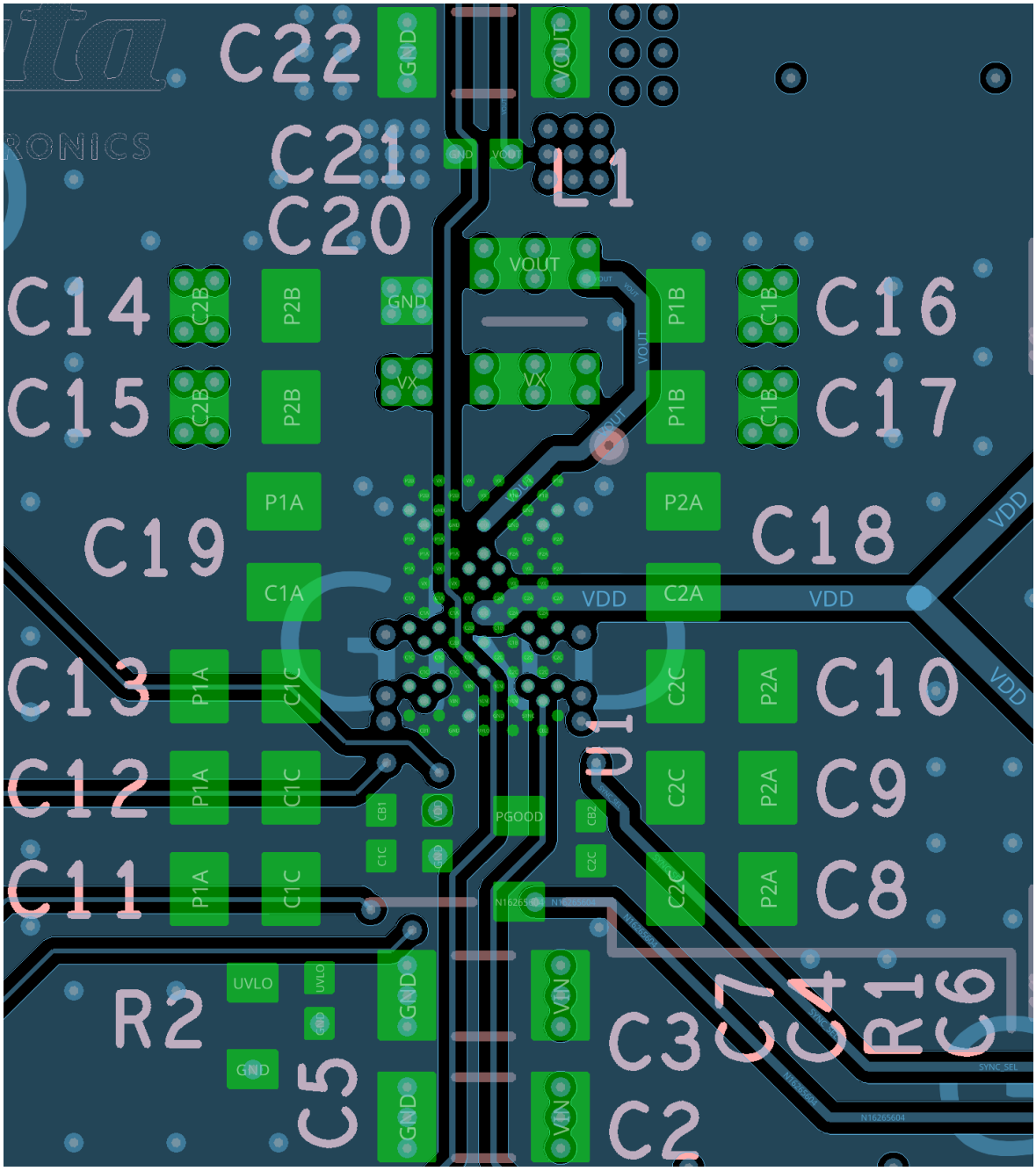


Figure 29. Inner Layer 2

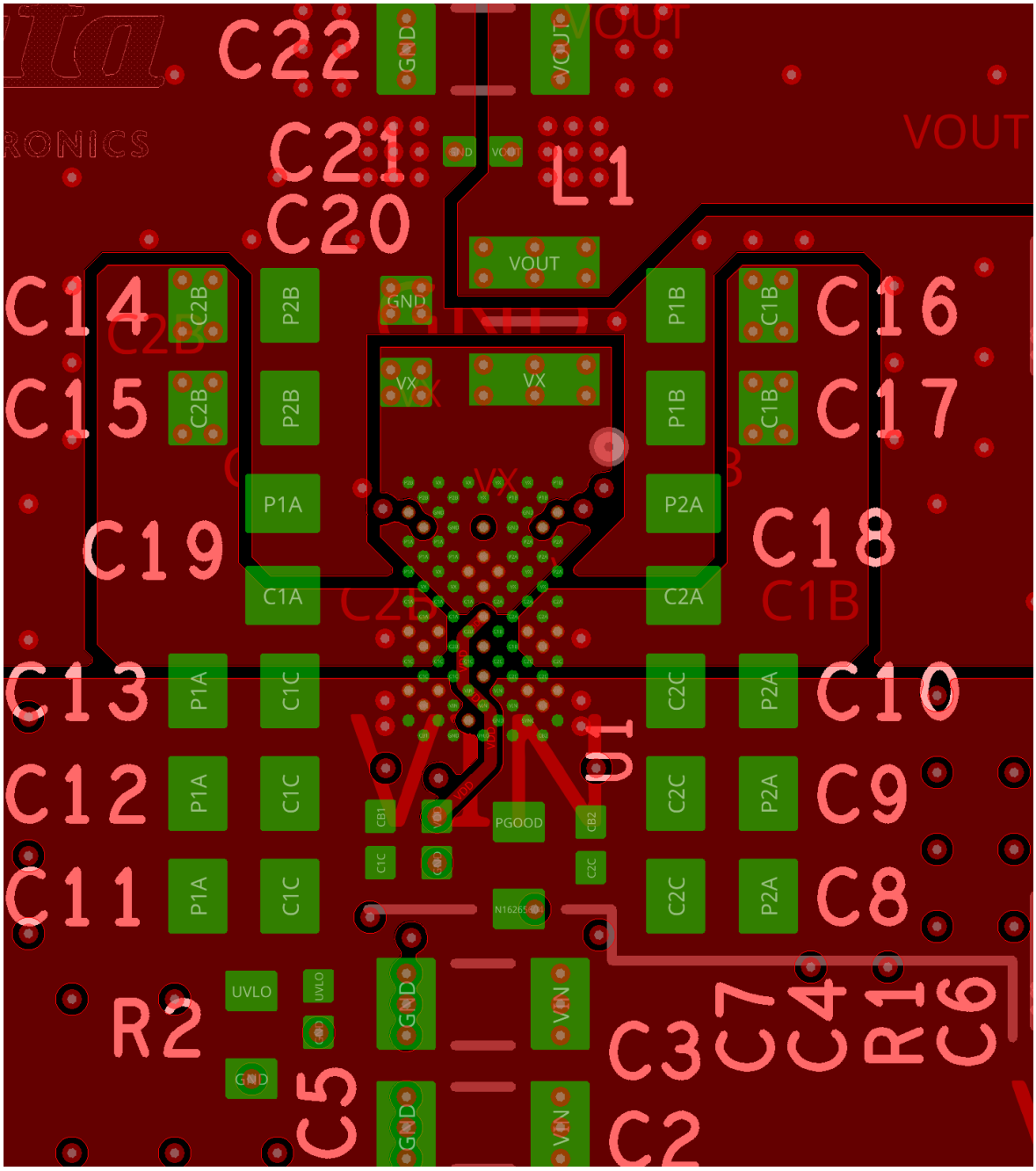


Figure 30. Bottom Layer

Pin Connections for Parallel Operation

In parallel operation, the pin connection is slightly different from single operation, as shown in Figure 31.

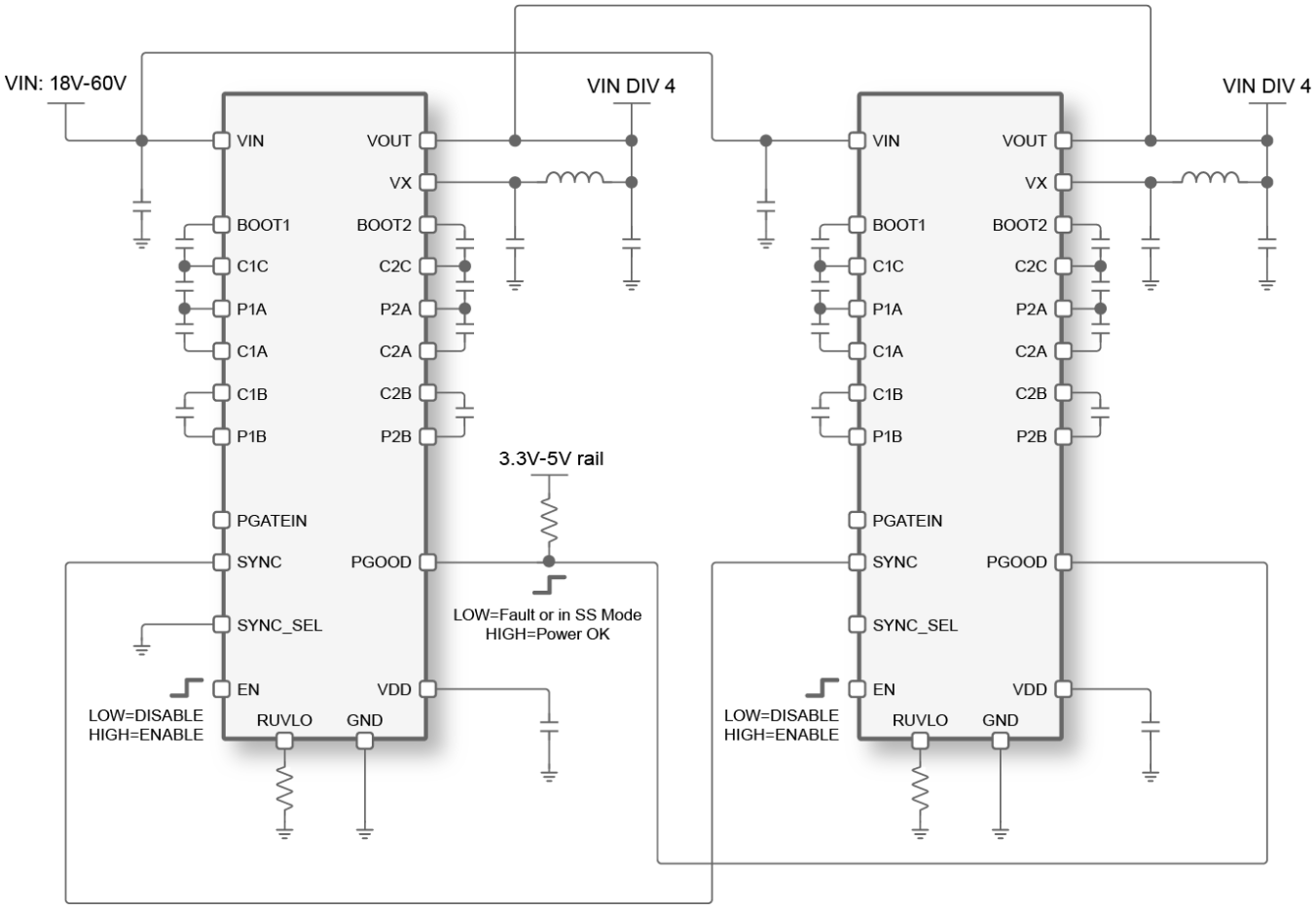


Figure 31. PE25204 Parallel Operation

Combine the PGOOD outputs in a wired OR configuration. Do not switch on the load following the charge pumps on until the common PGOOD signal goes high, then switch of the load immediately if any of the PGOOD outputs switch low after startup. In normal operation, the PGOOD pin is connected to the enable pin of a downstream DC-DC converter.

Leave the SYNC_SEL pin floating on all but the first device. On the first device, connect SYNC_SEL to GND so that the device provides the clock to the other devices connected in parallel.

Charge Pump Architecture and Important Notice

A charge pump-based DC-DC converter uses multiple low-impedance switches to take advantage of the higher energy density available in capacitors—compared to inductors—to transfer power. The keys to optimizing charge pump efficiency include reducing the charge redistribution losses and minimizing the thermal losses. The pSemi efficient charge pump series of products reduce the charge redistribution loss with patented *almost loss-less* architectures. The thermal losses are minimized by using lower voltage rated (internal) power FETs that take advantage of the reduced voltage as the input supply gets divided. These two key features make pSemi charge pumps very efficient. In exchange for the high efficiency, some of the differences regarding conventional buck converters must be recognized to avoid permanent damage to the device.

Soft Start and Capacitors Charge Balancing

The charge pump is an open-loop capacitive DC-DC converter. The output voltage is generated using “flying” capacitors (CFLY) that move the charge from one voltage level to another. The voltage across the flying capacitors in normal operation is limited to V_{OUT}. The voltage balancing between, and across, the flying capacitors is important to maintain stability. The PE25204 charge pump has several internal states that specifically enhance stability including “pre-charge” and “soft start.” During pre-charge, each of the CFLY capacitors is charged to the applicable DC voltage bias level—depending on both VOUT and Division ratio—to ensure a balanced state at startup.

During soft start, the charge pump starts switching with a controlled current—134 mA—to ramp V_{OUT} to the target voltage. The controlled start-up avoids in-rush current and EMI issues during turn-on and ensures that V_{OUT} reaches 95% of the output voltage before full power operation is enabled. As a further safety measure, the soft-start time is also monitored to ensure the system does not contain any unexpected leakage paths, such as V_{OUT} or CFLY shorts).

As a result of the limited soft-start current, the system does not support starting up into a full power load. The PGOOD pin indicates that the system is ready for full load when soft start has finished and V_{OUT} has reached at least 95% of the nominal target voltage. Any downstream power supply must wait for PGOOD to go high before enabling the downstream load. If PGOOD goes low due to a fault condition downstream, the loads must also be disconnected.

The soft-start timeout protection also means that the maximum output capacitance must be limited for reliable startup. Increasing COUT beyond the recommended level could mean that the charge pump requires several attempts to start up.

Hard Short Circuit Condition

The charge pump is a capacitive DC-DC converter and— deliberately—has low inductance at the output to optimize efficiency. As a result of the low output inductance, a hard short at the charge pump output can result in a high current di/dt condition which can be much higher than a conventional inductive buck converter would allow. The PE25204 charge pump has two levels of built-in output current protection:

- The first protection level is a relatively slow detector that reacts to the average output current.
- The second protection level is a quick detector (~1 µs) to protect against transient load current faults.

The combined over-current protection scheme is designed to prevent damage in the event of hard shorts.

The input voltage can be connected through an optional P-type FET to the input voltage at VIN. The purpose of this FET is to prevent power being transferred from the output to the input of the system. When a UVLO condition is detected, PGATE is turned off to prevent the power going into the system input. Figure 20 shows the PGATE pin behavior.

Packaging Information

This section provides the following packaging data:

- Moisture sensitivity level (MSL)
- Package drawing
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE25204 in the WLCSP package is MSL 1 per JEDEC standard J-STD-020E.

Package Drawing

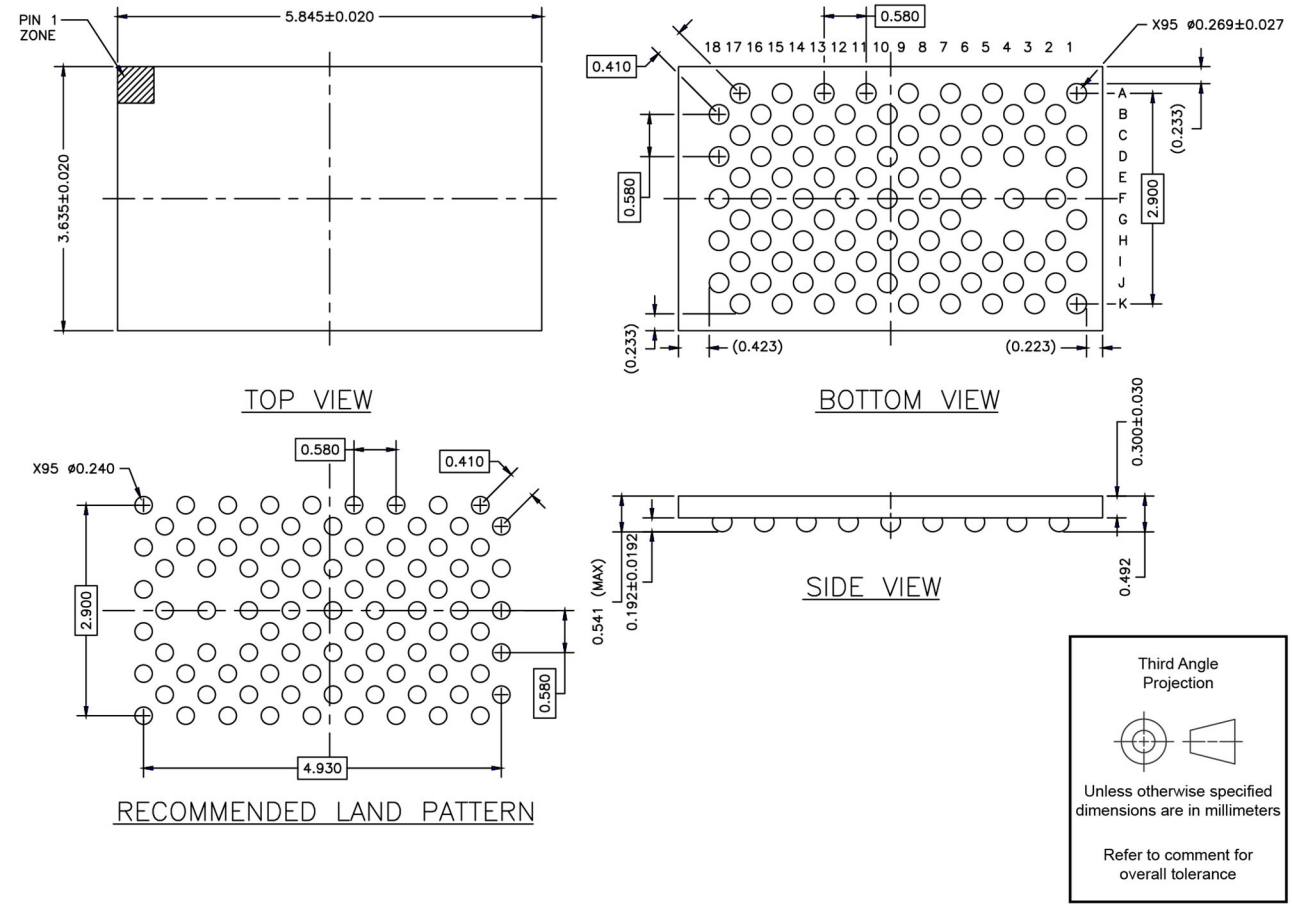


Figure 32. WLCSP Package Mechanical Drawing

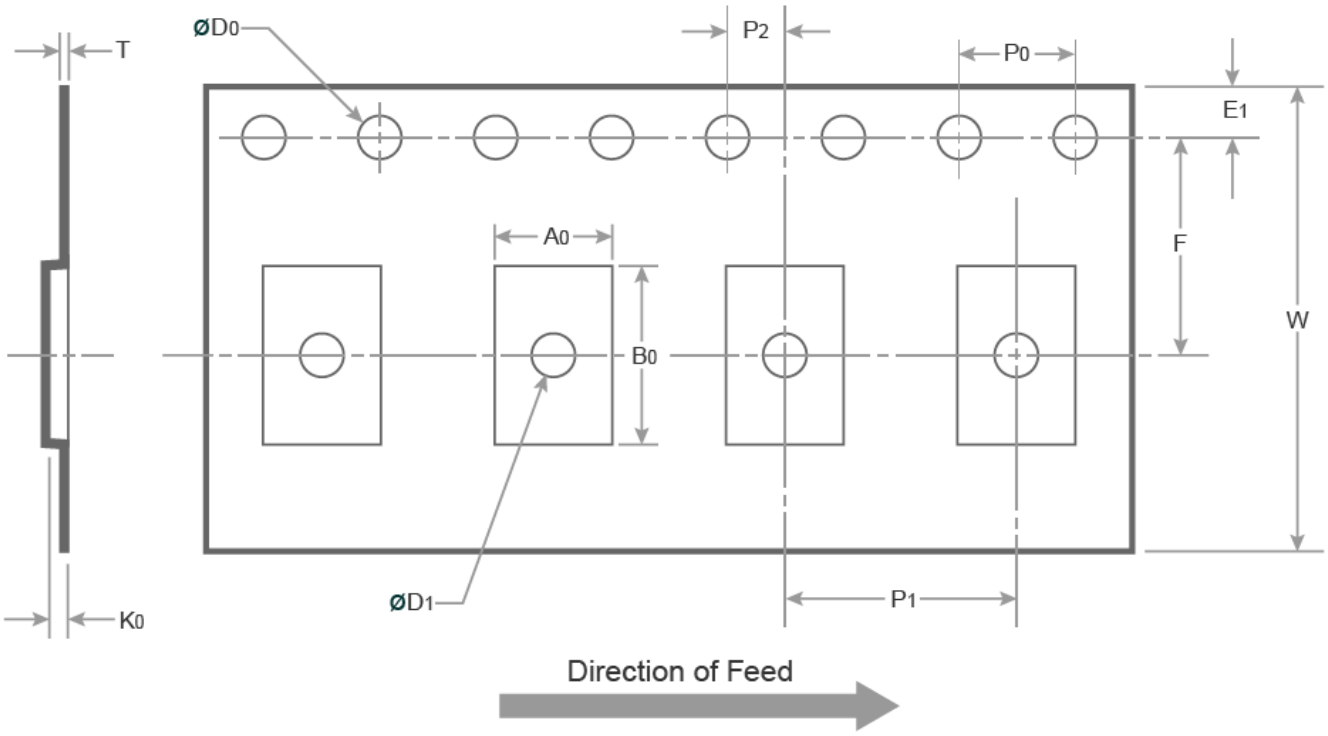
Top-Marking Specification

● = Pin 1 indicator
PPPPP = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
CB = Supplier code
Y = Last digit of assembly year (2020 = 0)
M = Assembly month (1,2,3...9,O,N,D)
DD = Assembly day (01,02,03...31)

DOC-100127-1

Figure 33. WLCSP Package Marking Specification

Tape and Reel Specification



Notes:

Not drawn to scale.
Dimensions are in millimeters.
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table					
Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
A_0	4.01	+/- 0.05	D_1	1.50	+ 0.25
B_0	6.10	+/- 0.05	D_0	1.50	+ 0.10
K_0	0.63	+/- 0.05	E_1	1.75	+/- 0.10
P_1	8.00	+/- 0.10	P_0	4.00	+/- 0.10
W	16.00	+ 0.30 / - 0.10	P_2	2.00	+/- 0.10
F	7.50	+/- 0.10	T	0.25	+/- 0.02

Figure 34. WLCSP Tape and Reel Specification

Ordering Information

Table 9 lists the PE25204 order codes and shipping methods.

Table 9. PE25204 Order Codes and Shipping Methods

Order Code	Description	Packaging	Shipping Method
PE25204A-X	6A Divide-by-4 Charge Pump	WLCSP	500 Units/Tape and Reel

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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