PE25208

Document Category: Product Specification

48 V_{IN} Divide-by-2- and -3, 8A Charge Pump, Capacitor Divider

General Description

The PE25208 is an ultra-high efficiency charge pump IC that is configurable to divide down an input voltage by two or three and delivers up to 8A with peak efficiency up to 98.2%. The PE25208 can also be used in parallel to increase output power

The PE25208 supports an input voltage range of 18V to 45V in divide-by-2 mode and 18V to 60V in divide-by-3 mode. The PE25208 is primarily used as a front-end converter to convert the USB PD EPR input to a lower voltage for downstream charger circuit with improved overall system efficiency.

The PE25208 comes in an 8.095 mm × 4.095 mm 148-pin WLCSP package. The pinout is specially designed to be fully compatible with Type III PCB design.

Features

- Proprietary architecture enables industry-leading efficiency in an ultra-compact footprint and low-profile solution
- Parts can be operated in parallel for higher output power
- Input voltage range of 18V to 60V supports USB PD EPR input and custom AC–DC bricks
- Peak efficiency of 98.2%
- Selectable divide-by-3 or divide-by-2 mode
- Fully protected with input under-voltage, output short circuit detection and thermal shutdown fault detection
- Low EMI fixed-frequency operation under heavy load conditions

Applications

- Ultrabooks/notebook computers
- Portable workstations
- Gaming laptops

Efficiency

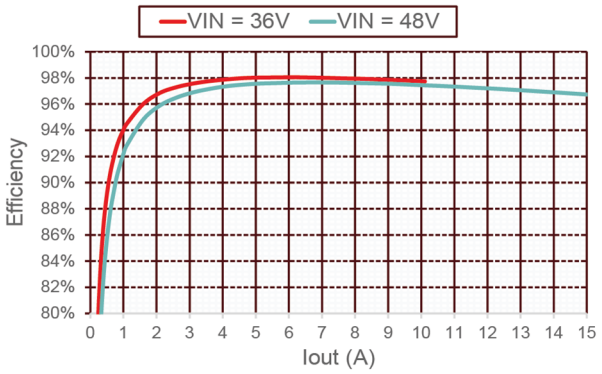


Figure 1. PE25208 typical efficiency vs. I_{OUT} at 48V divide-by-3 and 36V divide-by-2 parallel operations

Application

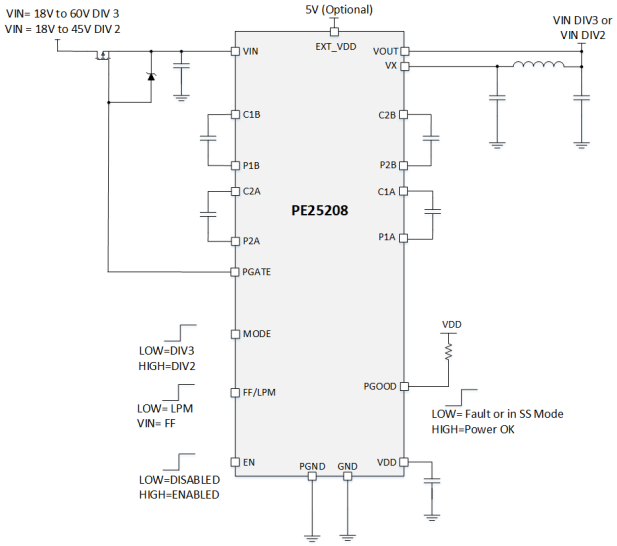


Figure 2. PE25208 Typical Application Circuit

Table of Contents

Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. PE25208 Absolute Maximum Ratings[1]

Parameter	Condition	Min	Max	Unit
FREQ, MODE, FF/LPM, SYNC, SYNC_SEL, PGOOD, EXT_VDD, VDD to AGND	–	-0.3	6	V
PGATE to PGND	–	-0.3	62	V
VIN to PGATE	–	-0.3	6	V
VIN to PGND	Divide-by-2 mode	-0.3	46	V
	Divide-by-3 mode	-0.3	62	
VOUT to PGND	Divide-by-2 mode	-0.3	23	V
	Divide-by-3 mode	-0.3	20.5	
EN to AGND	–	-0.3	VIN+0.3	V
VX, P1A, P1B, P2A, P2B to PGND	–	-0.3	28	V
C1A, C2A to PGND	–	-0.3	33	V
C1B, C2B to PGND	–	-0.3	49	V
AGND to PGND	–	-0.3	+0.3	V
ESD tolerance	HBM[2]	–	2500	V
ESD tolerance	CDM[3]	–	1000	V
Junction temperature	–	–	150	°C
Storage temperature	–	-65	150	°C
Soldering temperature	–	–	260	°C

Notes:

1. The above “Absolute Maximum Ratings” are stress ratings only; the notation of these conditions does not imply functional operation of the IC at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human Body Model, per the JEDEC standard JS-001-2012.
3. Field Induced Charge IC Model, per the JEDEC standard JESD22-C101.

Recommended Operating Conditions

Table 2 lists the PE25208 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE25208 Recommended Operating Conditions

Parameter	Min	Max	Unit
Input voltage V_{IN} range, relative to AGND or PGND, divide-by-3 mode	18	60	V
Input voltage V_{IN} range, relative to AGND or PGND, divide-by-2 mode	18	45	V
Output voltage V_{OUT} range, relative to AGND or PGND, divide-by-3 mode	6	20	V
Output voltage V_{OUT} range, relative to AGND or PGND, divide-by-2 mode	9	22.5	V
Junction temperature	-40	125	°C

Package Thermal Characteristics

Table 3. PE25208 Package Thermal Characteristics

Parameter	Condition	Min	Max	Unit
Junction-to-case top thermal resistance (ΘJT)	JEDEC JESD51-12-01 and JESD15-3	1.93	–	°C/W
Junction-to-board thermal resistance (ΘJB)	JEDEC JESD51-12-01 and JESD15-3	1.61	–	°C/W
Junction-to-air thermal characterization (ΘJA)	–	11.2	–	°C/W
Note: * Package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-12. See also pSemi Application Note 57: *Thermal Characterization*.				

Electrical Specifications

Table 4 lists the PE25208 key electrical specifications at the following specifications, unless otherwise specified:

V_{IN} = 48V, T_J = -40 ºC to +125 ºC, MODE = logic low, components from BOM on Table 7. Typical values are at T_A = 25 ºC

Table 4. PE25208 Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input supply						
Input voltage range	V_{IN}	Mode = Logic high (divide-by-2)	18	–	45	V
		Mode = Logic high (divide-by-2)	18	–	60	
Input voltage under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} rising	–	17	18	V
Input voltage under-voltage lockout (UVLO) hysteresis	V_{IN_HYST}	–	–	0.65	–	V
EXT_VDD external input range	V_{EXT_VDD}	–	4.75	–	5.5	V
External V_{DD} under-voltage lockout (UVLO) threshold	$V_{EXT\_VDDUVLO}$	–	–	–	4.56	V
External V_{DD} under-voltage lockout (UVLO) hysteresis	$V_{EXT\_VDDHYST}$	–	–	60	–	mV
Supply currents						
Shutdown supply current	I_{VIN_SHDN}	EN = 0V @ 25 °C	–	–	2	µA
Operating supply current	I_{VIN}	V_{IN} = 48V, ILOAD = 5 mA, FF/LPM = GND, V_{EXT_VDD}=5V	–	5	–	mA
EXT_VDD external supply current	I_{VDD}	V_{EXT_VDD} = 5V part switching, full load	–	6	10	mA
DC-DC converter						
Nominal output voltage	V_{OUT}	MODE = Logic low, no load	–	$V_{IN}/3$	–	V
		MODE = Logic high, no load	–	$V_{IN}/2$	–	
Maximum output power*	P_{OUT}	V_{IN} = 60V, divide-by-3 mode	160	–	–	W
		V_{IN} = 40V, divide-by-2 mode	120	–	–	
Maximum output current	I_{OUT}	MODE = Logic low V_{IN} = 18V to 58V, T_J = -40 ºC to +125 ºC V_{IN} = 58V to 60V, T_J = -20 ºC to +125 ºC	8	–	–	A
		MODE = Logic high	6	–	–	
Output current limit	I_{LIM}	MODE = Logic low	–	9.4	–	A
		MODE = Logic high	–	7.6	–	
PGATE specifications						
PGATE pull-down resistance	R_{PGATE_PD}	Enable external P-channel Disconnect FET	–	5	–	kΩ
PGATE pull-up resistance	R_{PGATE_PU}	Disable external P-channel disconnect FET	–	3	–	kΩ

Frequency settings						
Switching frequency	FREQ	–	–	300	–	kHz
Minimum frequency in LPM	–	FF/LPM = GND, I_{LOAD} = 0 mA	–	1/4 * FREQ	–	kHz
Soft start						
Soft-start timeout duration	–	–	–	6	–	ms
Soft-start input current limit	I_{SS_ILIM}	–	–	70	–	mA
Power good threshold						
Power good threshold	–	–	90	–	95	% V_{OUT}
Protection specifications						
VOUT under-voltage protection threshold	–	Mode = Logic high	0.8* V_{IN}/2	–	0.9* V_{IN}/2	V
		Mode = Logic low	0.8* V_{IN}/3	–	0.9* V_{IN}/3	
VX over-voltage protection	VX_{OVP}	–	30	–	–	V
Thermal shutdown	OTP	T_J, I_{LOAD}=0 mA	–	155	–	ºC
Thermal shutdown hysteresis	OTP_{HYST}	–	–	15	–	ºC
Logic pins EN, FF/LPM, MODE, and PGOOD						
PGOOD pin leakage	I_{PGOOD}	V_{PGOOD} = 5.5V	–	–	15	µA
PGOOD pull down resistance	–	–	–	–	18.5	Ω
PGOOD logic high voltage	V_{IH_PGOOD}	–	1.3	–	–	V
PGOOD logic low voltage	V_{IL_PGOOD}	–	–	–	0.4	V
PGOOD input hysteresis	V_{HYS_PGOOD}	–	–	0.5	–	V
Time for PGOOD detect	–	–	–	5	–	µs
PGOOD output initial wait time	t_{WAIT_PGOOD}	Initial wait time from EN logic high to first valid PGOOD output	–	40	–	µs
EN, FF/LPM, MODE logic high voltage	V_{IH}	–	1.5	–	–	V
EN, FF/LPM, MODE input low voltage	V_{IL}	–	–	–	0.4	V
EN pin leakage	I_{EN}	V_{IN} = 48V	–	–	40	µA
		V_{IN} = 5.5V	–	–	1	
FF/LPM, MODE pin leakage	I_{IO}	V_{IO} = 5.5V	–	–	2	µA
EN input minimum off time	$T_{ENL\_OFF\_MIN}$	Minimum logic low duration for shutdown	–	15	–	µs
Switchover time LPM to FF	–	Time to switch between LPM and FF mode before full power can be drawn	–	15	–	µs

Note: * The maximum output power depends on the system thermal solution and the ambient temperature.

Pin Information

This section provides the PE25208 pin configuration information. Figure 3 shows the pin map of this device for the WLCSP package, and Table 5 lists the description for each pin.

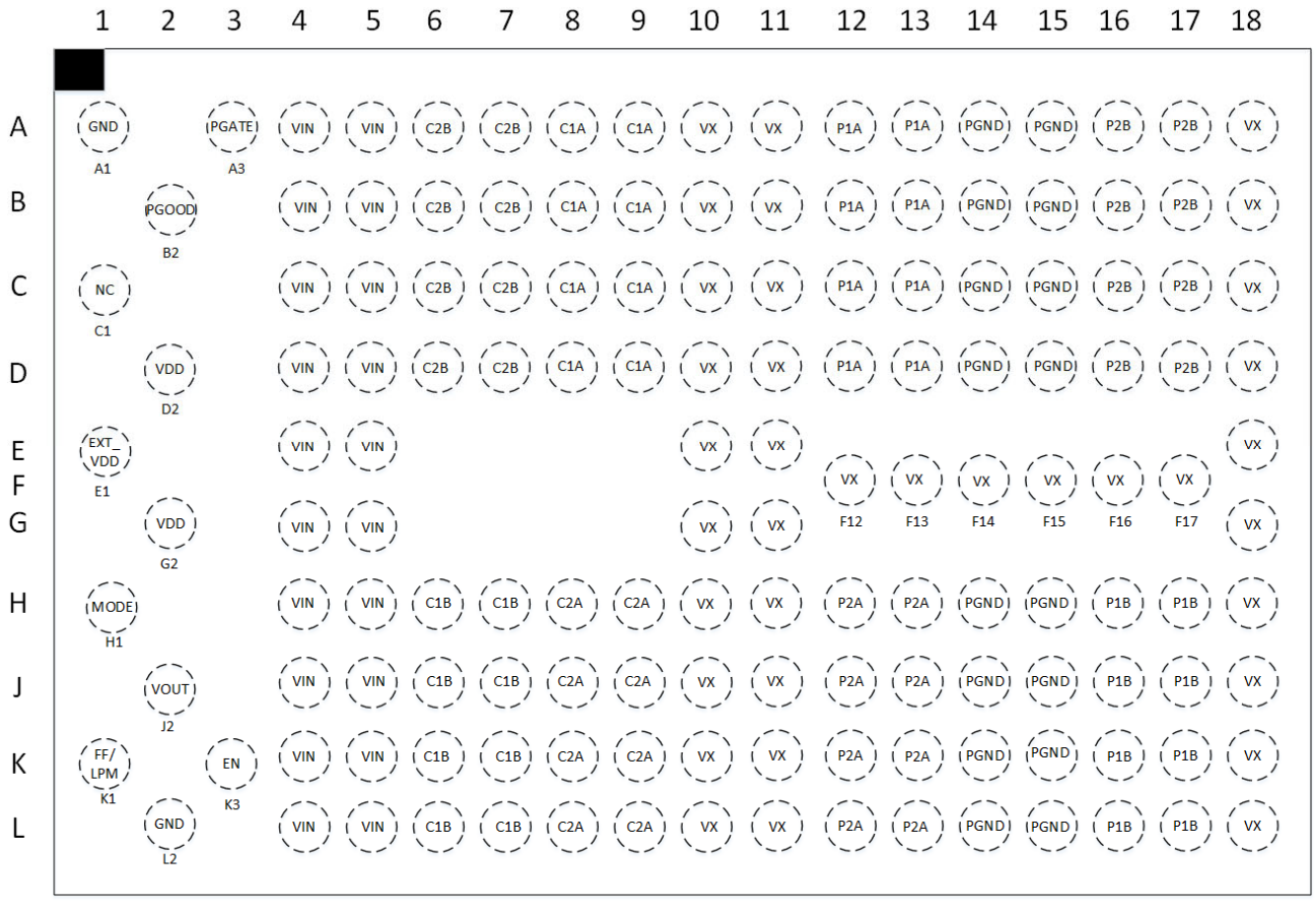


Figure 3. Pin Configuration (Top-Down View)

Pin Descriptions

Table 5. PE25208 Pin Descriptions

Pin Number	Pin Name	Description
A1	GND	Analog ground
A3	PGATE	Connect to external P-channel FET gate pin if the application requires reverse current to be blocked. Place a 5.6V Zener diode between PGATE and VIN pins for PGATE pin protection. In parallel operation, use the master IC to drive external P-channel FET only.
A4, A5, B4, B5, C4, C5, D4, D5, E4, E5, G4, G5, H4, H5, J4, J5, K4, K5, L4, L5	VIN	IC input voltage pins. Connect two 10 µF capacitors and two 1 µF capacitors between the VIN pins and the system ground.
A6, A7, B6, B7, C6, C7, D6, D7	C2B	Flying capacitor C2B terminal. Connect fly capacitor(s) between C2B and P2B pins.
A8, A9, B8, B9, C8, C9, D8, D9	C1A	Flying capacitor C1A terminal. Connect fly capacitor(s) between C1A and P1A pins.
A10, A11, A18, B10, B11, B18, C10, C11, C18, D10, D11, D18, E10, E11, E18, G10, G11, G18, H10, H11, H18, J10, J11, J18, K10, K11, K18, L10, L11, L18, F12, F13, F14, F15, F16, F17	VX	Charge pump output switching node. Connect to an external inductor.
A12, A13, B12, B13, C12, C13, D12, D13	P1A	Flying capacitor P1A phase node. Connect fly capacitor(s) between C1A and P1A pins.
A14, A15, B14, B15, C14, C15, D14, D15, H14, H15, J14, J15, K14, K15, L14, L15	PGND	Power ground
A16, A17, B16, B17, C16, C17, D16, D17	P2B	Flying capacitor P2B phase node. Connect fly capacitor(s) between C2B and P2B pins.
B2	PGOOD	Power good pin. Bidirectional pin must be pulled up with an external resistor to VDD pin or external voltage higher than 1.3V. In parallel operation, tie the PGOOD pin from all the ICs together.
C1	NC	Do not connect.
D2	VDD	Connect this pin to VDD on pin G2.
E1	EXT_VDD	External V_{DD} can be connected to an external supply voltage between 4.75V and 5.5V to improve light load efficiency. If not connected, the IC will generate its own VDD with internal LDO on VDD pin.
G2	VDD	Internally generated VDD from VIN, bypass to ground with a capacitor of 1 µF. If EXT VDD is present, then the IC will draw power from that pin.
H1	MODE	Selects the divide-by-2 or divide-by-3 modes. When connected to GND, it is in divide-by-3 mode. When connected to VDD, it is in divide-by-2 mode. This pin is not dynamic and is only read at power-up. In parallel operation, tie the MODE pin from all the ICs together.
H6, H7, J6, J7, K6, K7, L6, L7	C1B	Flying capacitor C1B terminal. Connect the fly capacitor(s) between the C1B and P1B pins.
H8, H9, J8, J9, K8, K9, L8, L9	C2A	Flying capacitor C2A terminal. Connect the fly capacitor(s) between the C2A and P2A pins.

H12, H13, J12, J13, K12, K13, L12, L13	P2A	Flying capacitor P2A phase node. Connect the fly capacitor(s) between the C2A and P2A pins.
H16, H17, J16, J17, K16, K17, L16, L17	P1B	Flying capacitor P1B phase node. Connect the fly capacitor(s) between the C1B and P1B pins.
J2	VOUT	Output voltage sense. Connect to the other side of the VX inductor. In parallel operation, connect VOUT sense to the local VX inductor.
K1	FF/LPM	Fixed-frequency or low-power mode select pin. When connected to logic high, it is in fixed frequency mode. When connected to logic low, it is in low-power mode, and the switching frequency for the charge pump is divided by 4 to reduce quiescent current. In parallel operation, tie the FF/LPM pin from all the ICs together.
K3	EN	Enable pin. When enable is logic low, the IC is put into shutdown. When logic is high, the IC is enabled. This pin can also be pulled to VIN. In parallel operation, tie the EN pin from all the ICs together.
L2	GND	Analog ground

Functional Block Diagram

Figure 4 shows the PE25208 functional block diagram.

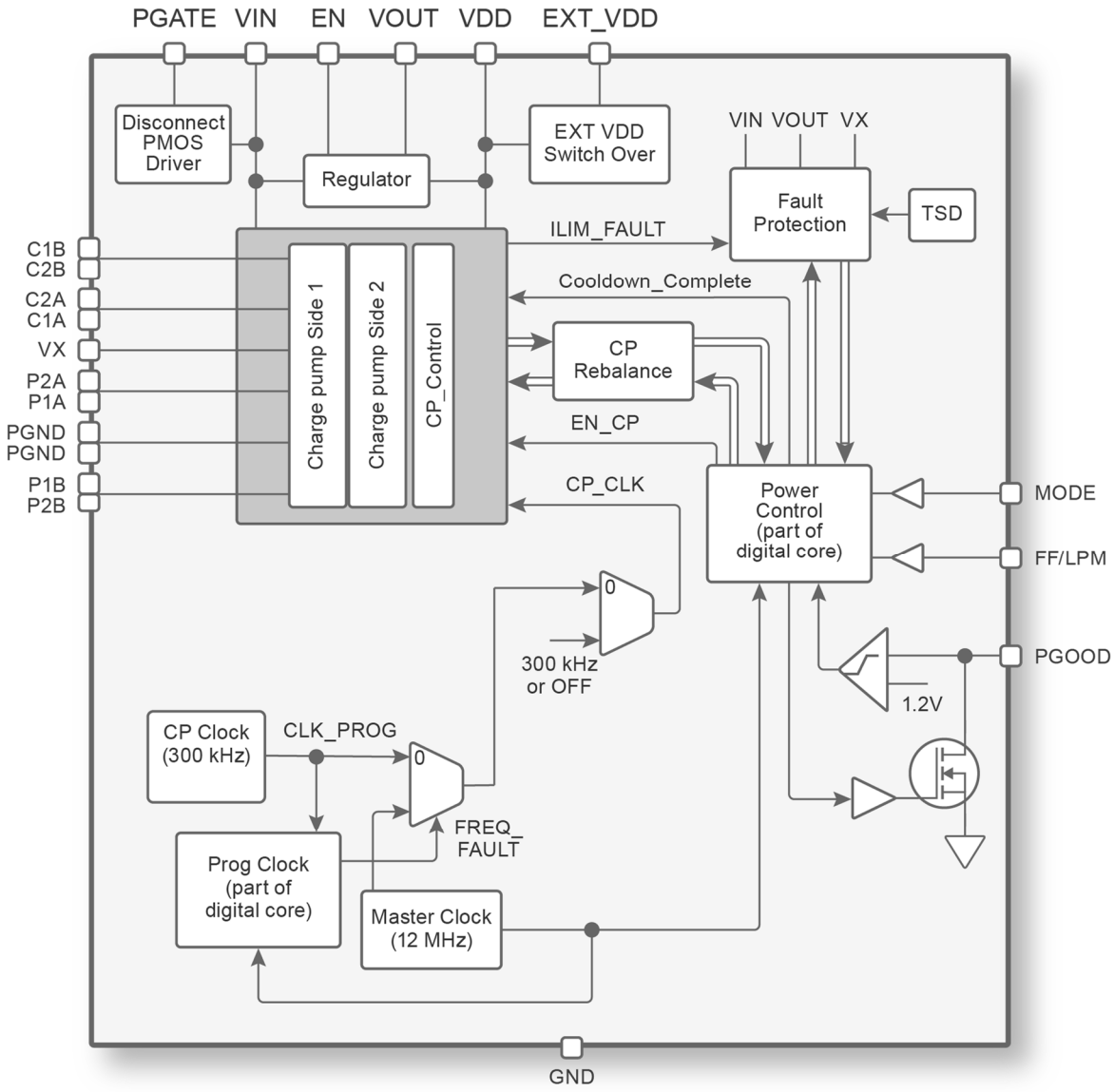


Figure 4. PE25208 Functional Block Diagram

Application Circuits

Figure 5 shows the application circuit for the PE25208 in single-IC operation.

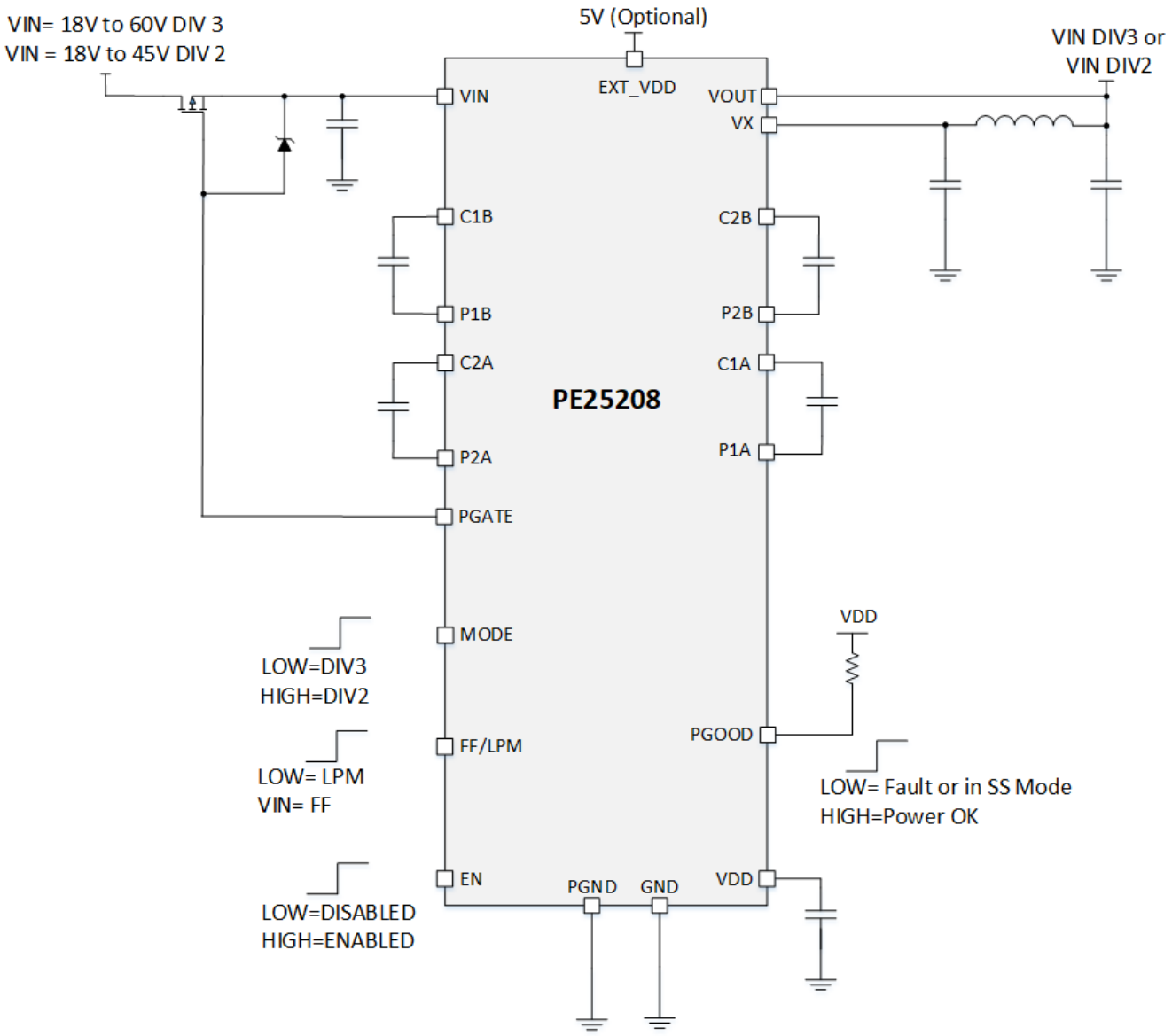


Figure 5. PE25208 Application Circuit in Single-IC Operation

Figure 6 shows the application circuit for the PE25208 in parallel-IC operation.

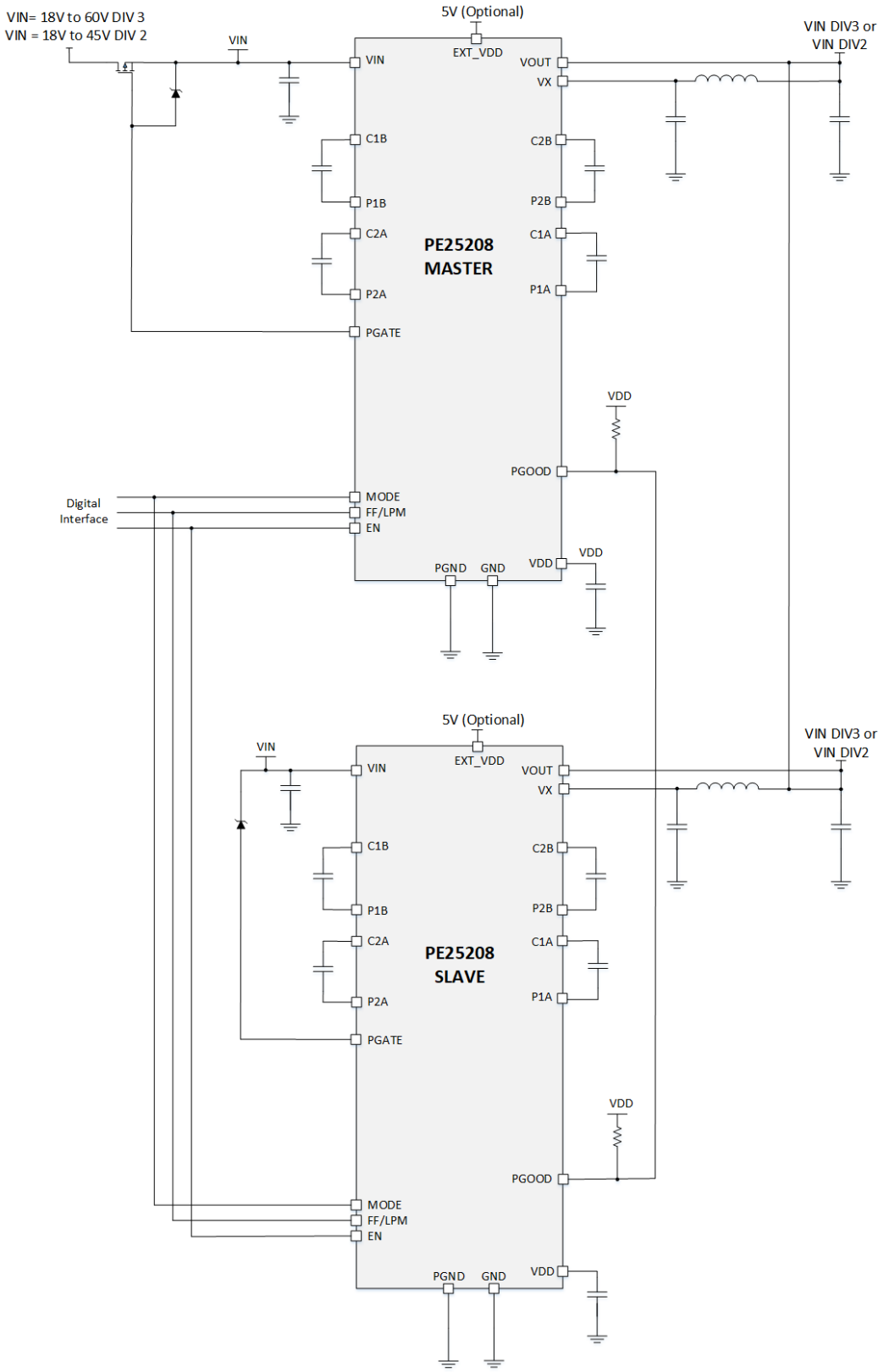


Figure 6. PE25208 Application Circuit in Parallel-IC Operation

Typical Performance Data

Figure 7–Figure 28 show the PE25208 typical performance data. The figures were measured according to the capacitances defined in the application circuit (see Figure 5 and Figure 6).

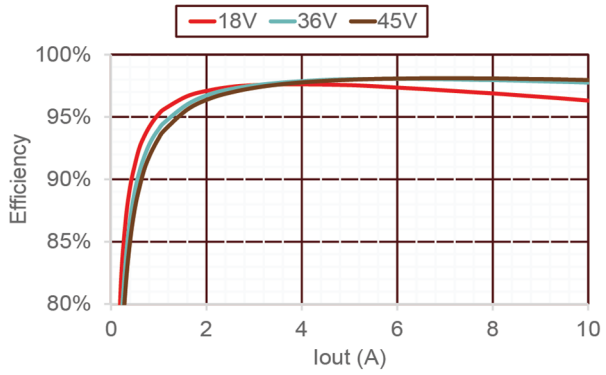


Figure 7. DIV 2 VIN = 18, 36, 45V. Efficiency vs. load current, fixed frequency, 25 °C, 300 kHz, internal VDD, parallel operation

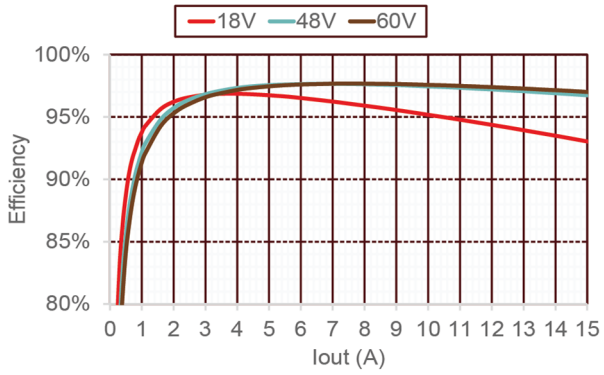


Figure 8. DIV 3 VIN = 18, 48, 60V. Efficiency vs. load current, fixed frequency, 25 °C, 300 kHz, internal VDD, parallel operation

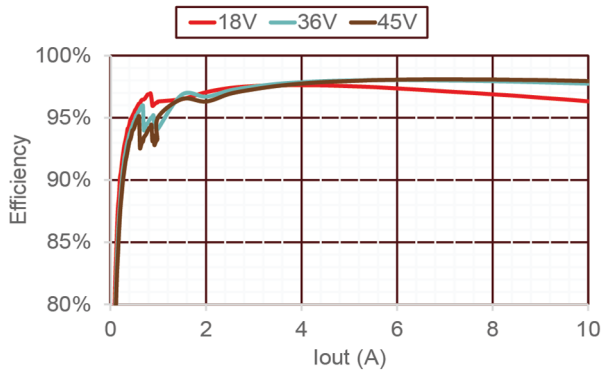


Figure 9. DIV 2 VIN = 18, 36, 45V. Efficiency vs. load current, low-power mode, 25 °C, 300 kHz, internal VDD, parallel operation

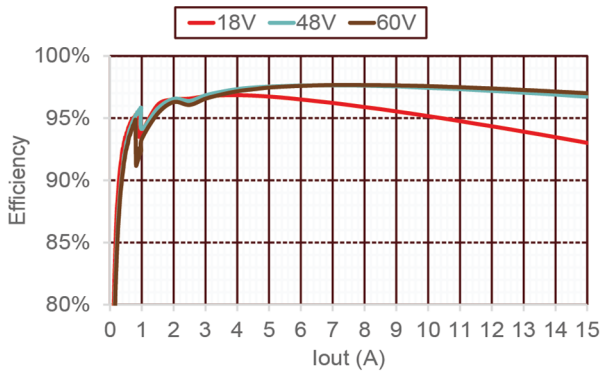


Figure 10. DIV 3 VIN = 18, 48, 60V. Efficiency vs. load current, low-power mode, 25 °C, 300 kHz, internal VDD, parallel operation

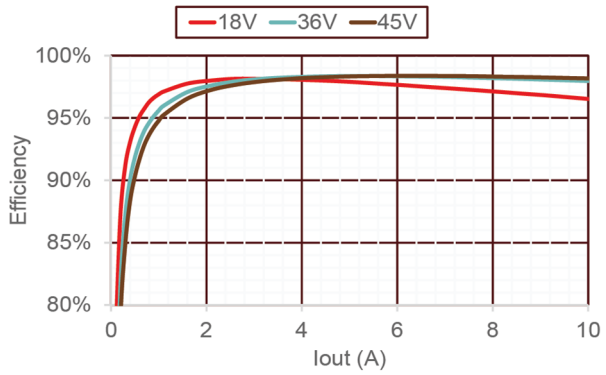


Figure 11. DIV 2 VIN = 18, 36, 45V. Efficiency vs. load current, fixed frequency, 25 °C, 300 kHz, external VDD, parallel operation

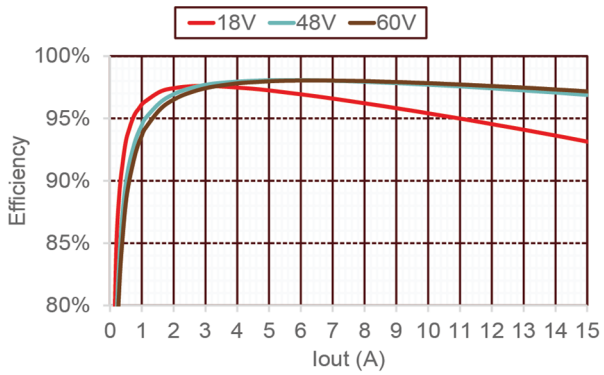


Figure 12. DIV 3 VIN = 18, 48, 60V. Efficiency vs. load current, fixed frequency, 25 °C, 300 kHz, external VDD, parallel operation

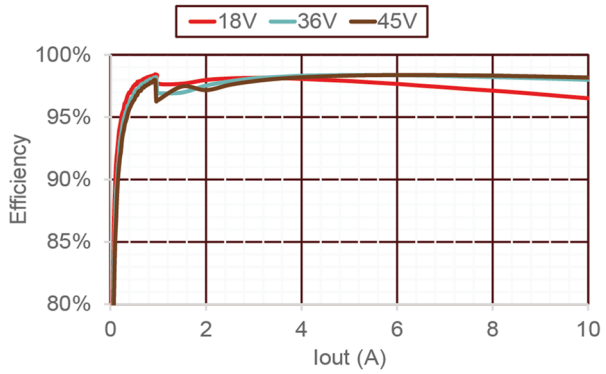


Figure 13. DIV 2 VIN = 18, 36, 45V. Efficiency vs. load current, low power mode, 25 °C, 300 kHz, external VDD, parallel operation

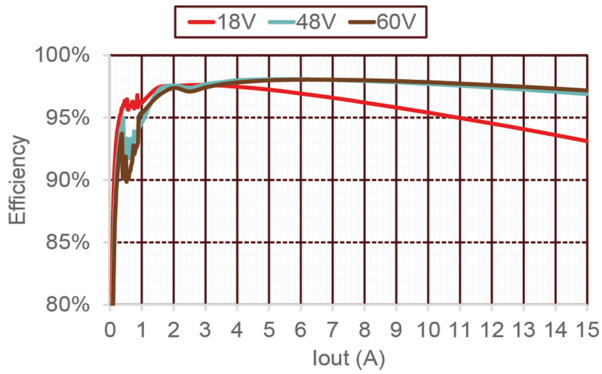


Figure 14. DIV 3 VIN = 18, 48, 60V. Efficiency vs. load current, low power mode, 25 °C, 300 kHz, external VDD, parallel operation

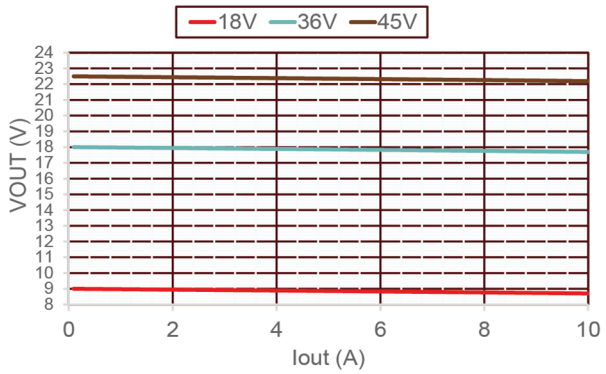


Figure 15. DIV 2 VOUT vs. load current, fixed frequency, 25 °C, 300 kHz, internal VDD, parallel operation

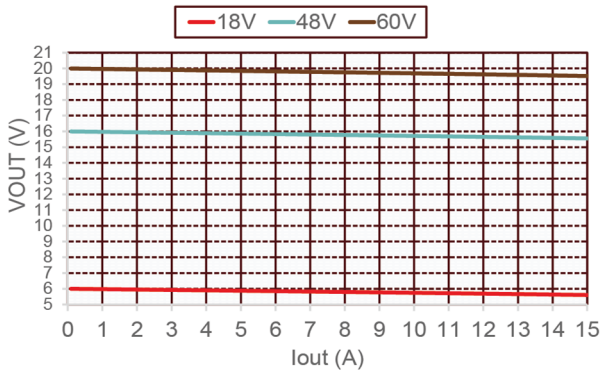


Figure 16. DIV 3 VOUT vs. load current, fixed frequency, 25 °C, 300 kHz, internal VDD, parallel operation

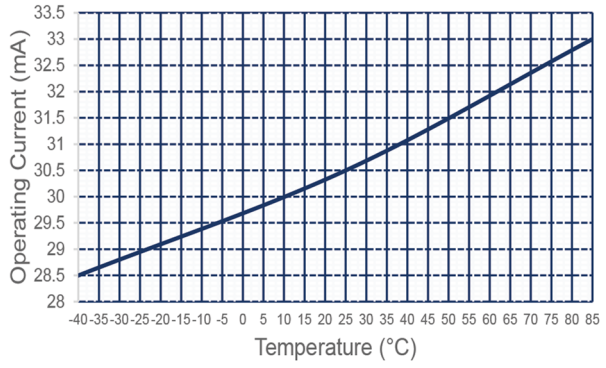


Figure 17. Operating current vs. temperature, DIV 2 VIN = 36V, fixed frequency, 300 kHz, internal VDD, parallel operation

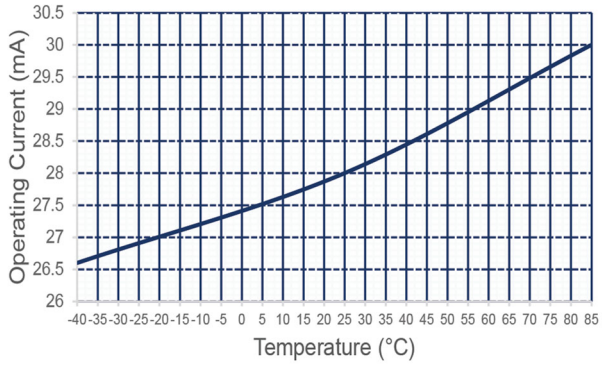


Figure 18. Operating current vs. temperature, DIV 3 VIN = 48V, fixed frequency, 300 kHz, internal VDD, parallel operation

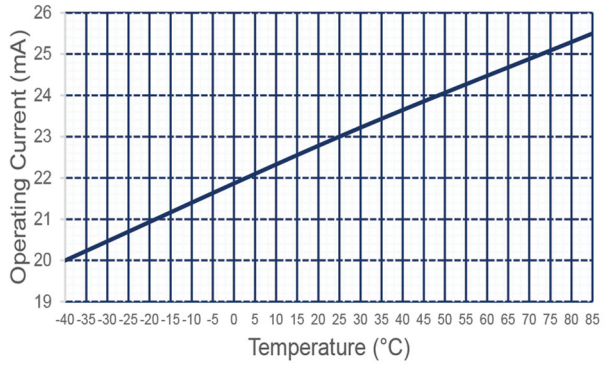


Figure 19. Operating current vs. temperature, DIV 2 VIN = 36V, low-power mode, 300 kHz, external VDD, parallel operation

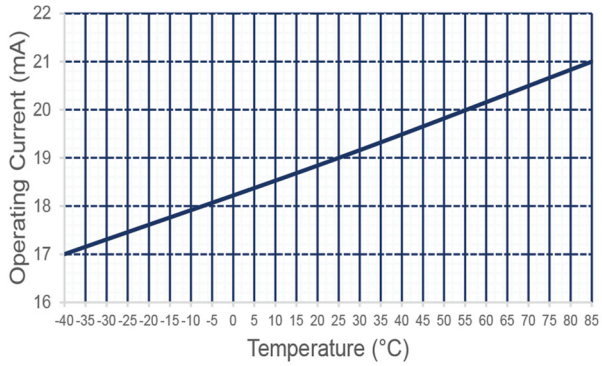


Figure 20. Operating current vs. temperature, DIV 3 VIN = 48V, low power mode, 300 kHz, external VDD, parallel operation

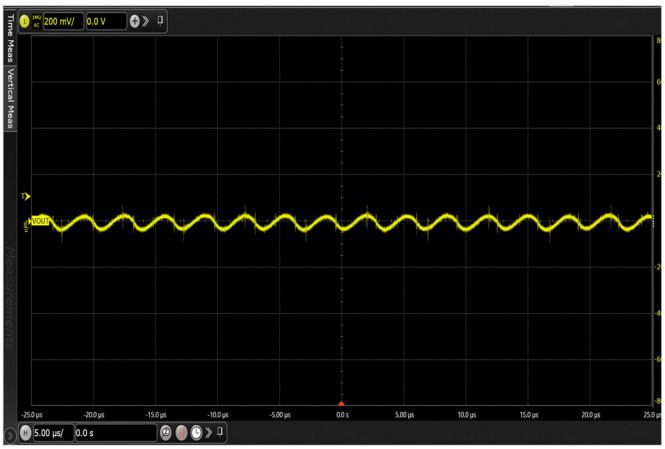


Figure 21. DIV 2 ripple (@ ILOAD = 6A), VIN = 36V, CLOAD = 80 µF, single operation

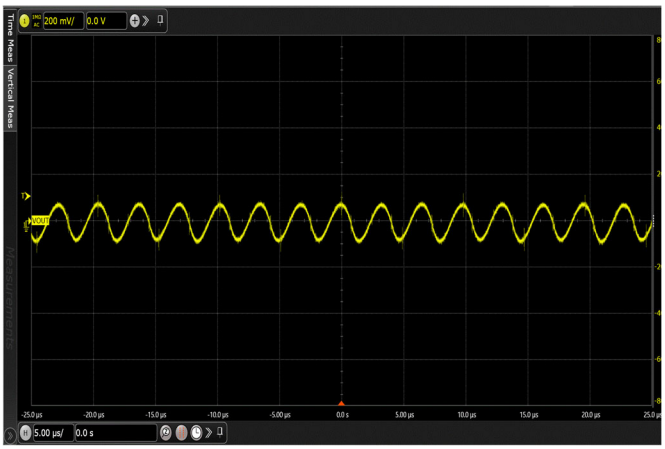


Figure 22. DIV 3 ripple (@ILOAD = 8A), VIN = 48V, CLOAD = 80 µF, single operation

Figure 23. DIV 2 VIN = 36V start up, CLOAD = 80 µF, single operation

Figure 24. DIV 3 VIN = 48V start up, CLOAD = 80 µF, single operation

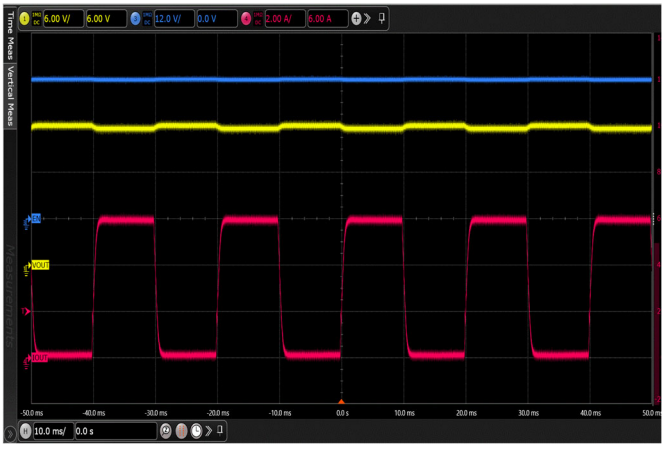


Figure 25. Load transient (0.1A - 6A) VIN = 36V DIV 2 CLOAD = 80 µF, single operation

Figure 26. Load transient (0.1A - 8A) VIN=48V DIV 3 CLOAD = 80µF, single operation

Figure 27. Line transient 24-36V ILOAD = 6A DIV 2 CLOAD = 80 µF single operation

Figure 28. Line transient 36-48V ILOAD = 8A DIV 3 CLOAD = 80 µF single operation

Detailed Description

The PE25208 is an ultra-high efficiency charge pump IC that is configurable to divide down an input voltage by two or three and delivers up to 8A with peak efficiency up to 98.2%. The PE25208 can also be used in parallel to increase output power.

A charge pump-based DC–DC converter is an open-loop, high-efficiency bus converter that does not have output regulation capability. Because of its architecture, it differs somewhat from conventional inductive buck converters, and some of its behaviors differ from buck converters. The PE25208 can be configured as an open-loop charge pump to either divide the input voltage by 2 or by 3.

The PE25208 supports an input voltage range of 18V to 45V in divide-by-2 mode and 18V to 60V in divide-by-3 mode. The under-voltage lockout is set at a fixed 17V typical and guaranteed to be out of under-voltage lockout by 18V.

The output voltage range supported in divide-by-2 configuration is 9V to 22.5V with load currents of up to 6A delivered to the external load. The output voltage range supported in divide-by-3 configuration is 6V to 20V with load currents of up to 8A delivered to the external load. To achieve higher power levels, connect multiple ICs in parallel.

Startup Operation

The pin configurations are sampled when the PE25208 starts up and before the charge pump stage is enabled. The configuration pins are not designed to be driven dynamically, so they must be in a fixed state at power-up except for the FF/LPM and EXT_VDD pins.

Enable (EN)

The PE25208 has an enable input pin (EN), which is designed to be compatible with typical low-voltage digital I/O levels so that it can be easily driven by an external controller. The EN pin can also be connected to the VIN pin.

If external power sequencing or control is not required, tie the EN pin to the VIN pin and do not leave it left open.

The PE25208 is enabled by an active-high EN input pin when a voltage greater than 1.5V is applied. The PE25208 is disabled when the voltage at the EN pin falls below 0.4V.

The EN pin can be shorted to the VIN pin to automatically enable the part with a minimal number of external components and PCB routing. When multiple PE25208s are used in parallel, connect all their EN pins to a single enable signal.

Input Under-voltage Lockout (UVLO)

The PE25208 provides continuous monitoring of the VIN input using a fixed under-voltage lockout. The PE25208 is enabled when the VIN voltage rises above 17V typical VIN_UVLO threshold and EN pulls to logic high.

When the VIN voltage falls below the VIN_UVLO threshold—VIN_HYST hysteresis—the charge pump circuit stops switching, the PGATE voltage pulls up to the VIN voltage to disable the external P-channel disconnect FET, and the IC shuts down. The PGOOD pin pulls low momentarily and enters the high-impedance state due to the IC UVLO shutdown.

Soft-Start Operation

The PE25208 is a high-power IC. To protect the system and the internal circuitry of the PE25208, power is supplied to the output and the flying capacitors in a controlled soft-start sequence.

To avoid excess thermal dissipation in the event of shorted output, the soft-start current is set to a typical 70 mA. Depending on the output capacitor setting, the PE25208 can take several soft-start cycles to ramp VOUT to the target voltage. Each soft-start cycle consists of a 6 ms timeout period and 60 ms cool down period for a total of 66 ms in each cycle. During both the soft-start and pre-charge phases, do not load VOUT until the PGOOD pin goes high. If a full load is connected before this, the IC does not start up and remains in soft start indefinitely.

Initialization Sequence

If the EN pin is held HIGH until VIN has reached its operating voltage, the PE25208 follows the initialization sequence shown in Figure 29.

If the EN pin is pulled LOW during the initialization sequence or normal operation, the PE25208 immediately shuts down with high impedance PGOOD.

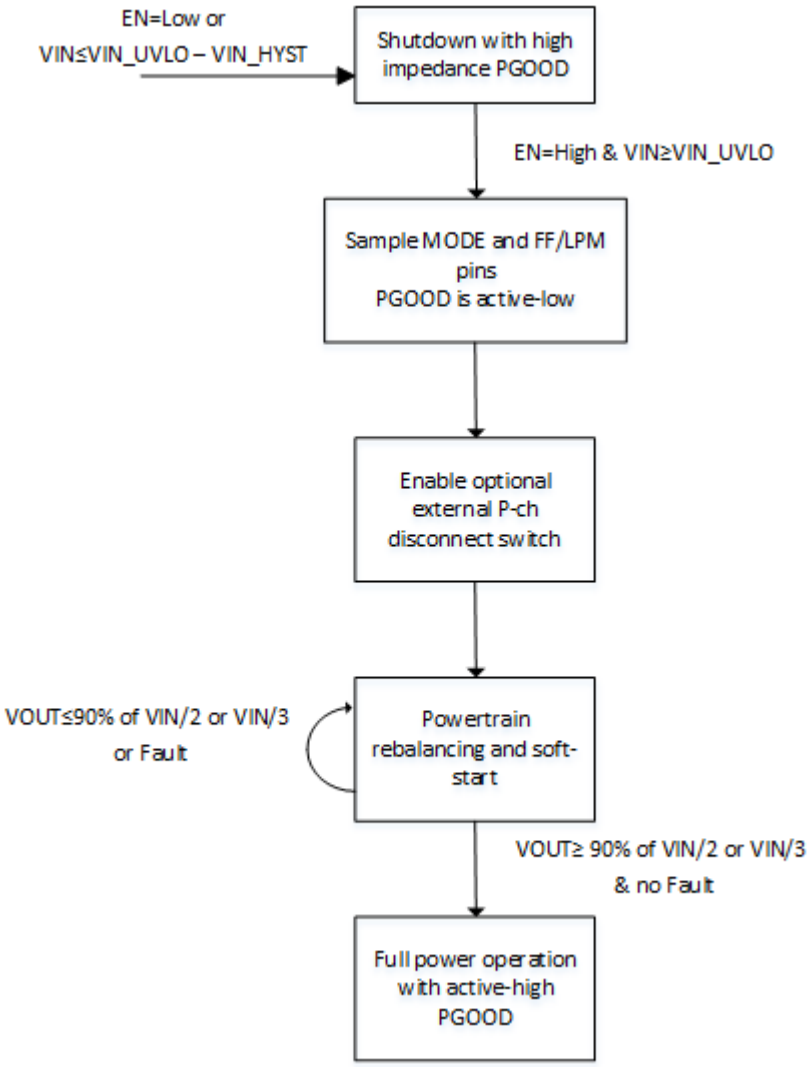


Figure 29. Initialization Sequence

P-channel Disconnect FET (PGATE)

The PE25208 supports an optional input disconnect switch between the system input supply and the VIN pin to prevent reverse power flow through the part during IC shutdown or fault condition. pSemi recommends a P-channel FET with the source terminal connected to the VIN pin, the drain terminal connected to the system input supply, and the gate terminal connected to the PGATE pin. The PE25208 pulls PGATE up to VIN to disable the disconnect switch. Connect a 5.6V Zener diode between PGATE and VIN to protect thePGATE pin. The PGATE pin sees the potential difference between VIN and the Zener diode, and this voltage difference drives the gate of the disconnect switch. Select a P-Channel FET with a Vgs that falls within the range of the 5.6V Zener diode voltage.

Power Good Indicator (PGOOD)

Power good (PGOOD) is an open-drain output that releases high after the output reaches above 95% of the target output voltage set by the MODE pin to VIN divide-by-2 or VIN divide-by-3.

After PGOOD is asserted, the PE25208 stops soft-start and enables full power operation. The PE25208 monitors the PGOOD pin directly, allowing an external capacitor to add filtering.

When multiple PE25208s are used in parallel, connect all their PGOOD pins together. In this case, all PE25208s must complete soft start before PGOOD is asserted and full power operation is allowed. In the event of a fault of one or more parallel PE25208s, the PGOOD pin is pulled low by the faulted PE25208(s), which in turn switches off the ICs connected in parallel. Then the ICs restart soft-start operation until the fault is cleared or the ICs are disabled.

The PGOOD pin of a disabled IC is NOT pulled low if the IC is not enabled. In effect, when the PE25208 is shut down by EN=0 or VIN UVLO, the PGOOD pin is in high impedance and can be ignored.

Protection Modes

To protect the system and the internal circuitry of PE25208, multiple fault detection circuits are built in.

Hard Short-Circuit Condition

The PE25208 is a capacitive DC-DC converter and has a low output inductance to optimize efficiency. As a result of the low output inductance, a hard short at the device output can result in a di/dt condition which can be much higher than a conventional, inductive, buck converter would allow.

The PE25208 has a built-in output protection. However, hard output shorts with very low impedance could cause permanent damage to the device and must be avoided. If such faults need to be considered, you might need to add primary protection—external to the device—to ensure adequate protection of the device.

Protection Features

Table 6 lists the various protection modes.

Table 6. Protection Modes

Protection	Persistent Fault*	Effect of the Fault on the PE25208
V_{IN} under-voltage	Yes	PGOOD goes low momentarily and then enters high impedance state. The PE25208 power stage is turned off through a soft shutdown. The IC shuts down until the V_{IN} voltage exceeds the V_{IN_UVLO} threshold.
V_{OUT} under-voltage	No	PGOOD goes low. The PE25208 power stage is turned off through a soft shutdown. After a cooldown period of 60 ms, the IC attempts to soft start again.
V_X over-voltage	Yes	PGOOD goes low. The PE25208 charge pump disconnects from V_{IN} (so no further power passes from V_{IN} to the load) but continues the clock to discharge the V_X node. When the V_X voltage falls below the V_{XOVP} threshold, the power stage fully turns off through a soft shutdown, and the IC attempts to soft start again.
V_{OUT} short circuit	No	PGOOD goes low. The PE25208 power stage is turned off through a soft shutdown. After a cooldown period of 60 ms, the IC attempts to soft start again.
V_{OUT} over-current	No	PGOOD goes low. The power stage of PE25208 is turned off through a soft shutdown. After a cooldown period of 60 ms, the IC attempts to soft start again.
Thermal shutdown	Yes	PGOOD goes low.

		The PE25208 power stage is turned off through a soft shutdown and stays off until the die temperature has reduced below the thermal shutdown level minus hysteresis. Then the power stage starts switching again.
Soft-start timeout	No	If VOUT does not reach the target voltage inside the soft-start timeout period of 6 ms, the charge pump enters a cooldown period of 60 ms before the IC attempts to soft-start again.
Note *: A persistent fault keeps the charge pump in a fault state for as long as the fault is present. A non-persistent fault does not prevent the charge pump from re-enabling after the fault recovery time has been applied.		

PGATE Reverse Charge Protection

Internal to the IC is a single disconnect switch, Q1 shown in Figure 30, which is a standard FET, so it has a parasitic diode. This diode stops current flowing from input to output when the Q1 is turned off, but it does not stop current flowing from output to input. This is necessary because a charge pump is inherently bi-directional.

To block reverse current, the PGATE pin allows for the addition of an external FET, Q2 shown in Figure 30, where the diode is placed in the standard back-to-back configuration with the diode from Q1. This FET mimics the functionality of Q1 to create a true bi-directional on/off switch.

- When the PE25208 enables, a pull-down from VIN is triggered to switch the external Q2 FET on.
- When the PE25208 disables, the PGATE pin is pulled high to VIN, thus turning off the Q2 FET.

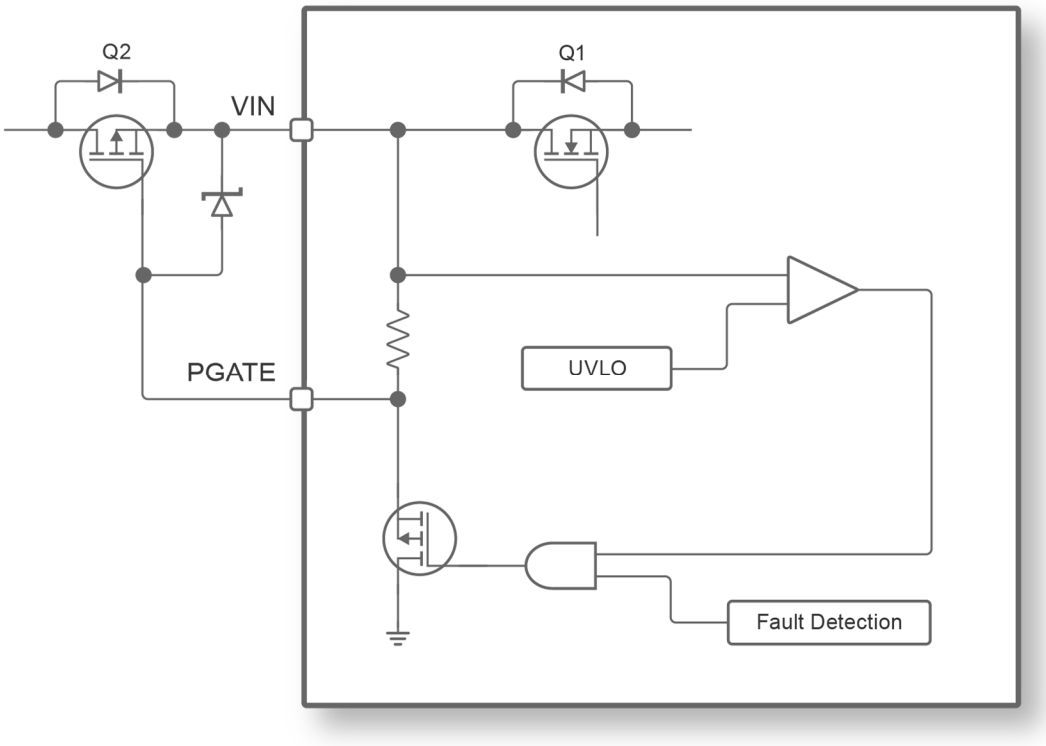


Figure 30. PGATE Operation Functional Diagram

Applications Information

The PE25208 is a charge pump-based DC-DC ratiometric converter. It is a high-efficiency bus converter in which the output follows the input by a fixed ratio of divide-by-2 or divide-by-3. Because of its architecture, there are differences from conventional inductive buck converters.

Application Schematics

Figure 31 and Figure 32 show the PE25208 application schematic examples. For the recommended components, see Table 7 and Table 8.

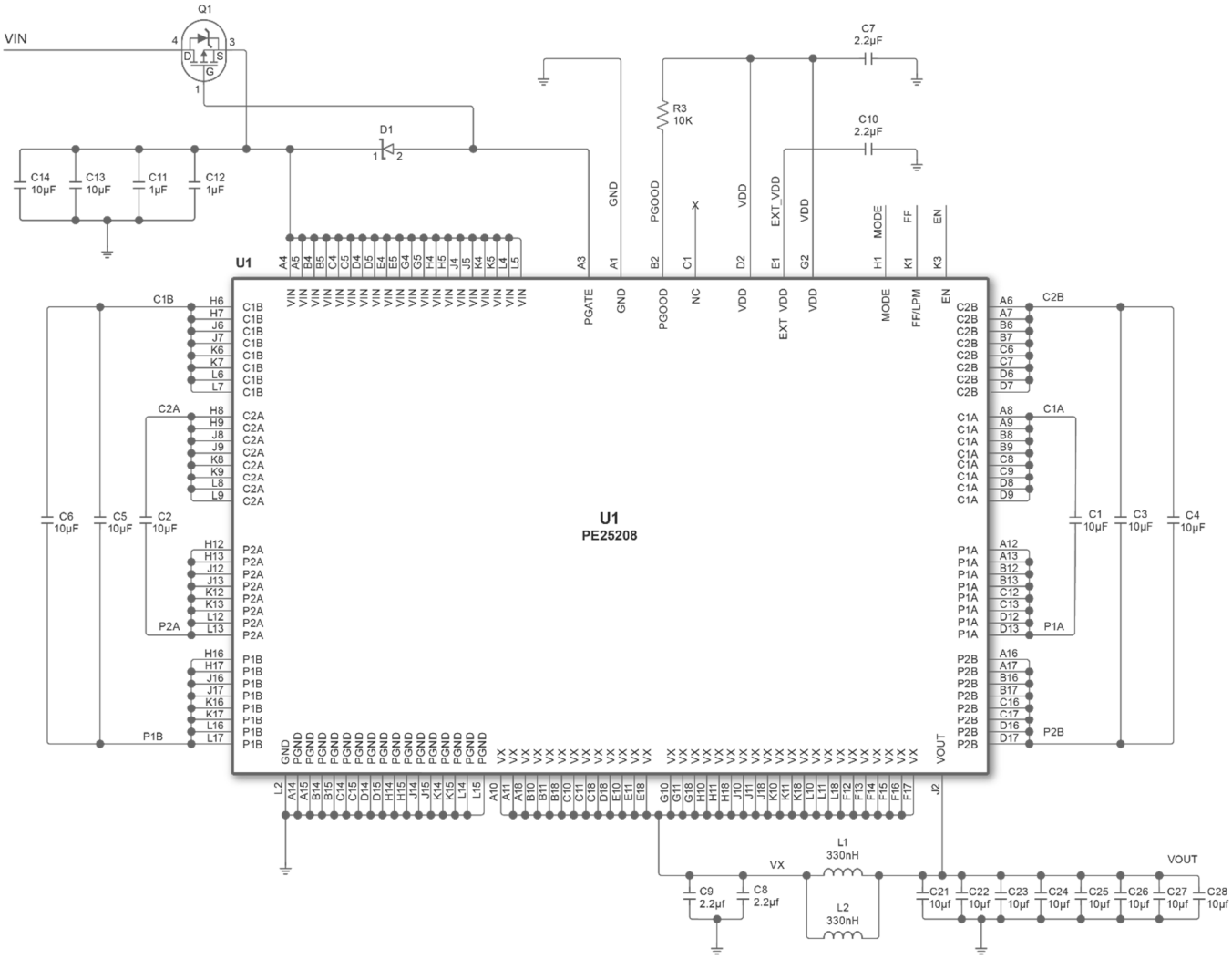


Figure 31. PE25208 Single Application Schematic

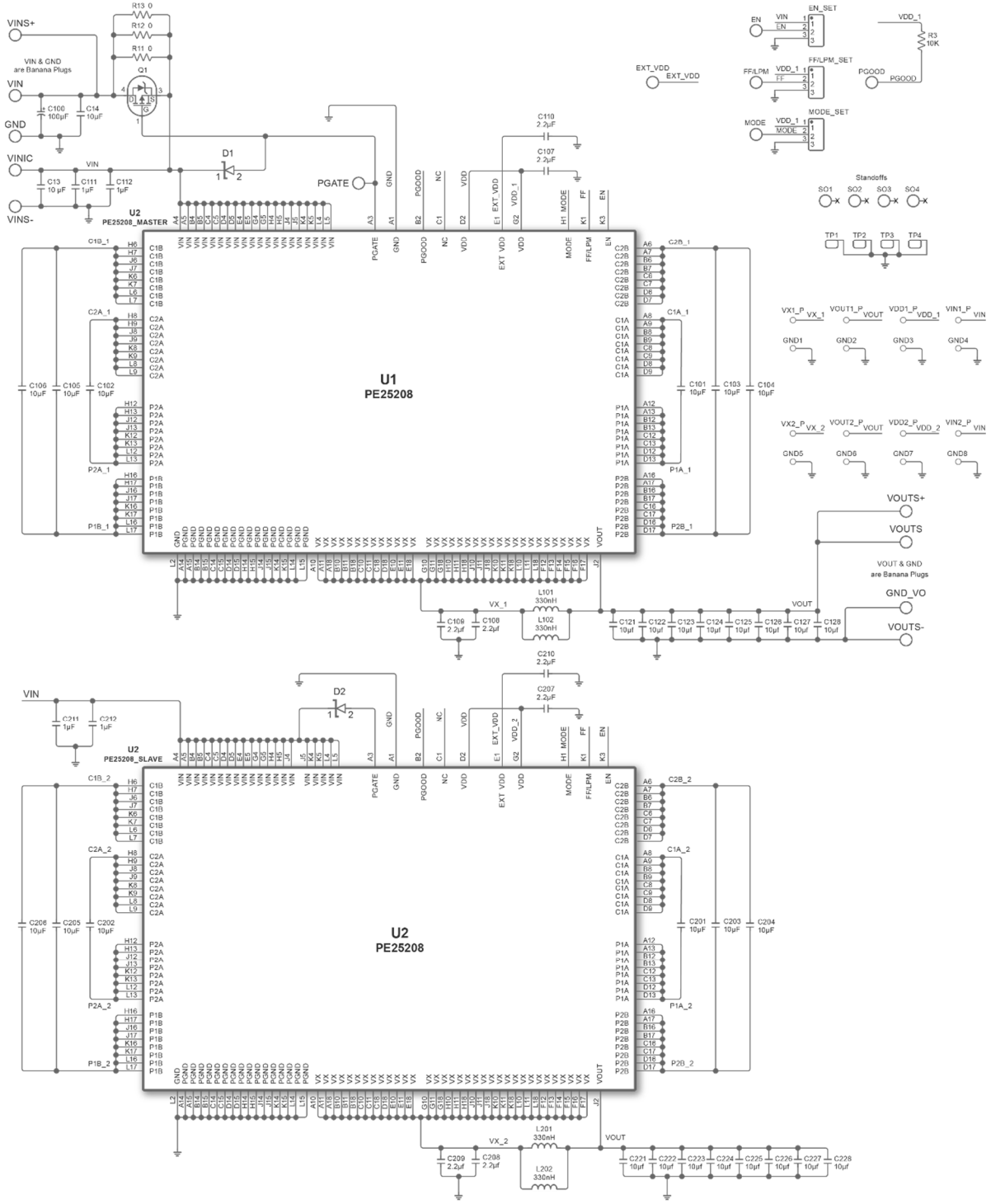


Figure 32. PE25208 Parallel Operation Schematic

Recommended Components

Table 7 lists examples of the standard components for the single application schematic in Figure 31. Table 8 lists examples of the standard components for the parallel application schematic in Figure 32. The components must be chosen by referring to system requirements, such as voltage, temperature, and so on. The information in these table is under evaluation and subject to change.

Table 7. PE25208 Single Recommended Components

Reference	Value	Description	Manufacturer	Part Number
C1, C2, C3, C4, C5, C6, C13, C14	10 µF	Charge pump fly capacitor 10 µF 100V X7S 1210	Murata	GRM32EC72A106KE05
C11, C12	1 µF	Input capacitor 1 µF 100V X7S 0805	Murata	GRM21BC72A105KE01
C7, C10	2.2 µF	VDD and EXT_VDD capacitors 2.2 µF 25V X5R 0402	Murata	GRM155R61E225ME15
C8, C9	2.2 µF	VX capacitor 2.2µF 50V X5R 06 03	Murata	GRM188R61H225ME11
C21, C22, C23, C24, C25, C26, C27, C28 [1]	10 µF	VOUT capacitor 10 µF 50V X5R 0805	Murata	GRM21BR61H106KE43
L1, L2	330 nH	VX inductor 330 nH 7.8A 8 MOHM SMD	Cyntec	HTEL25201B-R33MXR-01
D1	Diode	Zener single diode, 5.6V, SOD-523, 2 pins	ONSEMI	MM5Z5V6T1G
R3	10 kΩ	PGOOD pull-up resistor 10 kΩ 1% 1/10W 0603	Panasonic	ERJ-3EKF1002V
Q1 [2]	MOSFET	MOSFET P-CH 100V 37.1A TO252	Vishay	SUD50P10-43L-GE3
U1	PE25208	High voltage divide-by-2/3 charge pump	pSemi	PE25208A-R

Notes:
1. The minimum required VOUT capacitance is 47 µF. The maximum VOUT capacitance is 1 mF.
2. The Q1 external P-channel FET is optional.

Table 8. PE25208 Parallel Recommended Components

Reference	Value	Description	Manufacturer	Part Number
C101, C102, C103, C104, C105, C106, C201, C202, C203, C204, C205, C206, C13, C14	10 µF	Charge pump fly capacitor 10 µF 100V X7S 1210	Murata	GRM32EC72A106KE05
C111, C112, C211, C212	1 µF	Input capacitor 1 µF 100V X7S 0805	Murata	GRM21BC72A105KE01
C107, C110, C207, C210	2.2 µF	VDD and EXT_VDD capacitors 2.2 µF 25V X5R 0402	Murata	GRM155R61E225ME15
C108, C109, C208, C209	2.2 µF	VX capacitor 2.2µF 50V X5R 06 03	Murata	GRM188R61H225ME11
C121, C122, C123, C124, C221, C222, C223, C224 [1]	10 µF	VOUT capacitor 10 µF 50V X5R 0805	Murata	GRM21BR61H106KE43
L101, L102, L201, L202	330 nH	VX inductor 330 nH 7.8A 8 MOHM SMD	Cyntec	HTEL25201B-R33MXR-01
D1, D2	Diode	Zener single diode, 5.6V, SOD-523, 2 pins	ONSEMI	MM5Z5V6T1G
R3	10 kΩ	PGOOD pull-up resistor 10 kΩ 1% 1/10W 0603	Panasonic	ERJ-3EKF1002V
Q1 [2]	MOSFET	MOSFET P-CH 100V 37.1A TO252	Vishay	SUD50P10-43L-GE3
U1, U2	PE25208	High voltage divide-by-2/3 charge pump	pSemi	PE25208A-R

Notes:
1. The minimum required VOUT capacitance is 47 µF. The maximum VOUT capacitance is 1 mF.
2. The Q1 external P-channel FET is optional.

Recommended Layout

Figure 33 through Figure 36 show the layers of the recommended layout.

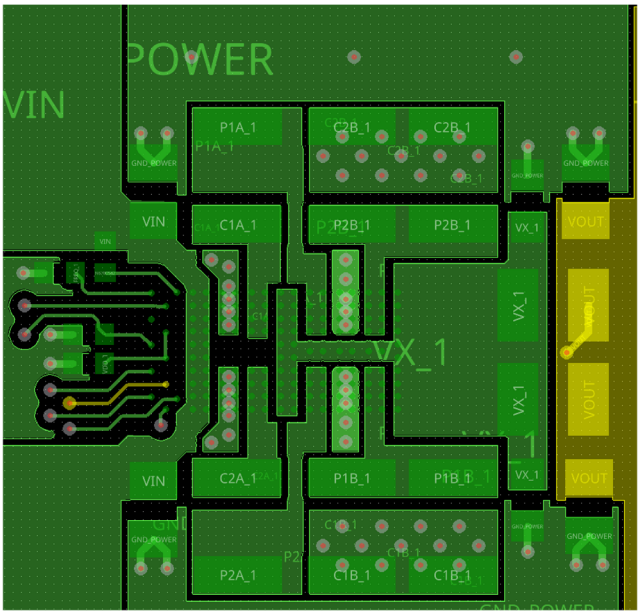


Figure 33. Top Layer (Power and Fan-out Routings)

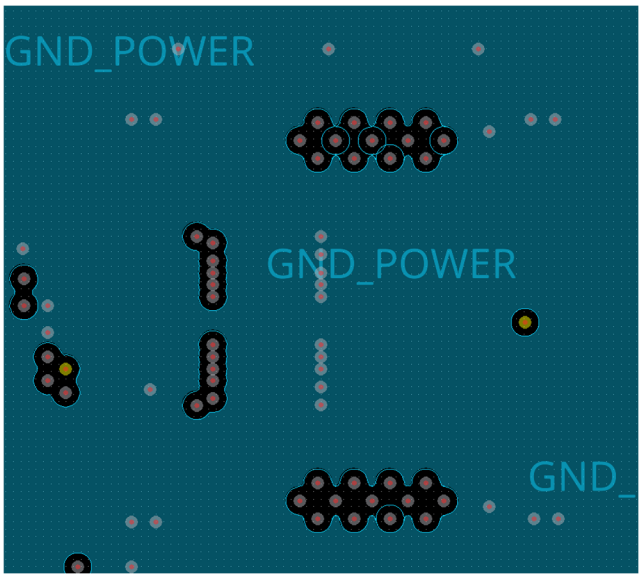


Figure 34. Inner Layer 1 (GND Layer)

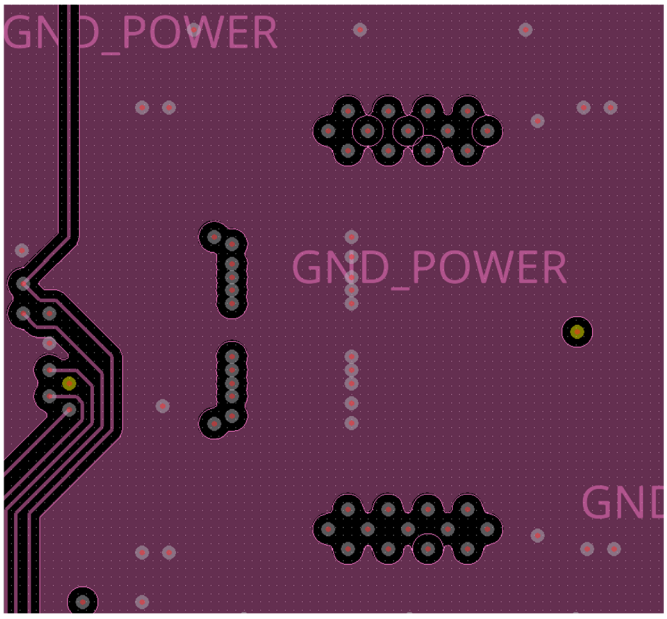


Figure 35. Inner Layer 2 (IO Routing)

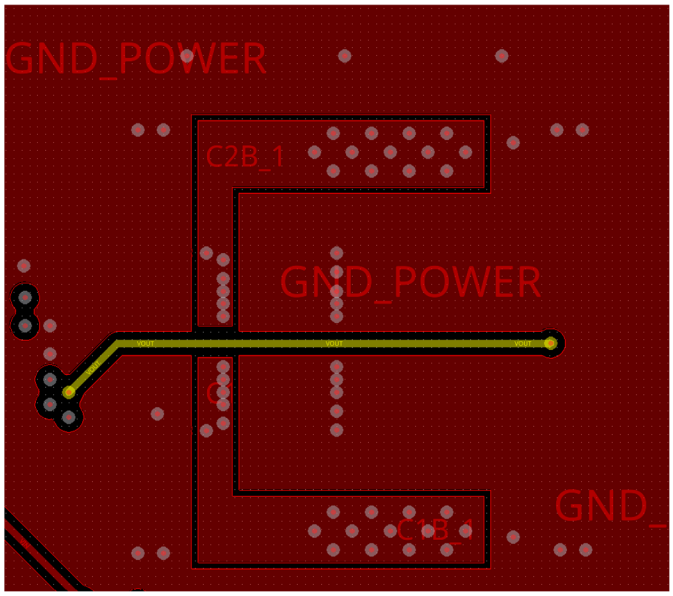


Figure 36. Bottom Layer (C1B and C2B routing and VOUT Sense)

Parallel Operation

As with standard inductive DC–DC converters, in a parallel design, a charge pump must ensure that both current and thermal loading is balanced. The PE25208 provides divided voltage of the input voltage at its output. The output voltage relates to the input voltage, and the output voltage is not regulated; therefore, the charge pump provides natural droop based on the equivalent output resistance (ROUT).

When the load is applied to the paralleled charge pumps, each output voltage of the modules starts to drop. The voltage drop from the ideal output voltage is decided by (ROUT + parasitic resistance) *IOUT. For the charge pumps to load-share effectively, pay attention to the layout to reduce the parasitic resistance of the output power tracks.

Figure 37 shows a layout example of two ICs in parallel configuration. Equal VOUT copper is used on the two ICs to achieve PCB balance.

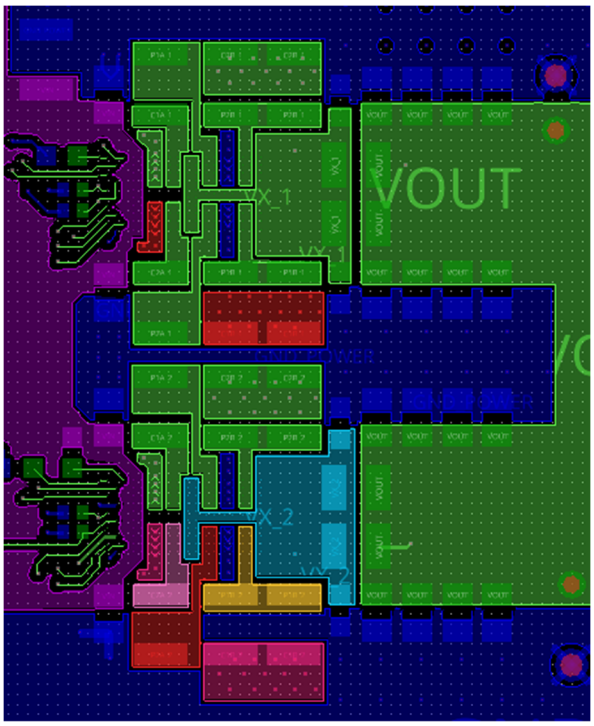


Figure 37. Layout Placement of Two ICs in Parallel Configuration

Component Selection

This section describes components required by the PE25208.

Input Capacitors

The input capacitors are connected between VIN and PGND and are used to reduce the ripple on VIN as the PE25208 switches. Place the input capacitors as close to the chip as possible to reduce any parasitic inductance effects. Because the PE25208 VIN pins extend from one side to the other side of the IC package, pSemi recommends separating the input capacitors by placing half of the capacitors on one side of the IC and the other half of the capacitors on the other side of the IC. Because the charge pump is not a regulator, ripple voltage on VIN can affect the output voltage.

The recommended effective capacitance used for Cin capacitors must have a typical value of 6 µF or higher for nominal voltages.

Flying Capacitors

The PE25208 requires two sets of flying capacitors: the “CB” and “CA” capacitors. The CB capacitors are connected between the C*B (C1B, C2B) and P*B (P1B, P2B) pins while the CA capacitors are connected between the C*A (C1A, C2A) and P*A (P1A, P2A) pins. Both the CA and CB capacitors are important components for efficiency and must be placed as close to the PE25208 as possible.

The steady-state voltage across the CB capacitors is 2* VOUT for divide-by-3 mode and 1* VOUT for divide-by-2. The steady-state voltage across the CA capacitors is 1* VOUT for both divide-by-3 and divide-by-2 modes. The capacitors must be chosen such that the component voltage rating is higher than the steady-state voltage to take ripples and spikes into account.

The capacitance value at the applied voltage across the capacitors has a direct impact on the maximum efficiency that can be achieved. The nominal capacitance value typically drops as the voltage across the capacitor increases, depending on the voltage coefficient of the selected capacitors.

The recommended effective capacitance for CB and CA capacitors must have typical values of CA = 7 µF and CB = 8 µF for nominal voltages. pSemi recommends that both CA and CB have similar effective capacitance under biased condition within your operating voltage range.

While selecting the capacitor values for maximum efficiency, the switching frequency must also be taken into consideration such that the self-resonant frequency (SRF) of the capacitors is higher than the maximum charge pump switching frequency.

At maximum power, the PE25208 could reach a junction temperature of up to 125 °C (at 85 °C ambient). This can heat the surroundings of the die and potentially the flying capacitors. The choice of the temperature rating of the capacitors is dependent on the temperature gradient across the board and the placement of the capacitors with respect to the die.

VX Capacitor

The VX capacitors are connected between VX and PGND. Place the VX capacitors as close to the IC as possible to reduce any parasitic inductance effects. Because the PE25208 VX pins extend from one side to the other side of the IC package, pSemi recommends separating the VX capacitors by placing one of the capacitors on one side of the IC and the other capacitor on the other side of the IC.

The Vx capacitor function is to reduce the voltage ripple at VX, but it can cause higher charge redistribution loss and reduction of efficiency. The value of the Vx capacitor must be optimized around those criteria.

The recommended effective capacitance used for Vx capacitors must have a typical value of 1 µF for nominal voltages.

Output Capacitor

The output capacitor reduces the ripple applied to the load at VOUT. The higher the capacitor value, the lower the ripple at VOUT. Increasing the output capacitor value increases the soft-start duration and might require multiple soft-start cycles to start-up. The minimum recommended VOUT effective capacitance is 14 µF for nominal voltages and the maximum VOUT capacitance is 1 mF.

Inductor Selection

The pSemi highly efficient charge pump products reduce the charge redistribution loss with patented “almost loss-less” architecture. This special architecture requires an inductor to achieve high-efficiency performance.

Inductors L1 and L2 are 330 nH inductors placed in parallel and must be placed as close as possible to the VX pin and theVX capacitors. The L1 and L2 inductors must have enough current rating to meet the output current requirement per application and a DCR resistance. All plots in this document are taken using the HTEL25201B-R33MXR-01 inductor. Efficiency results can differ with other inductors.

VDD Capacitor

The recommended effective capacitance used for VDD capacitor must have a typical value of 1 µF for 4.3V, which is the typical voltage of VDD.

The recommended effective capacitance values from this section are for the components used in Table 8. Contact pSemi for optimized value selection based on your application.

Packaging Information

This section provides the following packaging data:

- Moisture sensitivity level (MSL)
- Package drawing
- Package marking
- Tape-and-reel information

Underfill is required when mounting the PE25208 onto the PCB.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE25208 in the WLCSP package is MSL1 per the JEDEC standard J-STD-020E.

Package Drawing

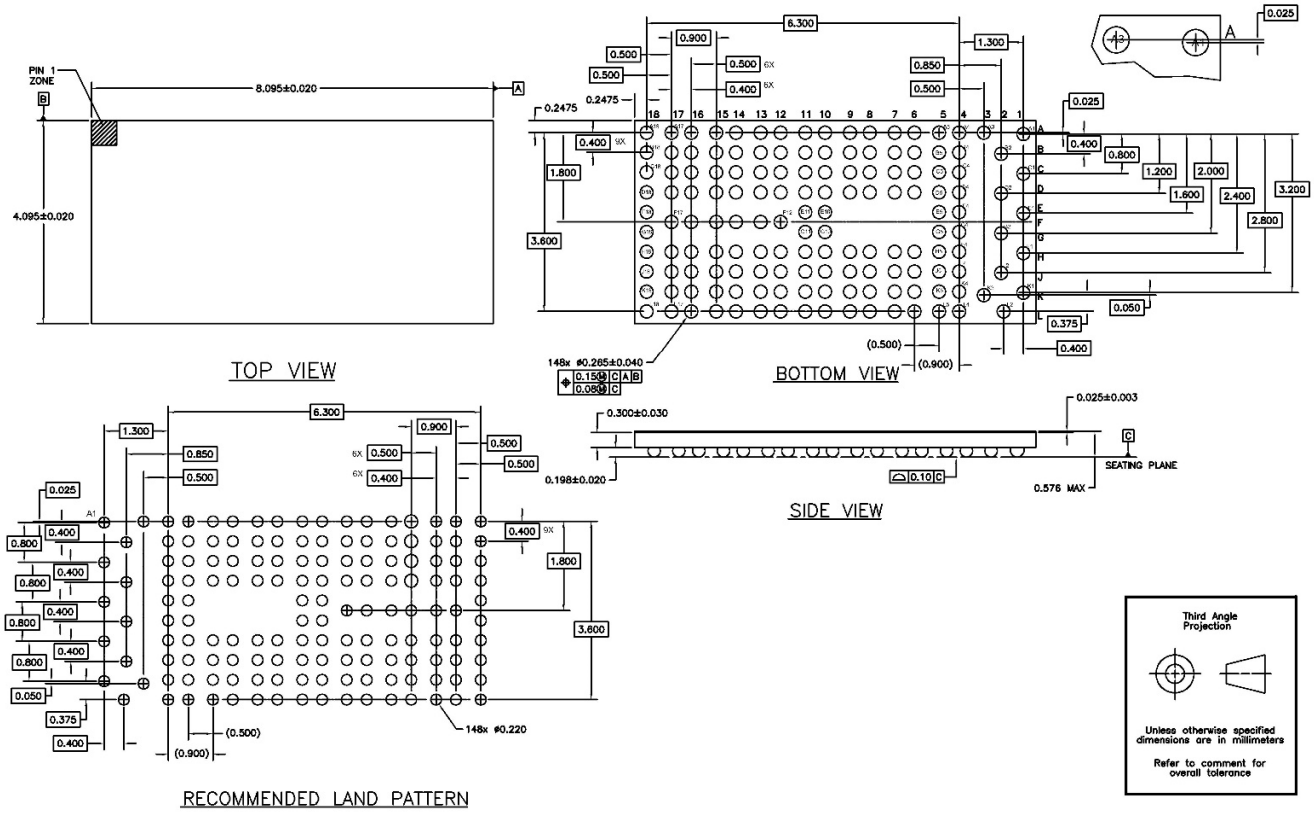
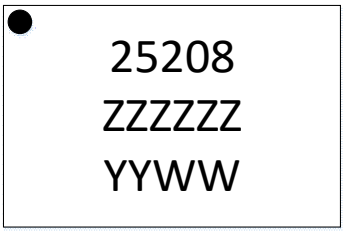


Figure 38. WLCSP Package Mechanical Drawing

Top-Marking Specification



● = Pin1 Indicator

25208 = Part Number

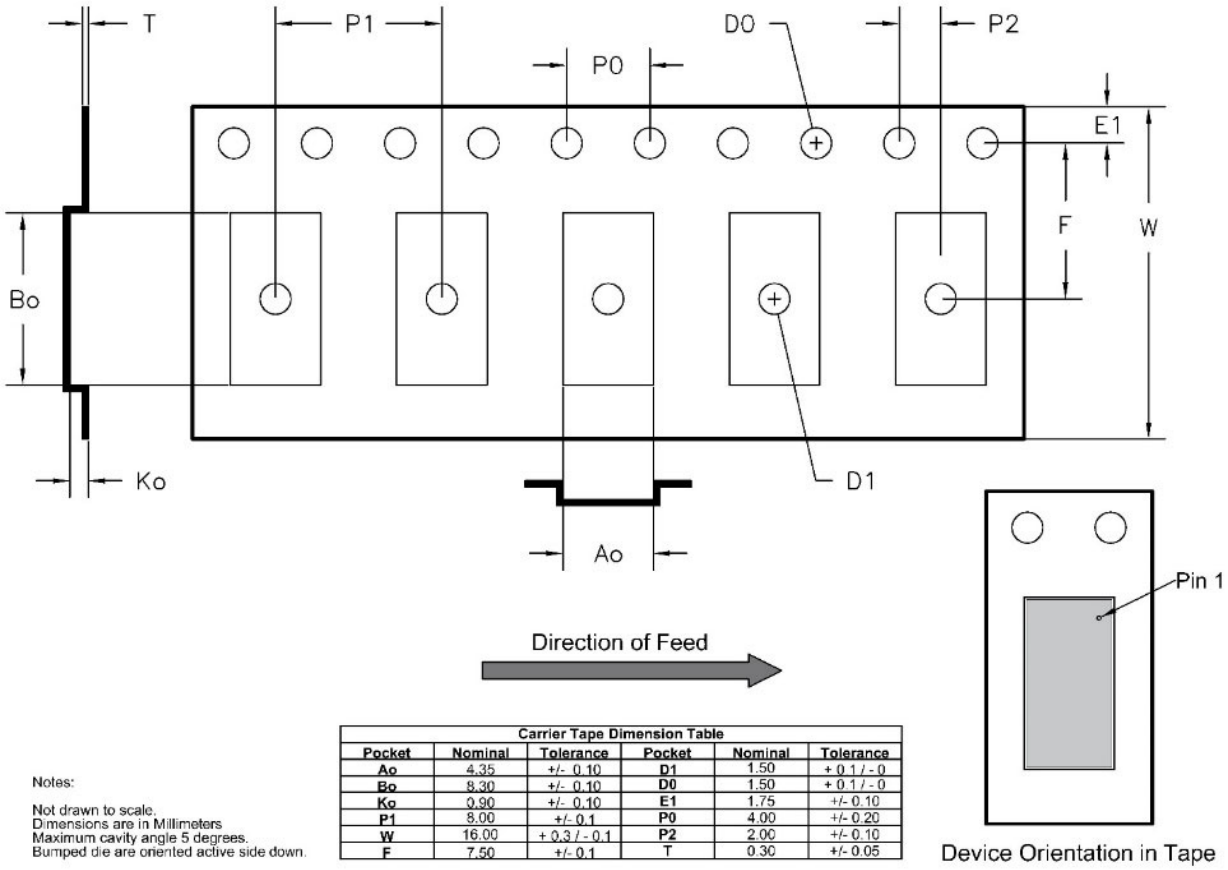
ZZZZZZ = Lot Number

YY = Last two digits of assembly year (2024 = 24)

WW = Assembly Work Week (01, 02, 03, …, 52)

Figure 39. WLCSP Package Marking Specifications

Tape and Reel Specification



Notes:

Not drawn to scale.
Dimensions are in Millimeters
Maximum cavity angle 5 degrees.
Bumped die are oriented active side down.

Carrier Tape Dimension Table

Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	4.35	+/- 0.10	D1	1.50	+ 0.1 / - 0
Bo	8.30	+/- 0.10	D0	1.50	+ 0.1 / - 0
Ko	0.90	+/- 0.10	E1	1.75	+/- 0.10
P1	8.00	+/- 0.1	P0	4.00	+/- 0.20
W	16.00	+ 0.3 / - 0.1	P2	2.00	+/- 0.10
F	7.50	+/- 0.1	T	0.30	+/- 0.05

Figure 40. WLCSP Tape and Reel Specifications

Ordering Information

Table 9 lists the PE25208 ordering codes and shipping methods.

Table 9. PE25208 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE25208A-R	8A Charge Pump Divide by 2 or 3	WLCSP	5000 Units/Tape and Reel
PE25208A-V (not for production use)	8A Charge Pump Divide by 2 or 3	WLCSP	250 Units/Tape and Reel

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark