PE25213

Document Category: Product Specification

Divide-by-2 and -3, 10A Charge Pump, Capacitor Divider

General Description

The PE25213 is an ultra-high efficiency charge pump that you can configure to divide down an input voltage by two or three and delivers up to 10A with peak efficiency up to 99%.

The PE25213 supports a 5.7V to 15V input voltage range in divide-by-2 mode and 8.4V to 15V in divide-by-3 mode. The PE25213 is primarily used as a front-end converter to convert a two- or three-cell battery input to a 1-1.5S output for downstream regulator to improve overall system efficiency and extend run time.

The PE25213 unique auto-switch mode changes the divide-down ratio during operation to avoid a downstream under-voltage lockout (UVLO) event at heavy system loading during a low-battery condition.

The PE25213 comes in a 4.545 mm × 2.715 mm 47-pin wafer-level chip scale package (WLCSP). The pinout is specially designed to be fully compatible with Type III PCB design.

Features

- Proprietary architecture enables industry leading efficiency with an ultra-low 1 mm profile solution.
- Wide input voltage range—from 5.7V to 15V—supports two- or three-cell mobile computers and 12V-bus point-of-load applications.
- Peak efficiency of 99%.
- Pin-selectable cycle skipping mode for improved light load efficiency.
- Dynamically configurable divide-by-2 or -3 modes under load.
- Low EMI fixed-frequency operation under heavy load conditions.
- Fully protected input under-voltage, output over-current and thermal shutdown.

Typical Applications

- Two-cell and three-cell lithium platforms
- Ultrabook and notebook computers
- Full-size tablet computers
- Ultra-thin form factor designs
- $12V_{IN}$ point-of-load designs in networking and telecommunications

Efficiency

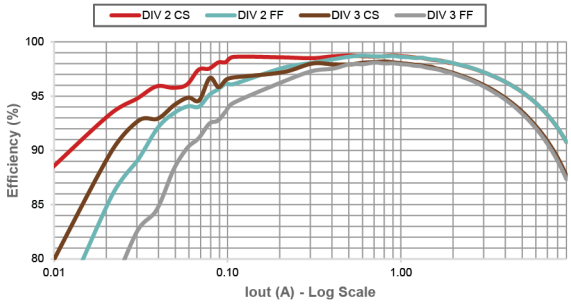


Figure 1. Typical Efficiency with V_{IN} = 7.4V in Divide-by-2 and V_{IN} = 11.4V in Divide-by-3, Fixed Frequency (FF), and Cycle Skip (CS) Modes

Simplified Application

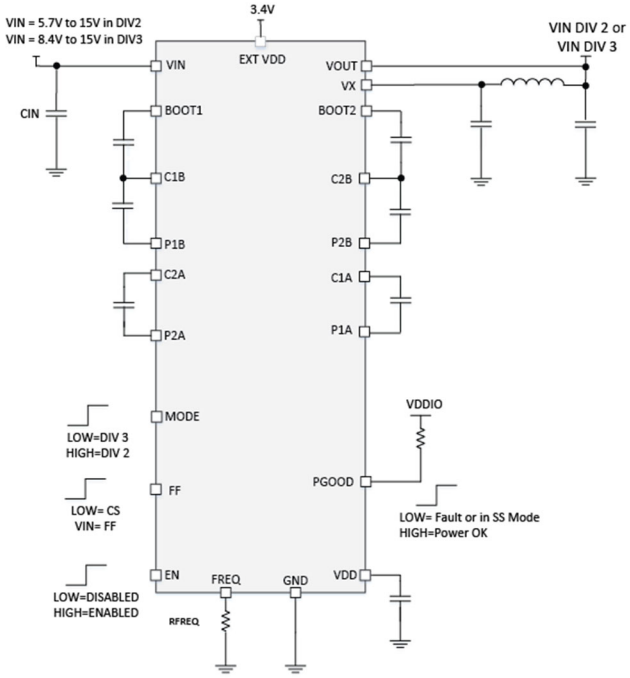


Figure 2. Application Schematic

Contents

Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the maximum operating range and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in Table 1.

Table 1. PE25213 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Input voltage, divide-by-3 mode	-0.3	30	V
Input voltage, divide-by-2 mode	-0.3	20	V
Output voltage V_{OUT}	-0.3	10	V
V_{DD} external	-0.3	10	V
Storage temperature	-65.0	150.0	°C
Junction temperature	-40.0	150.0	°C
Operating bump or lead temperature	–	260.0	°C
FREQ, FF	–	V_{DD} + 0.3	V
EN, MODE, PGOOD	-0.3	V_{IN} + 0.3	V
Human body model, all pins(1)	–	±2000	V
Charged device model, all pins(2)	–	±500	V

Notes:
1. Human Body Model, all pins (Joint JEDEC/ESDA Human Body Model (JS-001-2017)).
2. Charged Device Model, all pins (Joint JEDEC/ESDA Charged Device Model (JS-002-2018)).

Recommended Operating Conditions

Table 2 lists the PE25213 recommend operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2. PE25213 Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{IN} input voltage range, relative to GND, V_{IN}, in divide-by-3 mode	8.4	15	V
V_{IN} input voltage range, relative to GND, V_{IN}, in divide-by-2 mode	5.7	15	V
Junction temperature range, T_J	-40.0	125.0	°C

Package Thermal Characteristics

Table 3. Package Thermal Characteristics(*)

Parameter	Condition	Min	Max	Unit
Maximum junction temperature	Measured at max ambient temperature (T_A) and max power dissipation.	–	150.0	°C
Junction-to-case top thermal resistance (ΘJt)	JEDEC JESD51-12-01 and JESD15-3	4.8	–	°C/W
Junction-to-board thermal resistance (ΘJb)	JEDEC JESD51-12-01 and JESD15-3	4.3	–	°C/W
Junction-to-air thermal characterization (ΘJa)	–	24.5	–	°C/W

Note: * Package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-12. See also pSemi Application Note 57, *Thermal Characterization*.

Electrical Characteristics

Table 4 lists the PE25213 key electrical specifications at the following conditions, unless otherwise noted.

- V_{IN} = 5.7V to 15V, MODE = V_{IN}, T_J = -40 °C to +125 °C, FREQ = GND
- V_{IN} = 8.4V to 15V, MODE = GND, T_J = -40 °C to +125 °C, FREQ = GND

Table 4. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input voltage range						
Input voltage range	V_{IN}	MODE = Logic high (V_{OUT} = V_{IN}/2)	5.7	–	15	V
		MODE = Logic low (V_{OUT} = V_{IN}/3)	8.4	–	15	V
V_{IN} under-voltage lockout (UVLO) threshold high	V_{UVLO_H}	V_{IN} rising [MODE = Logic high (V_{OUT} = V_{IN}/2)]	–	–	5.69	V
		V_{IN} rising [MODE = Logic low (V_{OUT} = V_{IN}/3)]	–	–	8.39	V
Under-voltage lockout (UVLO) hysteresis	V_{UVLO_HYST}	–	–	150	–	mV
EXT V_{DD} input range	–	–	3.4	–	7.5	V
Transition from EXT V_{DD} to internal V_{DD} threshold	–	–	–	3.16	3.39	V
Output current						
Maximum output current	I_{LOAD}	DC continuous @ 25 °C	–	–	7	A
		Pulse width 100 ms at duty cycle 20% @ 25 °C	–	–	10	A
Output current limit	I_{LIMIT}	MODE = Logic high (V_{OUT} = V_{IN}/2)	10.1	12	–	A
		MODE = Logic high (V_{OUT} = V_{IN}/3)	8.9	12	–	
Supply current						
EXT V_{DD} supply current	–	EXT V_{DD} = 3.4V full load	–	175	–	µA
Shutdown supply current	–	EN = GND @ 25 °C	–	–	1	µA
Operating supply current	–	EXT V_{DD} = 3.465V, I_{LOAD} = 0A, FF = High (@ Max V_{IN} = 15V DIV3)	–	–	3.6	mA
Full-load switching frequency typical setting(1)	F_{SW}	Frequency range FREQ = 505 kΩ to 82.5 kΩ (1)	200	–	1000	kHz
		FREQ = 283 kΩ	–	260	–	kHz
		FREQ = GND	180	200	220	kHz
		FREQ = 82.5 kΩ	–	1000	–	kHz
Cycle skip frequency	F_{CS}	–	25	–	–	kHz
Nominal output voltage	V_{O_NOM}	MODE = Logic high	–	V_{IN}/2	–	V
		MODE = Logic low	–	V_{IN}/3	–	V
V_{OUT} under-voltage protection threshold	V_{UVP}	MODE = Logic high (V_{OUT} = V_{IN}/2)	0.7 × V_{IN}/2	0.8 × V_{IN}/2	0.9 × V_{IN}/2	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		MODE = Logic low (V_{OUT} = V_{IN}/3)	0.7 × V_{IN}/3	0.8 × V_{IN}/3	0.9 × V_{IN}/3	V
V_{OUT_UVP} glitch suppression	T_{UVP}	V_{OUT} must be less than V_{UVP} for longer than T_{UVP} to trigger fault	–	1.6	–	µs
Vx over-voltage protection	V_{XOVP}	–	9.5	11.5	13	V
Thermal shutdown threshold	T_{TSD}	–	140	160	–	°C
Thermal shutdown hysteresis	T_{TSD_HYST}	–	–	25	–	°C
Maximum soft start timeout duration	–	–	–	10	–	ms
Soft start input current limit	I_{SS_IIM}	V_{OUT} shorted to GND	–	2.5	–	A
Power good threshold	$PGOOD_{TH}$	Measured after SS completed without other faults.	–	–	95	% of V_{OUT}
Power good (PGOOD) pin						
Pull-down resistance	R_{PGOOD}	I_{SINK} = 15 mA	–	26	–	Ω
PGOOD rising threshold	–	–	–	1.3	–	V
PGOOD hysteresis	$PGOOD_{HYS}$	–	–	500	–	mV
Output leakage	–	V_{OUT} > $PGOOD_{TH}$	–		1	µA
Time for PGOOD detect	ProDirect	Time from falling edge of PGOOD to VOUT no longer able to support full load. No external capacitor on PGOOD.	–	10.0	–	µs
V_{DD} output voltage[2]	V_{DD}	See Note 2.	–	3.65	–	V
Logic levels EN, MODE, and FF						
Input high voltage	V_{IH}	EN and MODE	1.5	–	–	V
		FF	3.3	–	–	
Input low voltage	V_{IL}	–	–	–	0.4	V
EN pin input current	I_{EN}	EN = 15V	–	–	11	µA
MODE pin input current	I_{MODE}	MODE = 5.5V	–	–	3	µA
FF pin input current	I_{FF}	FF = 3.6V	–	–	1	µA

Notes:
1. Because the device is a dual-phase charge pump, each phase of the charge pump runs at 50% of the frequency set by the FREQ pin.
2. External loading of V_{DD} is only verified using Figure 41. Do not load V_{DD} externally.

Pin Configuration

This section provides the PE25213 pin configuration information. Figure 3 shows the PE25213 pin map for the 4.545 mm × 2.715 mm WLCSP. Table 6 lists the description for each pin.

Pin Configuration

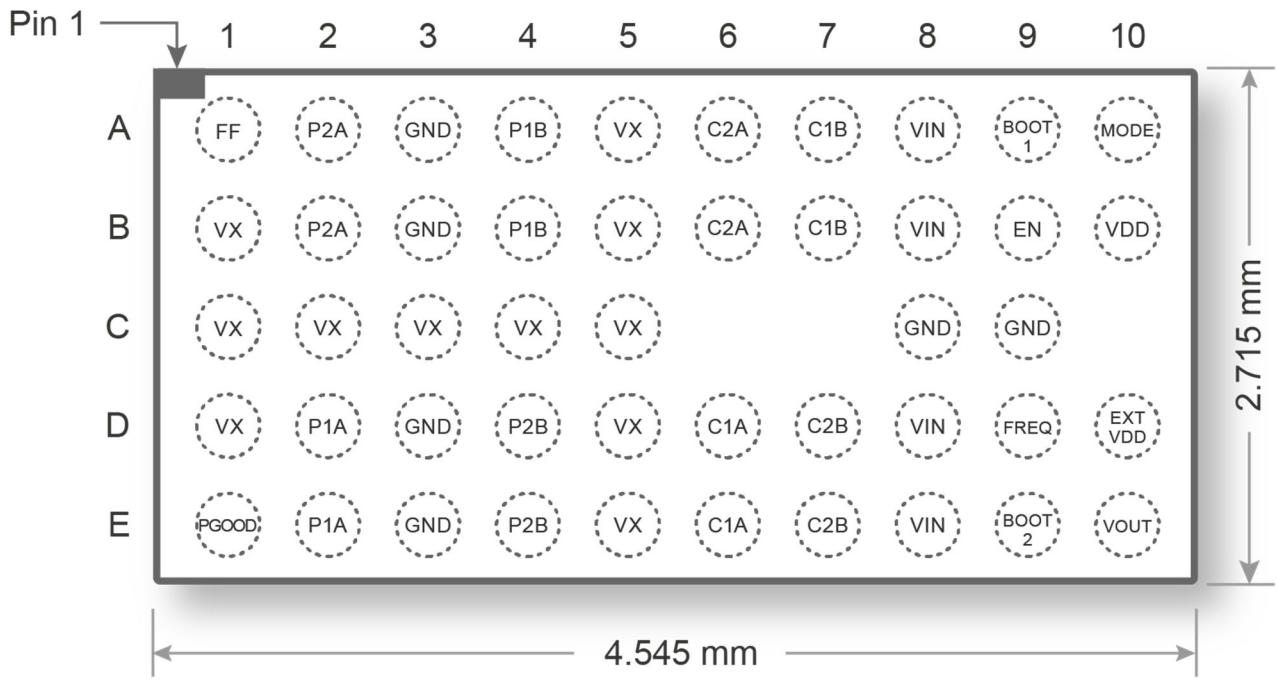


Figure 3. PE25213 Top View (Bumps Down)

Pin Descriptions

Table 5. Pin Descriptions

Pin number	Name	Description
A1	FF/CS	Selects the charge pump clock mode (logic high = fixed frequency, logic low = cycle skip). Read at IC power up. Value at this pin can be changed when EN = logic low.
A2, B2	P2A	Flying capacitor C2A phase node. Connect a fly capacitor between the C2A/P2A pins.
A3, B3, C8, C9, D3, E3	GND	Ground connection.
A4, B4	P1B	Flying capacitor C1B phase node. Connect a fly capacitor between the C1B/P1B pins.
A5, B1, B5, C1, C2, C3, C4, C5, D1, D5, E5	VX	Charge pump output switching node. Connect to an external inductor.
A6, B6	C2A	Flying capacitor C2A terminal. Connect a fly capacitor between the C2A/P2A pins.
A7, B7	C1B	Flying capacitor C1B terminal. Connect a fly capacitor between the C1B/P1B pins.
A8, B8, D8, E8	VIN	Input voltage.
A9	BOOT1	Bootstrap capacitor pin. Connect a 100-nF bootstrap capacitor between BOOT1 and C1B.
A10	MODE	Selects the charge pump voltage division ratio. Do not allow this pin to float. • MODE = Logic high or V_{IN} or 3.6V for divide-by-2 mode. • MODE = Logic low for divide-by-3 mode.
B9	EN	IC enable pin. Logic high enables the IC; logic low disables the IC.
B10	VDD	V_{DD} generated by the IC. Bypass with a 1 µF capacitor. Connect a capacitance to this pin even when powered by an external V_{DD}. Typically, 3V is generated on this pin.
D2, E2	P1A	Flying capacitor C1A phase node. Connect a fly capacitor between the C1A/P1A pins.
D4, E4	P2B	Flying capacitor C2B phase node. Connect a fly capacitor between the C2B/P2B pins.
D6, E6	C1A	Flying capacitor C1A terminal. Connect a fly capacitor between the C1A/P1A pins.
D7, E7	C2B	Flying capacitor C2B terminal. Connect a fly capacitor between the C2B/P2B pins.
D9	FREQ	Charge pump operating frequency select pin. The charge pump switching frequency switches at 50% of the operating frequency set by this pin. Setting this pin to GND sets the operating frequency to 200 kHz. For other frequency selection, see Setting the Operating Frequency on page 19.
D10	EXT VDD	External V_{DD} input pin. In this mode, the IC is powered from the external V_{DD} instead of the internally generated V_{DD} on B10. The PE25213 does not need this to be supplied to operate, but if externally applied, it can increase system efficiency. This pin can also be connected to the VOUT pin. If not used, connect it to ground.
E1	PGOOD	The open-drain power good (PGOOD) signal is enabled when V_{OUT} >95% of the division ratio and no other faults are present. Externally pull up with a 499 kΩ resistor. Lower resistor values can reduce system efficiency.
E9	BOOT2	Bootstrap capacitor pin. Connect a 100-nF bootstrap capacitor between BOOT2 and C2B.
E10	VOUT	Output voltage sense. Connect to the other side of the VX inductor.

Functional Block Diagram

The PE25213 uses proprietary charge pump technology to deliver superior efficiency in a fully integrated WLCSP.

The PE25213 provides the following protection features to ensure robust system operation:

- Input under-voltage lockout (UVLO)
- Thermal shutdown (TSD)
- Over-current protection (OCP)
- Output under-voltage protection (UVP)
- Output over-voltage protection (VX OVP)
- Soft-start timeout (SST)

Figure 4 shows the PE25213 functional block diagram.

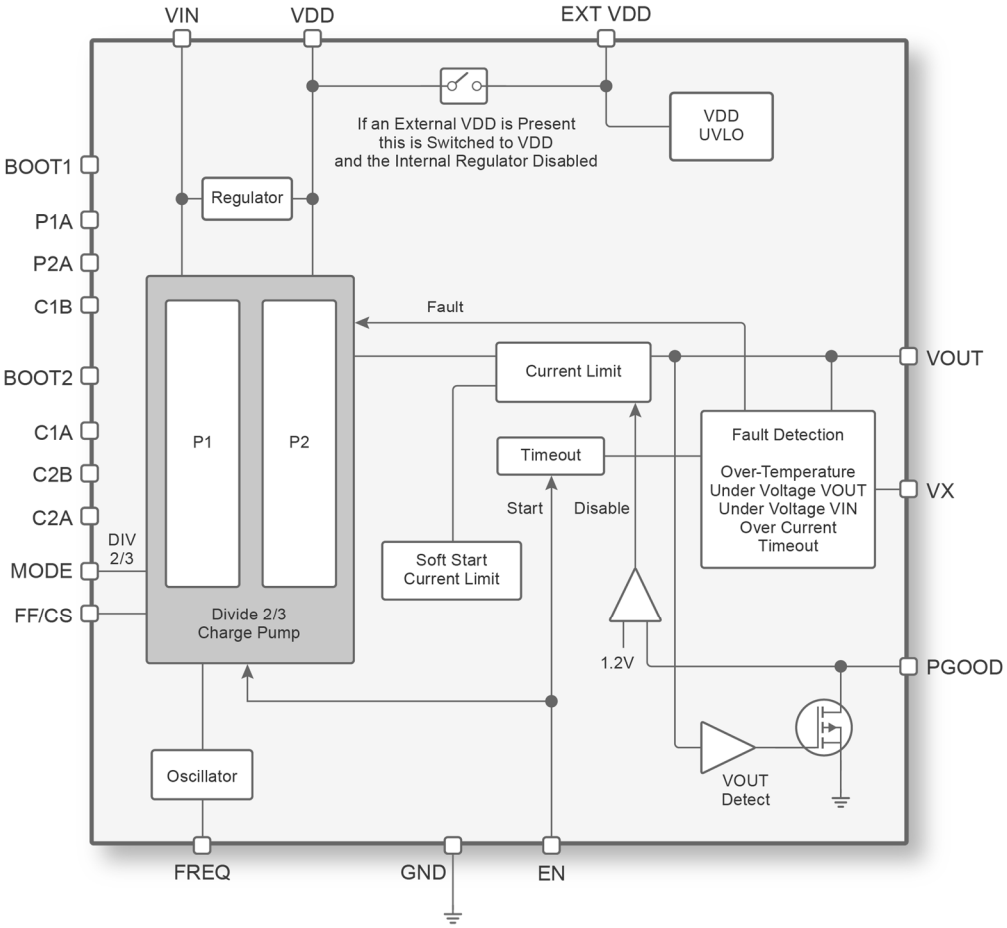


Figure 4. PE25213 Functional Diagram

Application Circuit

Figure 5 shows a typical application circuit configured to operate in divide-by-2 and divide-by-3 modes. For more details about component values, see the Application Information on page 28.

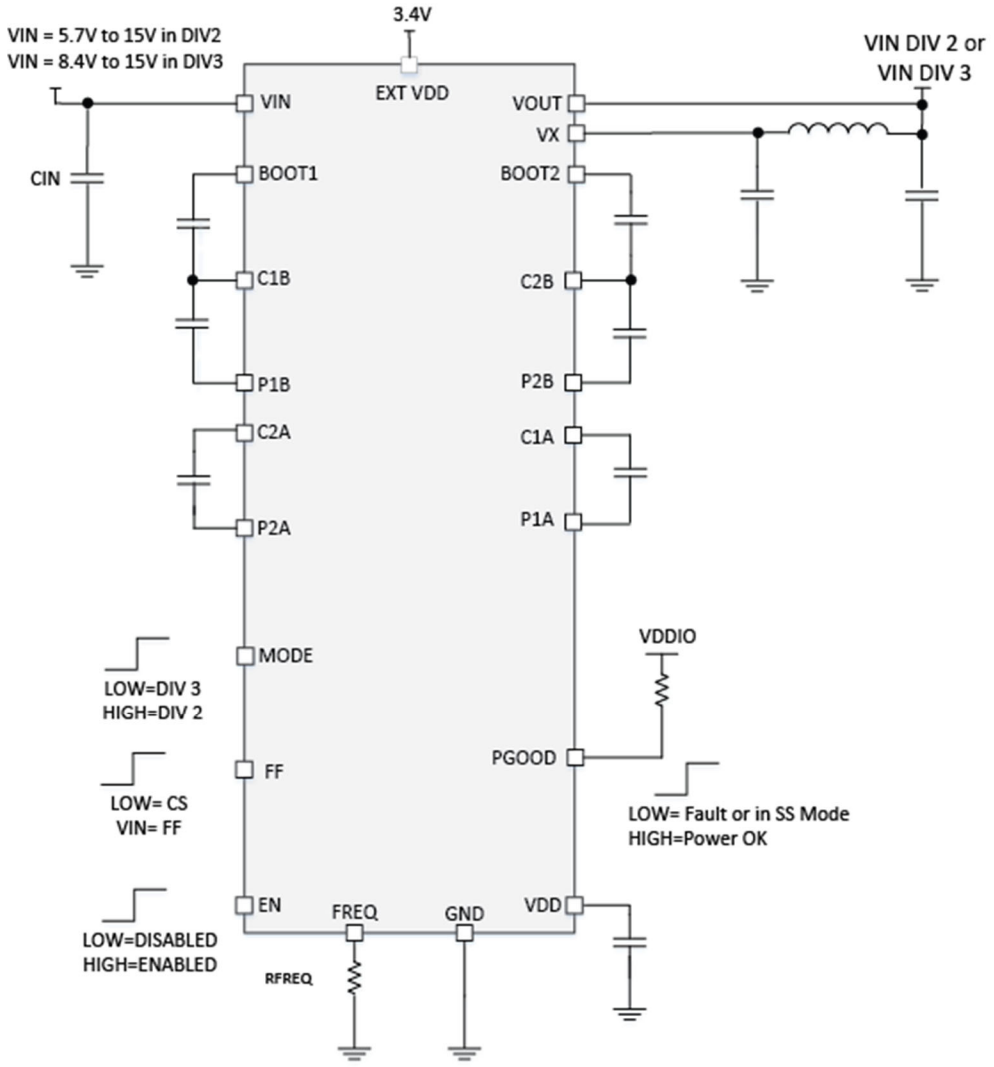


Figure 5. Simplified Application Circuit

Typical Performance Characteristics

Figure 6–Figure 31 show the PE25213 typical operating performance data.

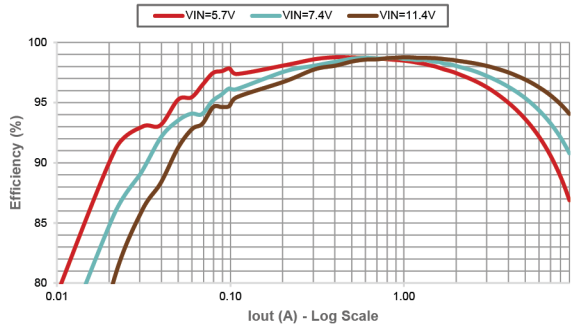


Figure 6. DIV 2, V_{IN} = 5.7, 7.4, 11.4V. Efficiency vs. Load Current, Fixed Frequency, 25°C, 260 kHz, Internal V_{DD}

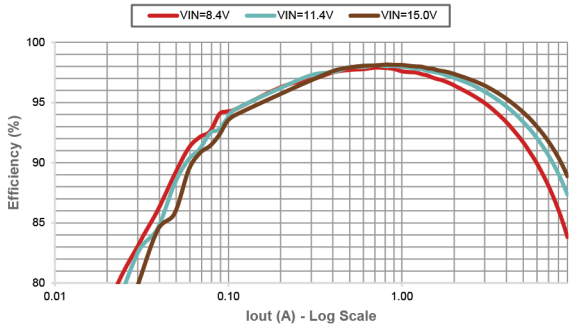


Figure 7. DIV 3, V_{IN} = 8.4, 11.4, 15V. Efficiency vs. Load Current, Fixed Frequency, 25°C, 260 kHz, Internal V_{DD}

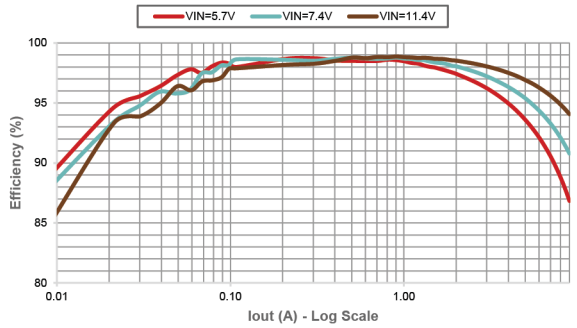


Figure 8. DIV 2, V_{IN} = 5.7, 7.4,11.4V. Efficiency vs. Load Current, Cycle Skip, 25°C, 260 kHz, Internal V_{DD}

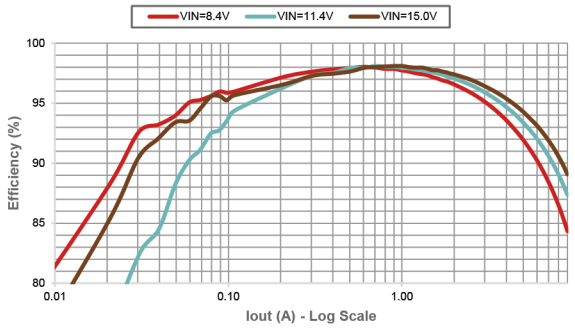


Figure 9. DIV 3, V_{IN} = 8.4, 11.4, 15V. Efficiency vs. Load Current, Cycle Skip, 25°C, 260 kHz, Internal V_{DD}

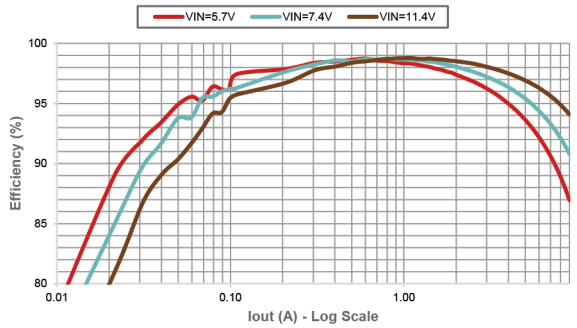


Figure 10. DIV 2, V_{IN} = 5.7, 7.4, 11.4V Efficiency vs. Load Current, Fixed Frequency, 25°C, 260 kHz, External V_{DD}

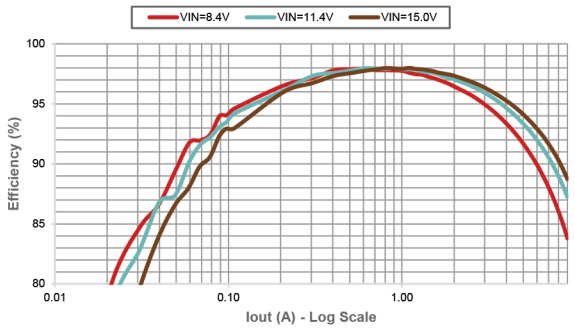


Figure 11. DIV 3, V_{IN} = 8.4, 11.4, 15V Efficiency vs. Load Current, Fixed Frequency, 25°C, 260 kHz, External V_{DD}

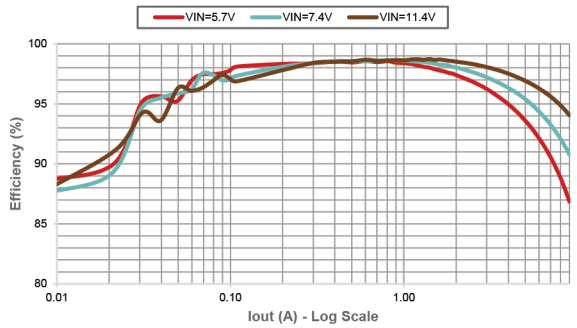


Figure 12. DIV 2, V_{IN} = 5.7, 7.4, 11.4V Efficiency vs. Load Current, Cycle Skip, 25°C, 260 kHz, External V_{DD}

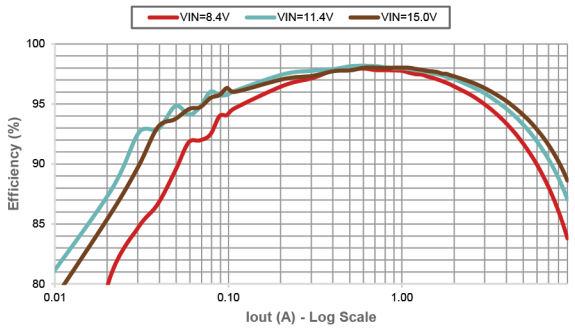


Figure 13. DIV 2, V_{IN} = 8.4, 11.4, 15V Efficiency vs. Load Current, Cycle Skip, 25°C, 260 kHz, External V_{DD}

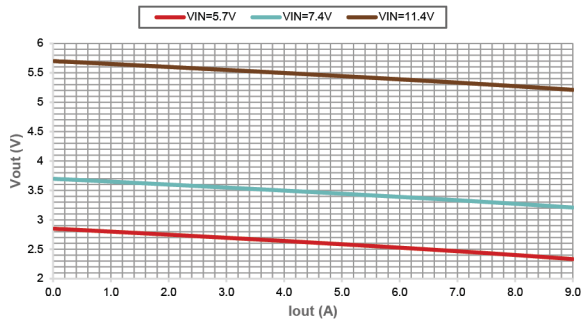


Figure 14. DIV 2, V_{OUT} vs. Load Current, Fixed Frequency, 25°C, 260 kHz, Internal V_{DD}

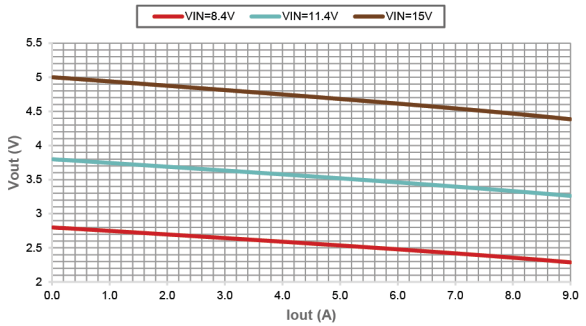


Figure 15. DIV 3, V_{OUT} vs. Load Current, 25°C, Fixed Frequency, 25°C, 260 kHz, Internal V_{DD}

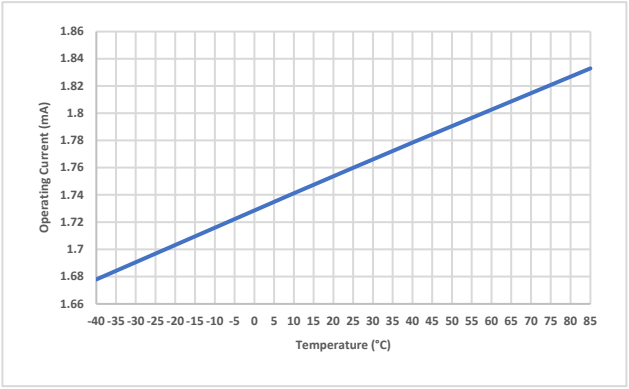


Figure 16. Operating Current vs. Temperature, DIV 2, V_{IN} = 7.4, Fixed Frequency, 260 kHz, Internal V_{DD}

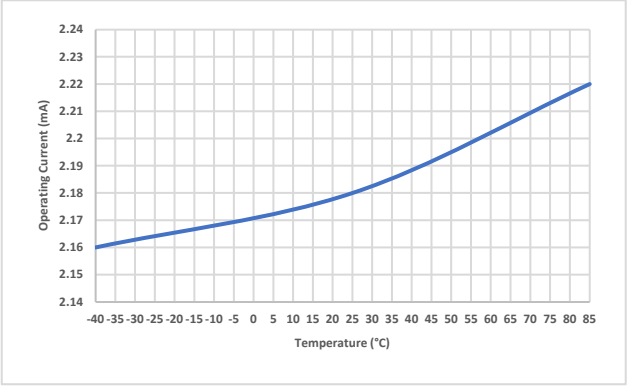


Figure 17. Operating Current vs. Temperature, DIV 3, V_{IN} = 11.4, Fixed Frequency, 260 kHz, Internal V_{DD}

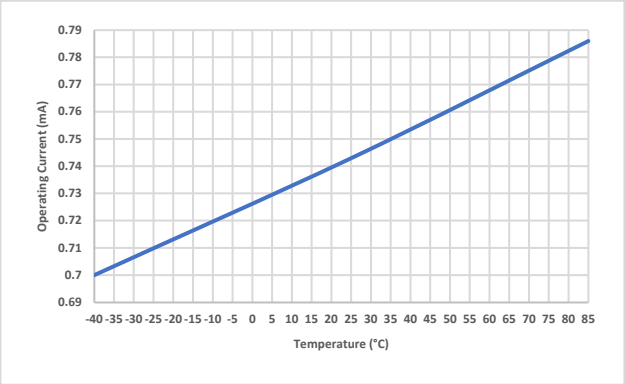


Figure 18. Operating Current vs. Temperature, DIV 2, V_{IN} = 7.4, Cycle Skip, 260 kHz, Internal V_{DD}

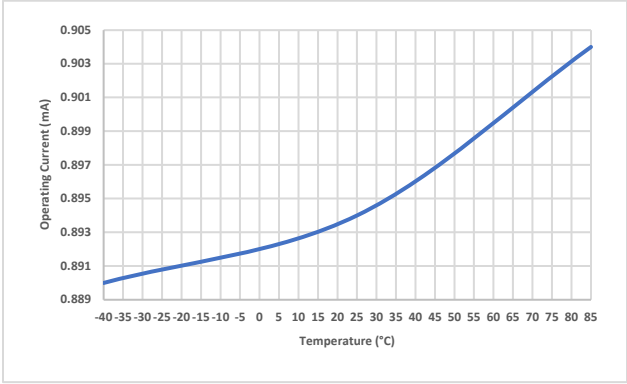


Figure 19. Operating Current vs. Temperature, DIV 3 V_{IN} = 11.4, Cycle Skip, 260 kHz, Internal V_{DD}

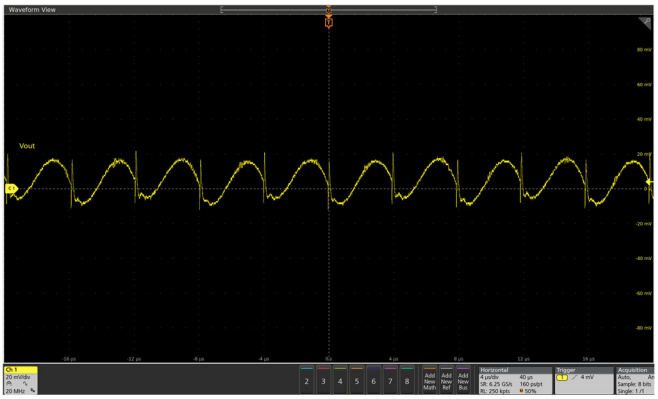


Figure 20. Divide-by-2 Ripple (@ I_{LOAD} = 7A), 7.4V

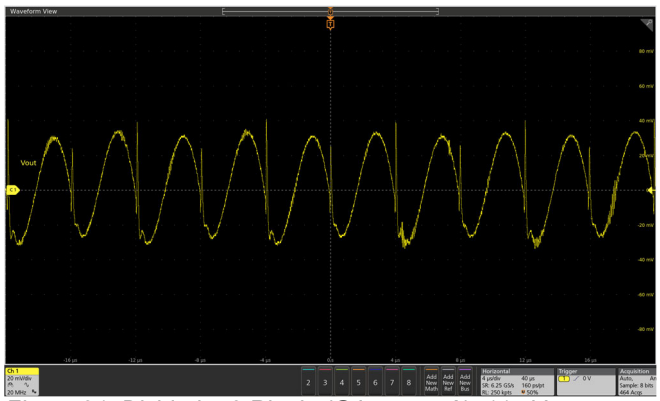


Figure 21. Divide-by-3 Ripple (@I_{LOAD} = 7A), 11.4V

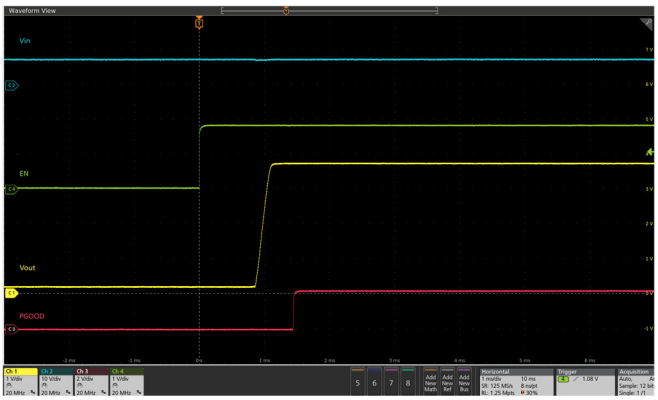


Figure 22. DIV2 Startup, C_{LOAD}=100 µF

Figure 23. DIV3 Startup, C_{LOAD}=100 µF

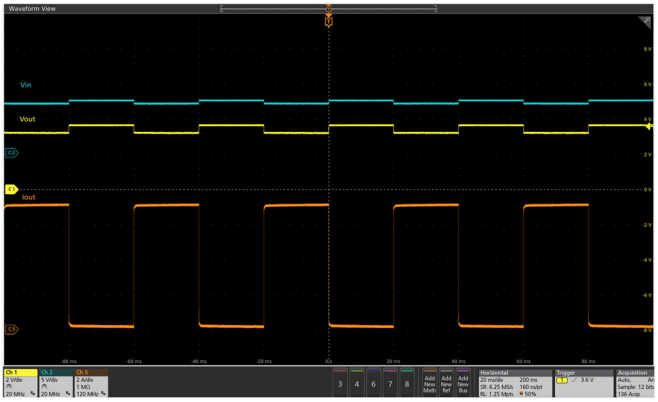


Figure 24. Load Transient (0.1A - 7A), V_{IN} = 7.4V, DIV2, C_{LOAD}=100 µF

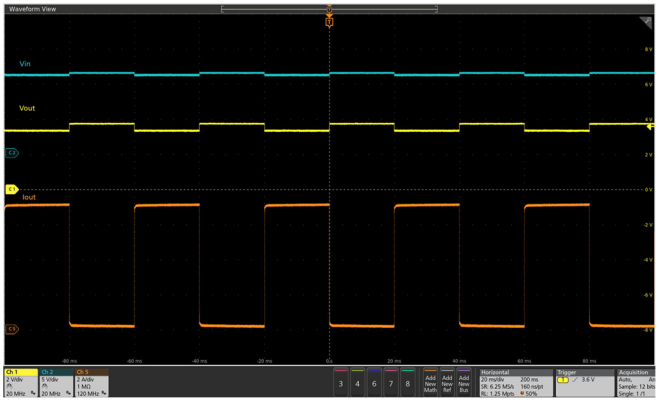


Figure 25. Load Transient (0.1A - 7A), V_{IN} = 11.4V, DIV3, C_{LOAD}=100 µF

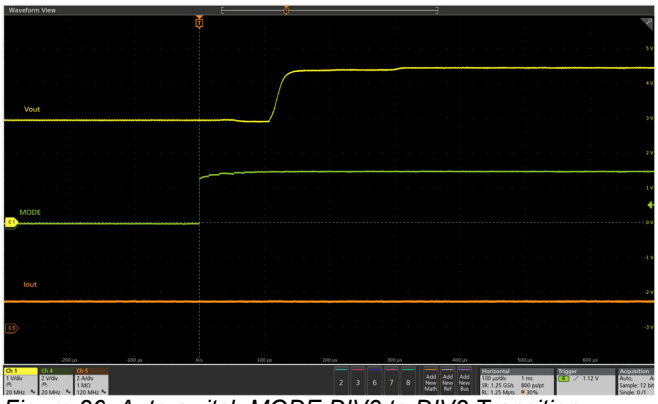


Figure 26. Auto-switch MODE DIV3 to DIV2 Transition, I_{OUT} = 1.5A

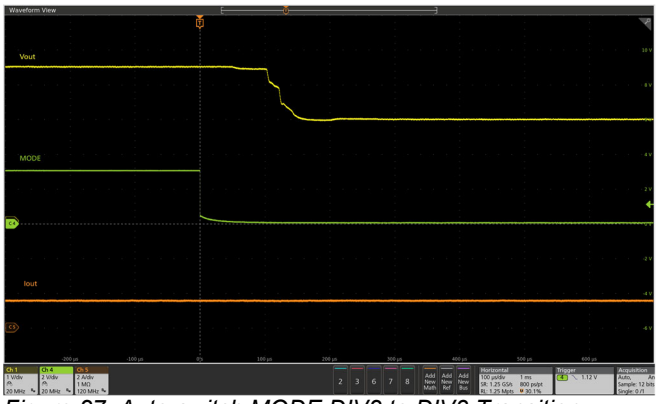


Figure 27. Auto-switch MODE DIV2 to DIV3 Transition, I_{OUT} =1.5A

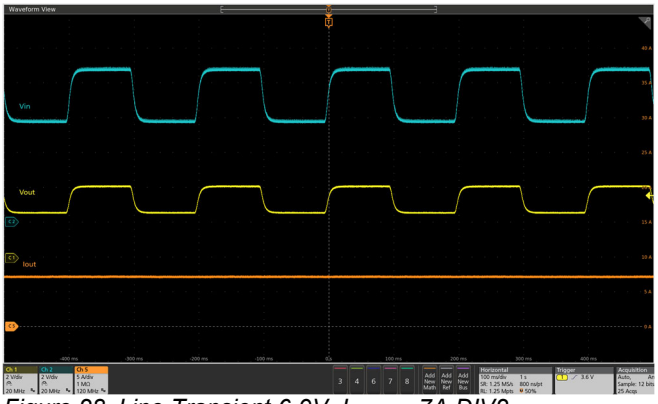


Figure 28. Line Transient 6-9V, I_{LOAD} = 7A DIV2, C_{LOAD}=100 µF

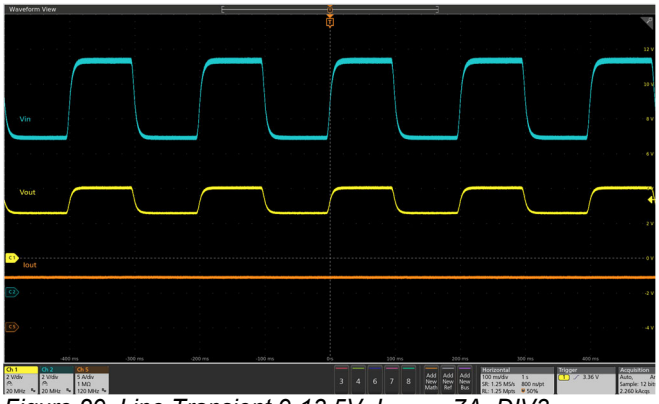


Figure 29. Line Transient 9-13.5V, I_{LOAD} = 7A, DIV3, CLOAD=100 µF

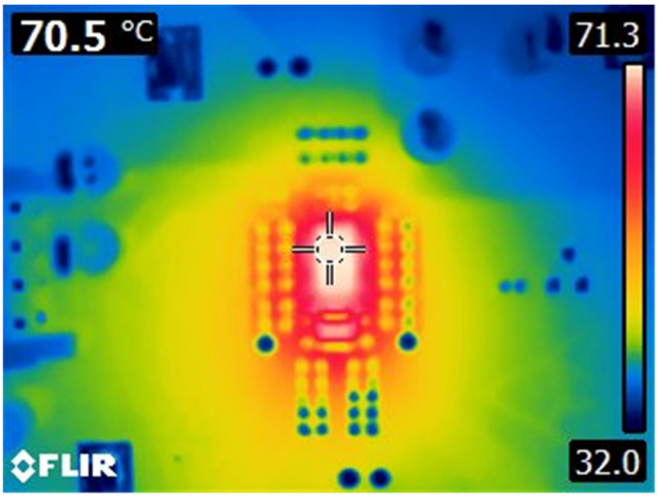


Figure 30. Thermal Plot Divide-by-2 I_{OUT}= 7A, (V_{IN} = 9V & V_{OUT} = 4.14V), P_{DISS} = 1.66 W, Top Case Temperature = 70.5 ˚C at TA = 25 ˚C

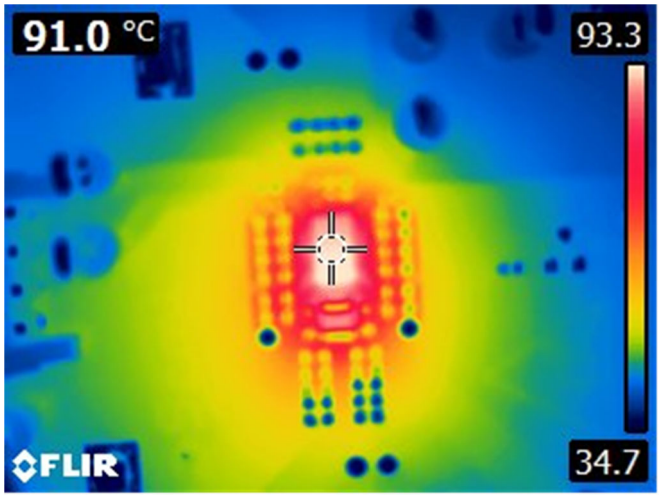


Figure 31. Thermal Plot Divide-by-3 I_{OUT}= 7A, (V_{IN} = 13.5V & V_{OUT} = 3.62V), P_{DISS} = 2.67W, Top Case Temperature = 91.0 ˚C at TA = 25 ˚C

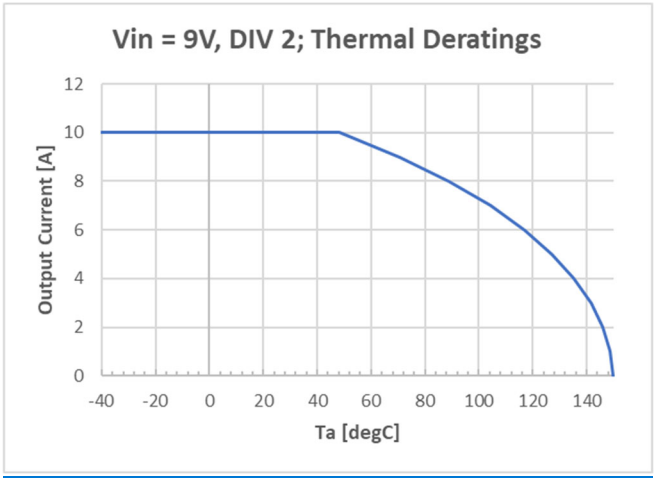


Figure 32. Thermal Deratings, (V_{IN} = 9V)

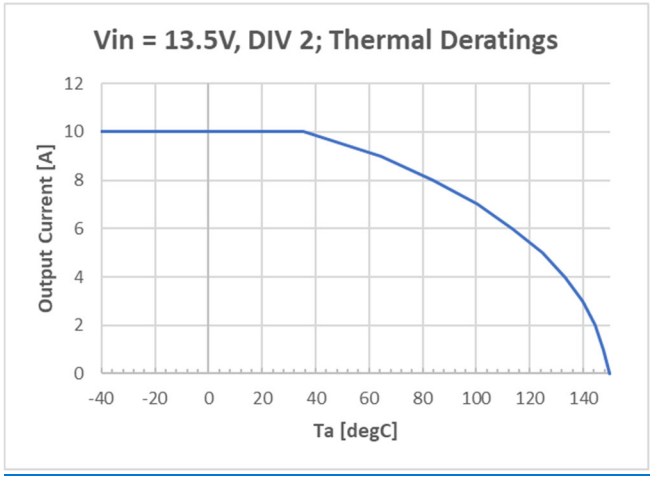


Figure 33. Thermal Deratings, (V_{IN} = 13.5V)

Detailed Description

The PE25213 is a dual-phase, charge pump-based, DC-DC converter that is designed to operate in either a fixed divide-by-2 or divide-by-3 mode. The supported output voltage range is from 2.85V to 7.5V with load currents of up to 10A and up to 75W delivered to the external load (require thermal solution when continuous load current >7A). You can configure the charge pump to operate over a range of frequencies using the FREQ pin to allow easier optimization of EMI vs. efficiency for the target application.

Voltage Division and MODE Pin

The device configuration is set by connecting the MODE pin to a voltage greater than 1.2V or less than 0.4V. This pin can be driven dynamically to change between divide-by-2 and divide-by-3 mode.

If the ability to change MODE is not required, connect it to ground for divide-by-3 mode or a voltage higher than 1.2V for divide-by-2 mode. To minimize quiescent current, connect MODE to VIN in divide-by-2 mode.

The MODE pin can be driven dynamically to change division ratios. For the limitations when in this mode, see Driving the Voltage Division Pin Dynamically on page 17.

Table 6. MODE Pin

Mode pin	Division ratio
<0.4V	Divide-by-3
>1.2V	Divide-by-2

Drive the MODE low or high. By default, this pin is pulled down with an internal resistor.

The PE25213 implements all the power switches and switch control to operate in divide-by-2 or divide-by-3 mode. The same PCB design can support either mode. If only operating in a divide-by-2 mode, you can achieve small efficiency improvements if you short the C1B/C2A and the C2B/C1A pins to each other at the PCB level.

These shorts operate in parallel with internal power switches in the PE25213, decreasing switch impedance and slightly reducing losses as a result. The C1B/C2A and C2B/C1A pins are placed adjacent to each other on the chip pin-out to make this board level connection easier for divide-by-2-only applications.

Driving the Voltage Division Pin Dynamically

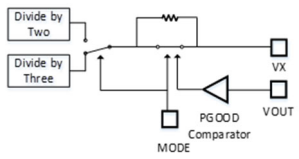
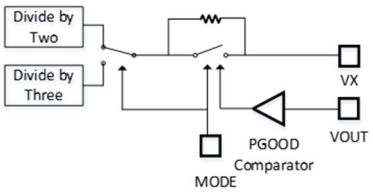
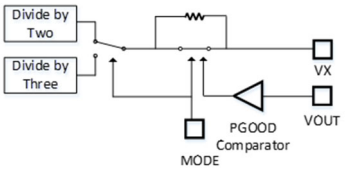
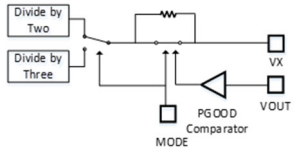
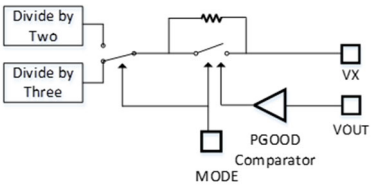
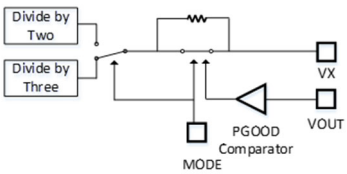
The MODE pin can be driven during operation to change the division ratio. This can be useful to extend the operating life of an application with a battery stack of three-cells. As the input voltage decays, the device can be switched from divide-by-3 mode to divide-by-2 mode. As the cell stack charges, the device can be switched from divide-by-2 mode to divide-by-3 mode.

- To change from divide-by-3 mode to divide-by-2 mode, switch the MODE pin from logic low to logic high.
- To change from divide-by-2 mode to divide-by-3 mode, switch the MODE pin from logic high to logic low.

Before the transition, the device operates normally in divide-by-2 or divide-by-3 MODE, depending on the logic level on the MODE pin. In this state, the PE25213 can supply up to 10A output current.

During the transition, the charge pump switches to a fixed frequency of 200 kHz per phase, and the FETs in the charge pump are driven in a higher impedance mode. In the Table 7 diagrams, this is represented by an output resistor.

Table 7. Operation Stages During Dynamic Changeover

Transition	Before transition	During transition	After transition
Divide-by-3 to Divide-by-2			
Divide-by-2 to Divide-by-3			

When the charge pump frequency is switched to the fixed frequency of 100 kHz, the MODE pin change is delayed for a period of about 50 µs. Depending on the load on the output during this time, a small dip in output voltage could be seen before the output starts to transition.

When the output is transitioning, the device supplies both the current to charge the output capacitor and the current to supply the downstream load. Because of this, the rate of rise and decline of the output voltage are dependent on the downstream load and output capacitance.

If the PE25213 is held in the transition region for a prolonged time at high load currents, it could reach the over-temperature threshold and switch off in a fault mode. During the transition, limit the maximum load to 1.5A.

When changing from divide-by-2 to divide-by-3 mode, the only discharge path available from the output capacitor is through the load as a passive discharge. If the output is not loaded, during the transition from divide-by-2 to divide-by-3 mode, the charge pump switches to the lowest switch frequency setting and waits for the output to gradually discharge.

Over-temperature Detection and Behavior

If the PE25213 enters over-temperature, it switches off as it cools down below the over-temperature threshold and then restarts.

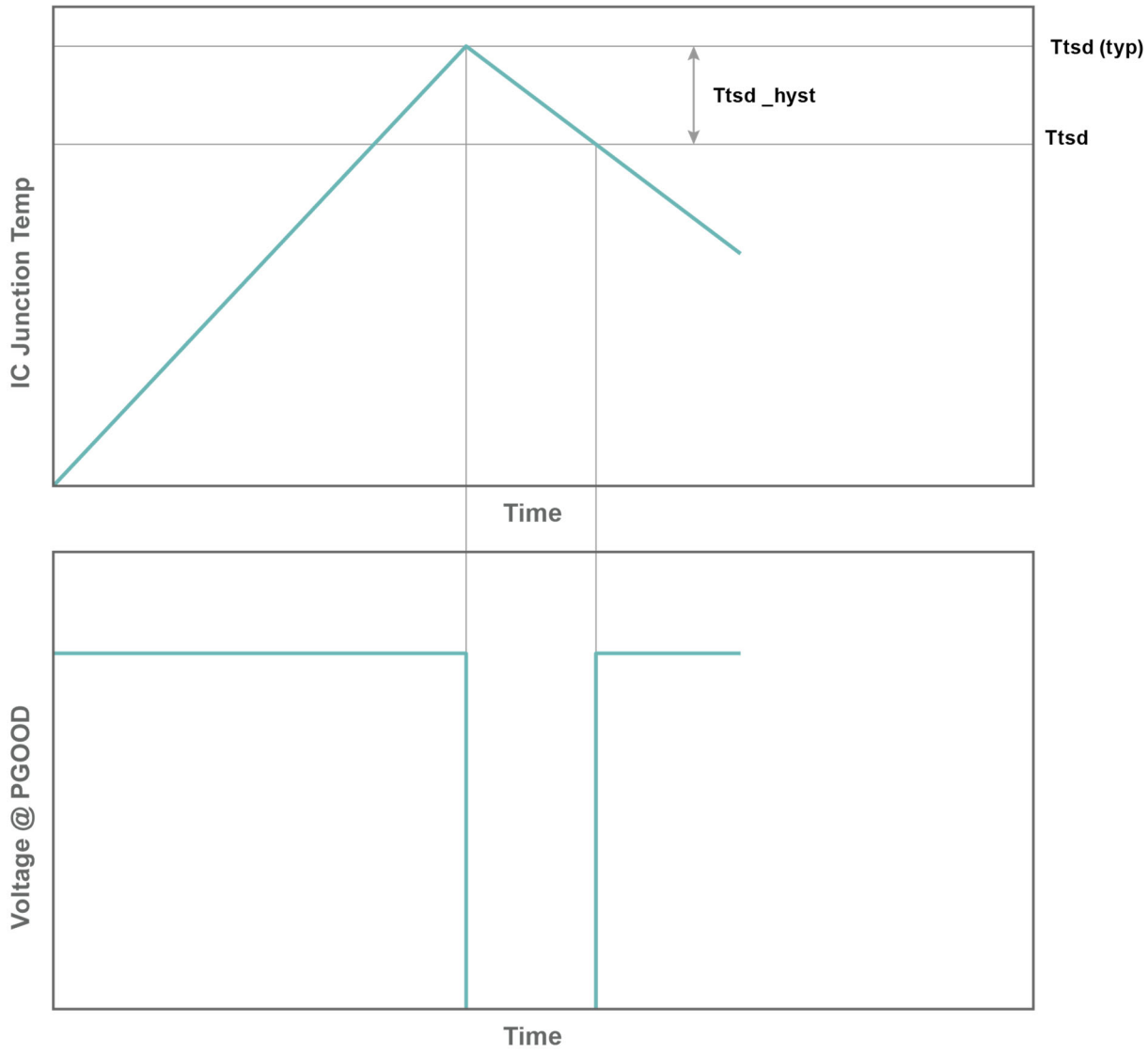


Figure 34. Over-temperature Behavior

Setting the Operating Frequency

Use the FREQ pin to set the operating frequency of the PE25213. To save a resistor, connect the FREQ pin to GND to oscillate at a nominal 200 kHz. This is the frequency of oscillation at the VX pin and the charge pump frequency per phase switches at 50% of this value.

To adjust the frequency, connect a 82.5 KΩ to 505 KΩ resistor between the FREQ pin and GND. Figure 35 shows the VX switching period versus the resistance value set at the FREQ pin.

Use the following equation to find the required VX switching period in µs:

$$VX\ switching\ period = (0.0093 * resistance\ value\ in\ \mathrm{K\Omega}) + 0.2254$$

Using a resistor value of 505 KΩ in the equation above:

$$VX\ switching\ period = (0.0093 * 505) + 0.2254 = 4.92\ \mu s\ (203\ kHz)$$

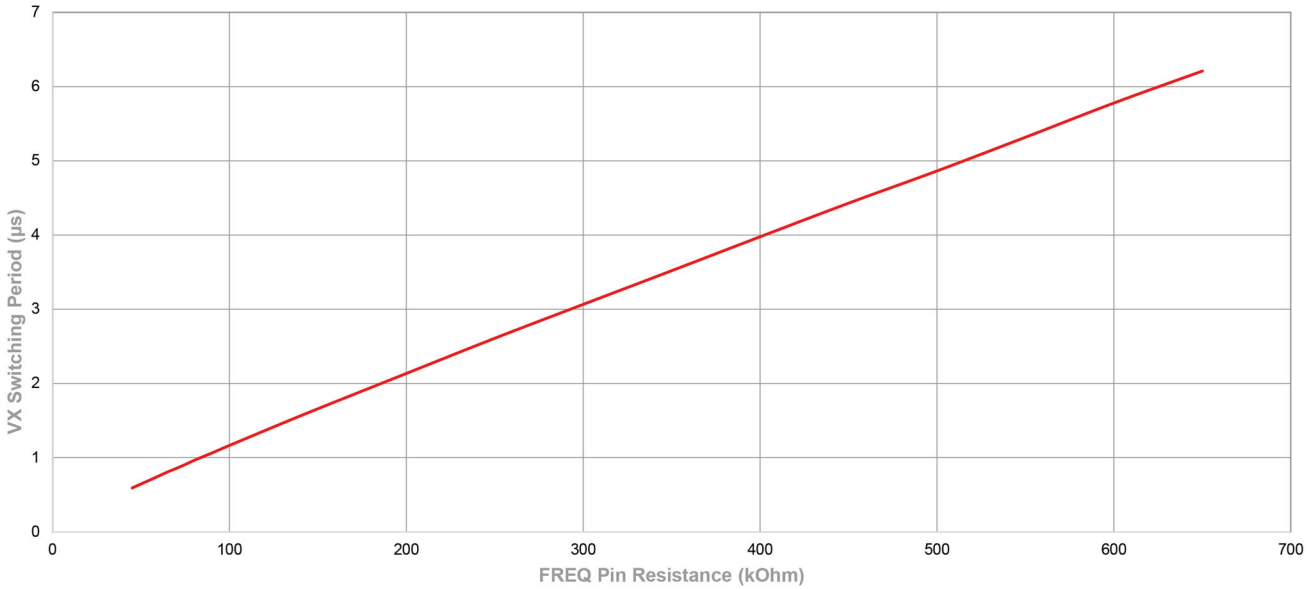


Figure 35. Switching Frequency vs. Resistance on the FREQ Pin

Startup – EN, VIN, and VDD Relationship

The PE25213 enable input pin (EN) was designed to be compatible with typical low voltage digital I/O levels so that an external controller can easily drive it. If external power sequencing or control is not required, EN can also be connected to the VIN pin.

If the EN pin is held low until VIN reaches its nominal voltage, PE25213 follows the initialization sequence in Figure 36.

An internally regulated supply voltage (VDD) is nominally set around 3.6V and is derived from VIN or external VDD, if it is present.

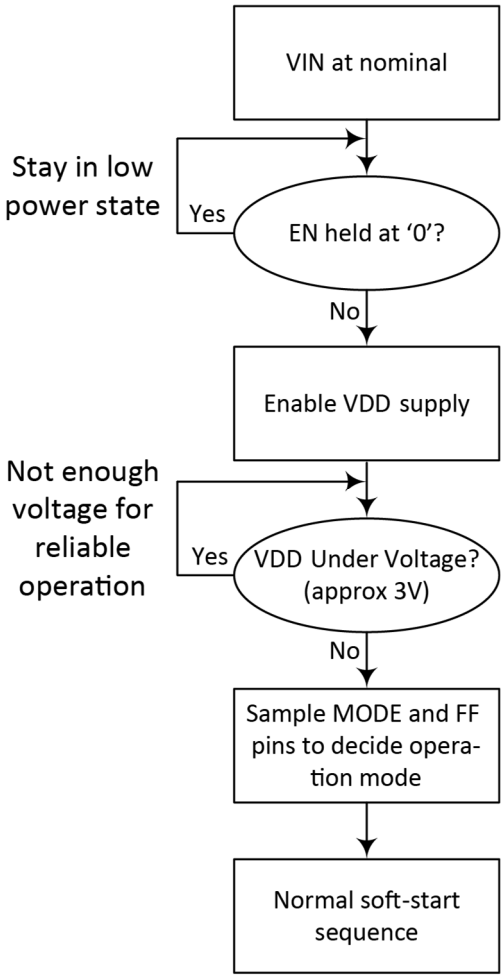


Figure 36. EN-controlled Startup Flow

During the initial startup and soft start sequence, the state of the MODE pin is initially sampled, and any changes are ignored until the device is in normal operation and the PGOOD pin is high.

Soft Start

In soft start, the PE25213 charge pump operates in a high resistance mode to ensure that the PE25213 exits the soft-start phase and transitions to full power switching mode when the VOUT voltage has reached 95% of the target voltage. The PGOOD pin tri-states, and the external resistor pulls PGOOD high at the same time, assuming that no other faults are present. Use the PGOOD pin as a power sequencing signal to enable the downstream converters connected to the PE25213 output.

Applying a load equal to or higher than the soft-start current (I_{SS_IIM}) during soft start can cause failure during startup or prolong the startup duration.

If a fault situation in which VOUT is shorted occurs, after the timeout period the PE25213 enters a cooldown period before it attempts to restart.

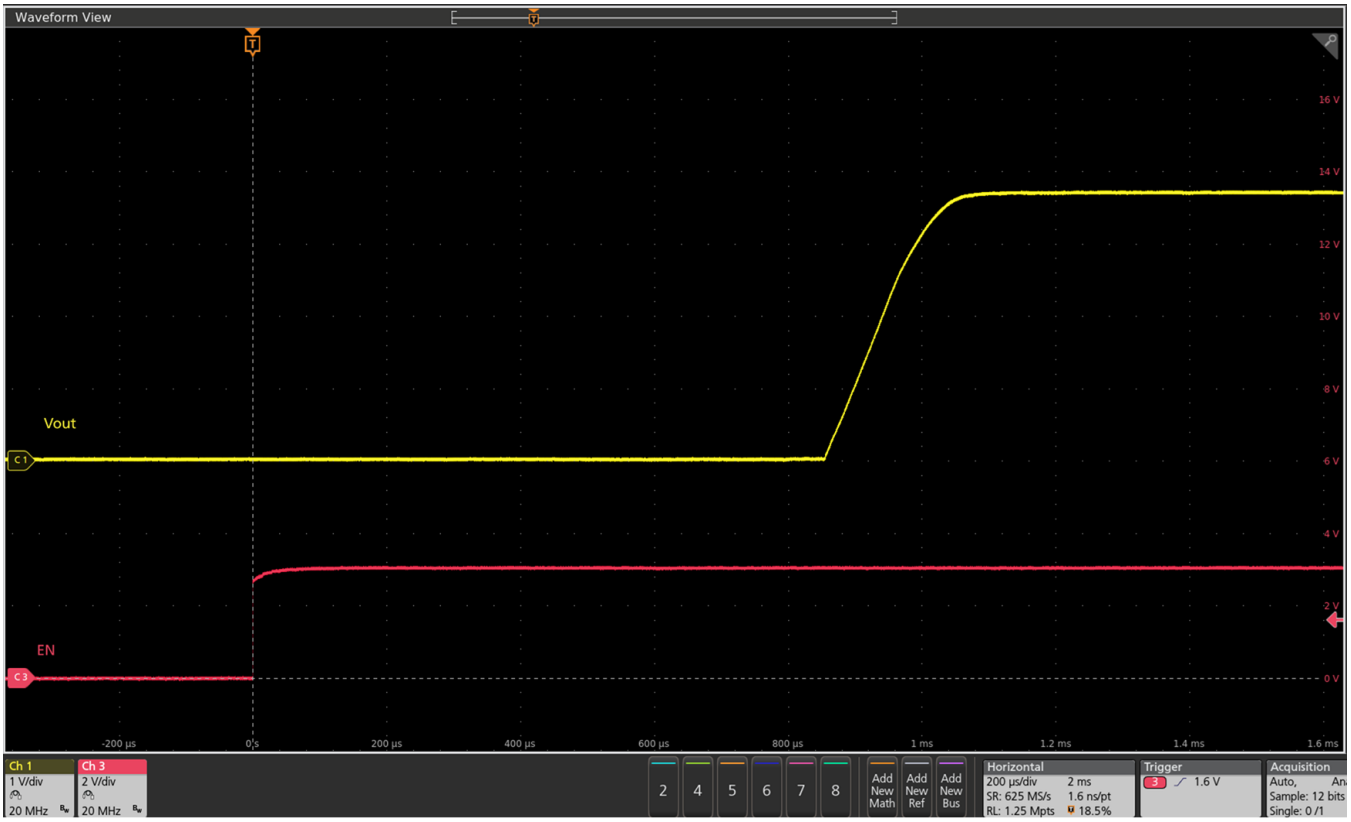


Figure 37. Soft-start Waveform into a Discharged Output Voltage

Figure 37 shows how the PE25213 exits the soft-start mode and enters full power. Throughout the soft start, the PE25213 operates the charge pump in a fixed-frequency mode of 260 kHz, no matter how the FREQ pin is configured.

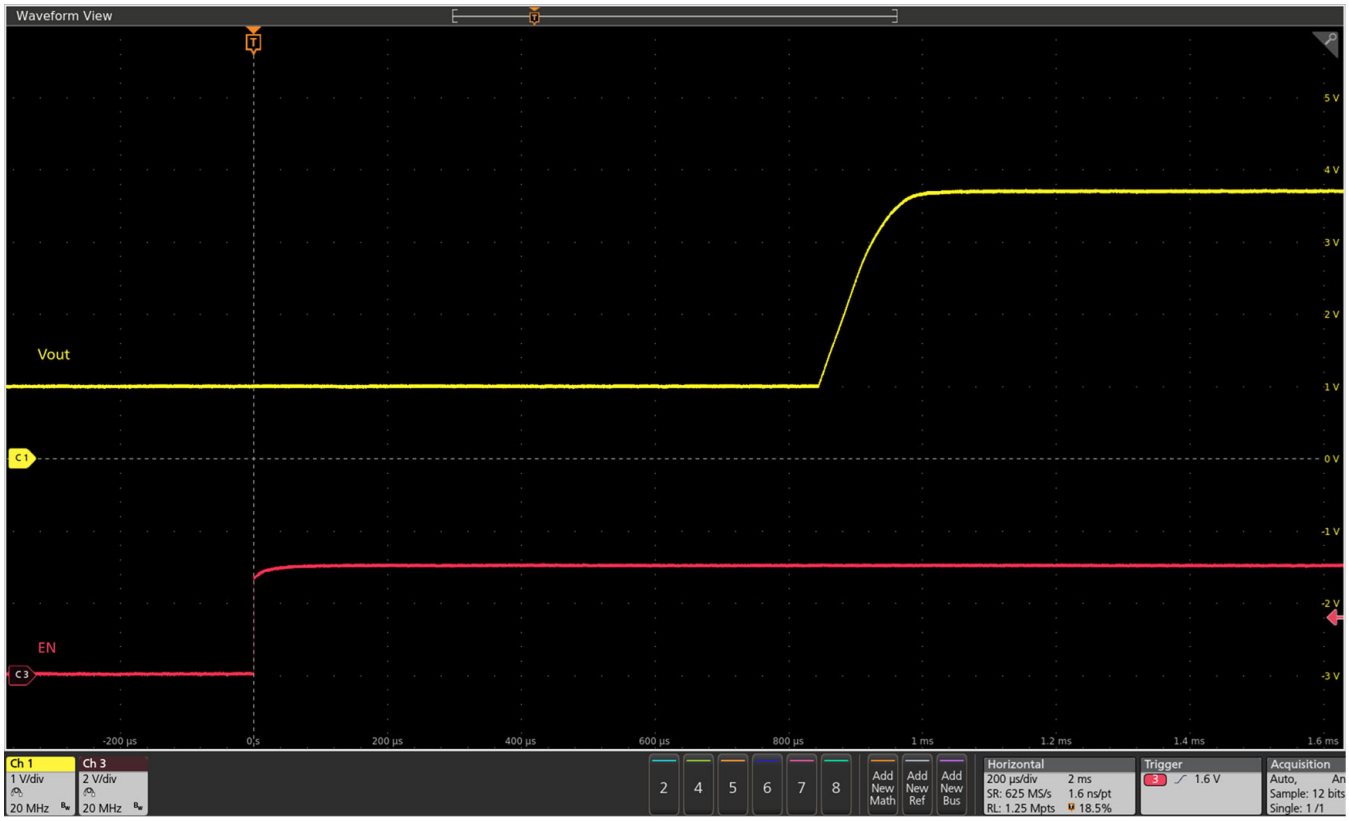


Figure 38. Soft Start Waveform into a Pre-charged Load

Soft-start Timeout

When the PE25213 first tries to supply power to the load, it uses a soft-start circuit to limit the power level. Using a soft start has no significant side effects if the start-up is “normal.”

If the PE25213 starts up into a fault, the soft start helps to manage the power supplied to the fault and limits the power dissipation in the PE25213. In normal, fault-free operation, the soft-start timeout is invisible if the soft-start current can ramp VOUT to the target voltage of 95% of the division ratio within 10 ms. If a fault occurs, the soft-start timeout occurs when VOUT does not ramp to the target voltage within the expected time. In this case, the soft-start timeout stops power to the load, and the PE25213 goes into a controlled shutdown sequence. When the soft-start sequence is complete—and after a 40-ms cooldown time—the PE25213 attempts the start-up again, as shown in Figure 39.

Figure 39 shows the flow for a persistent fault case. The fault initially triggers the recovery step, and then—assuming the charge pump remains enabled—the PE25213 attempts to soft start again. If VOUT is still held low by the fault, the PE25213 goes into a “hiccup” mode in which the soft-start timeout trips and causes the cooldown phase to restart. The Figure 39 loop repeats as long as the fault is present and the PE25213 remains enabled.

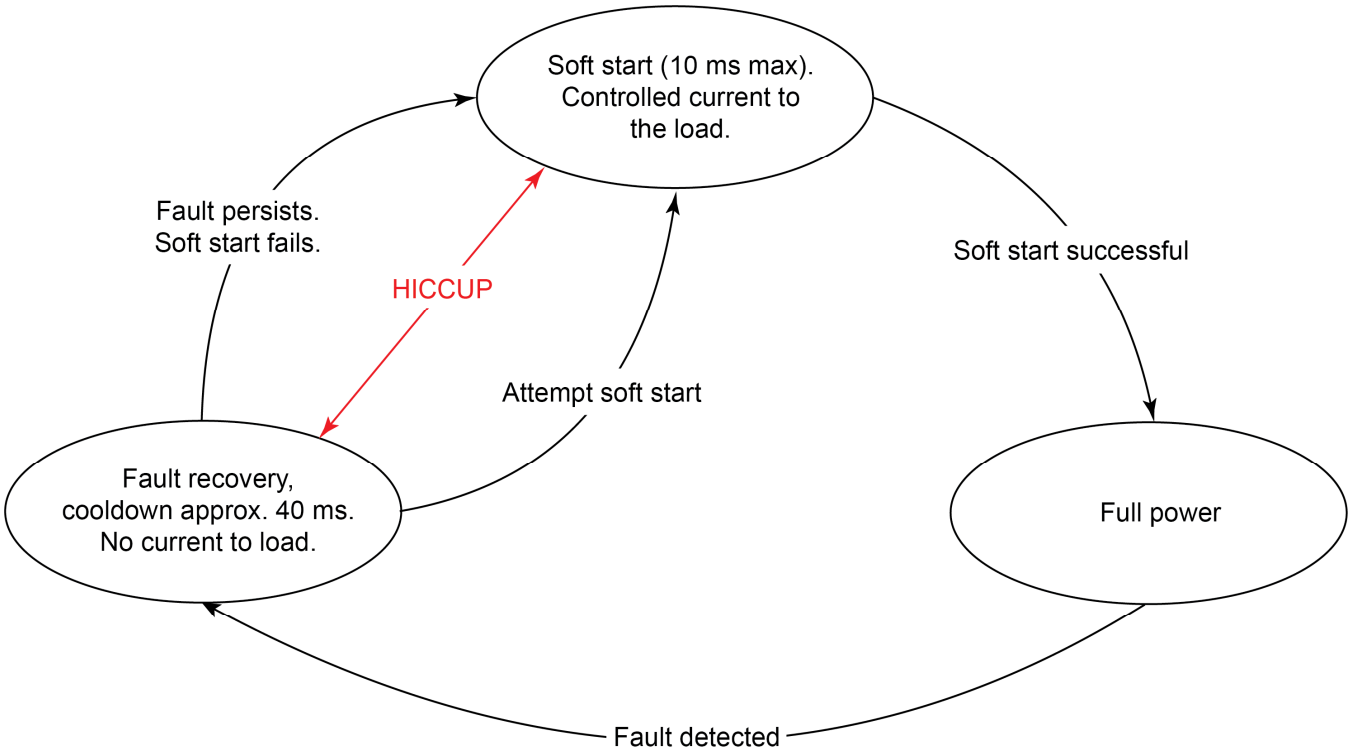


Figure 39. Hiccup Mode for Some Persistent Faults

Protection Modes

To protect the system and the PE25213 internal circuitry, pSemi built-in multiple fault detection circuits.

Table 8 summarizes the various protection modes.

Table 8. Protection Mode

Detector	Persistent fault(*)	Response time	Effect of the fault on the PE25213
V_{IN} under-voltage	Yes	ns	PGOOD goes low. The power stage of PE25213 turns off through a soft shutdown and stays off until the V_{IN} voltage exceeds the under-voltage lockout (UVLO) threshold.
V_{OUT} under-voltage	No	ns	PGOOD goes low. The power stage of PE25213 turns off through a soft shutdown. After a 40-ms cooldown period, the charge pump attempts to soft start again.
VX over-voltage	Yes	µs	PGOOD goes low. The PE25213 charge pump disconnects from VIN so no further power passes from VIN to the load. A load must be present to discharge the output. When the VX voltage falls below the V_{XOVP} threshold, the power stage fully turns off through a soft shutdown and the device restarts.
I_{LOADSC} current	No	ns	PGOOD goes low. The PE25213 power stage turns off through a soft shutdown. After a 40-ms cooldown period, the charge pump attempts to soft start again. For details, see I_{LOAD} Short Circuit and Over-current Protection on page 26.
V_{OUT} short circuit	No	µs	PGOOD goes low. The PE25213 power stage turns off through a soft shutdown. After a 40-ms cooldown period, the charge pump attempts to soft start again
I_{LOADOC} current	No	µs	PGOOD goes low. The PE25213 power stage turns off through a soft shutdown. After a 40-ms cooldown period, the charge pump attempts to soft start again. For details, see I_{LOAD} Short Circuit and Over-current Protection on page 26.
Over-temperature thermal shutdown	Yes	µs	PGOOD goes low. The PE25213 power stage turns off through a soft shutdown and stays off until the die temperature has reduced below the thermal shutdown level minus hysteresis.
V_{DD} under-voltage	Yes	µs	PGOOD goes low. The PE25213 power stage turns off immediately. This is an uncontrolled shutdown. The charge pump remains off until the internal VDD recovers.
Soft-start timeout	No	µs	If V_{OUT} does not reach the target voltage within the 10 ms soft-start timeout period, the charge pump enters cooldown state for approximately 40 ms before it attempts to soft-start again.
PGOOD held—or set—low when expected high	Yes	µs	From full power, the charge pump initially returns to a limited load current soft-start mode. If the PGOOD signal is held low for less than the soft-start timeout period, the charge pump returns to full power operation. If PGOOD = 0 exceeds the soft-start timeout, the charge pump loops through soft-start or cooldown until PGOOD is allowed to go high.
V_{OUT} over-voltage in divide-by-2 to divide-by-3 transition	Yes	–	If a dynamic switchover from divide-by-2 to divide-by-3 occurs and the output is not loaded during the transition, the device stays in reduced clock frequency mode indefinitely until the output is discharged.
Note: * A persistent fault keeps the charge pump in a fault state for as long as the fault is present. A non-persistent fault does not prevent the charge pump from re-enabling after applying the fault recovery time.			

PGOOD Operation

The PE25213 has an open drain “power good” pin. For proper operation, PGOOD must have an external pull-up to VIN, VDD or an external voltage >1.5V.

The PE25213 holds the PGOOD pin low whenever the charge pump is in soft-start, or when a fault condition is detected and being managed.

When the PE25213 allows PGOOD to be pulled high, the charge pump is ready to support the full load current.

The PGOOD pin of a disabled device is NOT pulled low. When EN = 0, the PGOOD pin can be ignored.

VIN Under-voltage and Thermal Shutdown Faults

The VIN under-voltage and thermal shutdown faults are grouped together because the effect they have on the charge pump is similar. If either of these faults is present when the charge pump is first enabled, then the charge pump starts to power-up but holds before any power—even soft-start current—is applied to the load. The charge pump holds in this state until both faults are clear, regardless of how long this takes. The VIN under-voltage and thermal shutdown faults are considered “persistent” because they hold the charge pump disabled until the fault clears.

In the case of VIN under-voltage, it is unlikely that the charge pump can support the full load current when VIN—and therefore VOUT—is too low. This is not preferable for the PE25213 or the load, so the charge pump waits for VIN to improve or recover.

An over-temperature fault is likely to occur only when the PE25213 is dissipating too much internal power. This fault normally results from some other fault condition, or from operating the PE25213 with low efficiency and high-power levels. If an over-temperature fault occurs, the PE25213 might start to operate outside of guaranteed performance specifications, which is not ideal for the system. To recover from over-temperature, the PE25213 stops switching, so it stops dissipating power and starts to cool down towards the ambient temperature.

When a VIN under-voltage or an over-temperature fault is detected during normal operation, the PE25213 goes into a controlled shutdown sequence with an unlimited cooldown period (there is a typical cooldown time of approximately 40 ms). When the faults clear, the PE25213 goes through a normal soft-start sequence and attempts to start-up.

VX Over-voltage Protection

The VX over-voltage fault detector is intended to protect both the PE25213 and the output load from over-voltage conditions. To ensure that an over-voltage at VX does not propagate to VOUT, the VX over-voltage detection circuit is designed to operate quickly. VX over-voltage faults are treated differently from most of the other fault flags.

The first response is to disconnect the PE25213 power stage from VIN. The path for power from VIN to VOUT opens to remove one source of the over-voltage. The charge pump does not continue to clock, and a fixed-frequency mode is temporarily enforced regardless of the FF pin connection. Clocking the charge pump without a connection to VIN creates a path from VX to GND which discharges VX. VX typically discharges rapidly so that the VX fault is cleared quickly.

To complete the recovery from the VX over-voltage, the PE25213 goes into a controlled shutdown sequence. When the soft-start sequence is complete—and after a 40-ms cooldown time—the PE25213 attempts to restart.

The initial response to the VX over-voltage of disconnecting VIN and continuing to clock continues—with no time limit—for as long as the VX over-voltage fault is detected. In most cases, this is expected to quickly clear the VX over-voltage within a few charge pump clocks. In the unlikely event that VX over-voltage is detected because of over-voltage at VOUT—for example due to a second power source in the system—the PE25213 attempts to discharge VX—and thus VOUT—through the switching action and the flying capacitors for an unlimited period. While in this VX over-voltage recovery state, some of the normal fault detectors—such as load current detectors—do not operate. For this reason, do not use VX over-voltage to recover from a system-caused VOUT over-voltage fault.

I_{LOAD} Short Circuit and Over-current Protection

The I_{LOAD} fault detection flags both operate in the same way by sensing the current being drawn from VIN. The short circuit flag (I_{LOADSC}) is a fast-acting fault with a high trip threshold and is designed to capture instantaneous fault levels, such as a dead short occurring at VOUT. The over-current protection flag (I_{LOADOC}) can be considered as a longer-term average current type of measurement. As a result, the trip point can be set closer to the nominal 10A maximum output load. The over-current protection trips if the PE25213 is operating outside the recommended operating conditions.

The reaction to the I_{LOADSC} and I_{LOADOC} faults is the same. The PE25213 goes into a controlled shutdown sequence. When the soft-start sequence is complete— and after a 40-ms cooldown time— the PE25213 attempts to restart. Persistent fault conditions can prevent the charge pump from restarting successfully, for example, in the event of a hard fault to GND at VOUT (which would trigger the I_{LOADSC} fault).

V_{OUT} Short Circuit and Under-voltage Protection

The VOUT short circuit and VOUT under-voltage fault detectors work in similar ways. They compare the measured value at VOUT with the expected value derived from VIN, so VOUT is compared with VIN/2 or VIN/3 depending on the MODE pin setting. The VOUT short circuit fault is designed to operate quickly, but only when VOUT is substantially below 60% of the target voltage. The VOUT under-voltage fault is designed to be slower and represents more of an average value. The VOUT under-voltage flag trips when VOUT goes below 80% of the target (V_{UVP}).

The VOUT short circuit detector is designed to operate in parallel to the I_{LOADSC} fault to give more independence from the external component values. For example, the result of a dead short to GND at VOUT while the PE25213 is operating at 10A depends partly on the inductor between VX and VOUT. VOUT could reach the V_{OUTSC} threshold sooner than I_{LOADSC} reaches the short circuit current limit, so supporting both fault detectors allows a better opportunity to stop the power going to the fault condition as soon as possible.

The VOUT under-voltage detector trips when VOUT goes below 80% of the target voltage. Choose the external components so that the expected transient loads do not trip the V_{UVP} threshold. In effect, the application must ensure that the load dependency causes less than 20% deviation from the nominal VOUT.

When a VOUT short circuit or VOUT under-voltage occurs, the effect on the charge pump is similar, and the same for I_{LOADSC}. The PE25213 goes into a controlled shutdown sequence. When the soft-start sequence is complete—and after a 40-ms cooldown time—the PE25213 goes through a normal soft-start sequence and attempts to restart.

VDD Under-voltage Protection

The VDD under-voltage fault condition is potentially serious. Much of the charge pump control and many of the fault detection flags use the VDD supply internally. For this reason, VDD must not be externally loaded to ensure that the VDD under-voltage fault is not triggered by external circuit load.

When VDD is pulled below the under-voltage trip voltage (approximately 3V), the charge pump shuts down immediately, PGOOD is pulled low, and no further power is supplied to the load. The internal VDD regulator has an internal short circuit current limit, so the VDD fault itself does not damage the PE25213, but the effects of stopping the supply to the load in an unplanned way could be serious. The PE25213 is designed to survive the immediate shutdown, but not all the effects of the shutdown are controlled by the PE25213 itself. For example, the inductor can cause a voltage spike as the load current is abruptly cut off. The voltage spike depends on the external inductor, the load capacitance, and the load current at the instant of shutdown. Consider the PE25213 absolute maximum ratings for the end application so that a VDD short can be managed without exceeding the device ratings.

The VDD under-voltage fault is “persistent,” so the PE25213 remains disabled for as long as VDD is held below the under-voltage threshold. When the fault clears, the PE25213 samples the FF and MODE pins again to get the chip configuration, then goes through a soft start sequence before allowing PGOOD to go high and flag that full power operation is possible.

Capacitor Imbalance

The PE25213 implements proprietary algorithms to handle capacitor imbalance in real-world solutions. Because the PE25213 is a charge pump-based DC-DC device, it uses four flying capacitors. In any real-world solution, the flying capacitor components are not ideal and likely not identical. The PE25213 can work with extremes of capacitance values, such as phase 1 capacitors at +20% of the nominal value and phase 2 capacitors at -20% of the nominal value. The proprietary algorithms allow full power to be supplied to the load and help prevent capacitor imbalance from inducing large ripple at the VX pin (and higher ripple at VOUT).

Application Information

The PE25213 is a charge pump-based DC-DC ratiometric converter. It is a high-efficiency bus converter in which the output follows the input by a fixed ratio of divide-by-2 or divide-by-3. Because of its architecture, there are differences from conventional inductive buck converters.

Application Schematic

Figure 40 shows a typical application circuit, with details of links and corresponding modes of operation, and suggested component values.

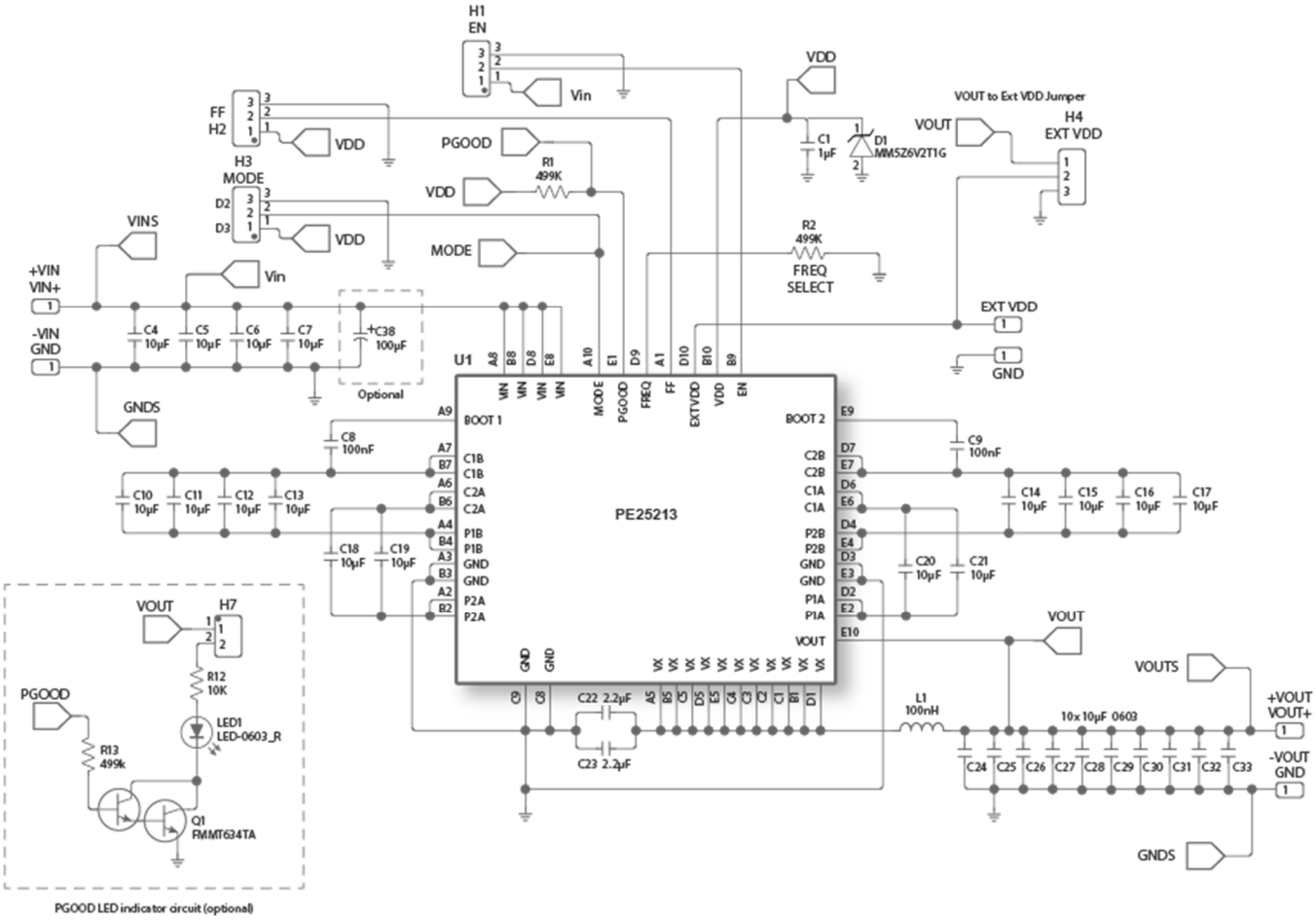


Figure 40. Detailed Application Schematic Circuit

Application Circuit Part List

Table 9. pSemi Recommended Parts

Reference number	Value	Part size	Part number
C1	1 µF 6.3V X7R or better	0402	GRM155R70J105KA12D
C4, C5, C6, C7, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21	10 µF 25V X5R or better	0603	GRM188R61E106KA73D
C8, C9	100 nF 100V X5R or better	0402	GRM155R62A104KE14D
C22, C23	2.2 µF 25V X5R or better	0402	GRM155C81C225ME15D (X6S)(*) GRM155R61E225KE11D (X5R)(*)
C24, C25, C26, C27, C28, C29, C30, C31, C32, C33	10 µF 25V X5R	0603	GRM188R61E106KA73D
D1	DIODE ZENER 6.2V 500 MW	SOD523	MM5Z6V2T1G
L1	100 nH	2.5 mm × 2 mm × 1.2 mm	TFM252012ALMAR10MTAA
R1, R2	499 kΩ	0603	RC0603FR-07499KL
U1	Divide-by-2 and -3, 10A Charge Pump, Capacitor Divider	4.545 mm × 2.715 mm	PE25213
Note: * X5R for applications with maximum $T_A \leq 85$ °C and X6S for applications with maximum $T_A > 85$ °C but ≤ 105 °C.			

Auto-switch Mode Circuit

The circuit in Figure 41 is implemented to achieve the auto-switch mode ratio of the PE25213 EVK.

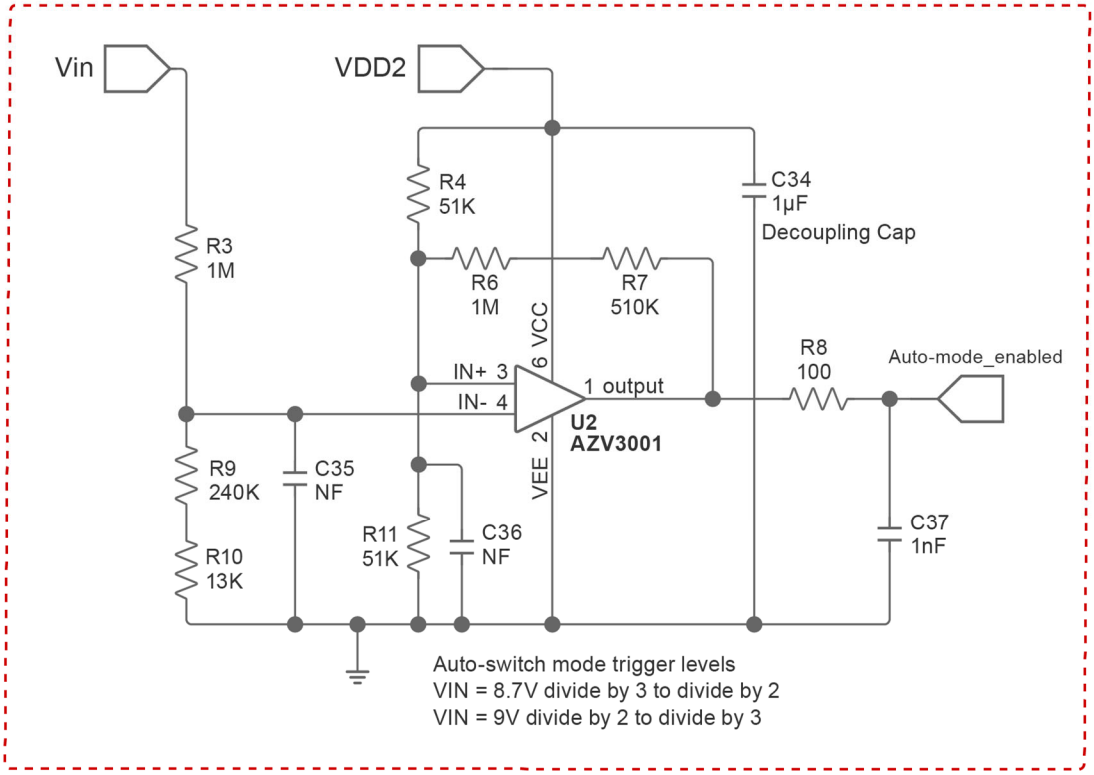


Figure 41. Optional Auto-switch Mode Circuit

Evaluation Board

Figure 42 shows the PE25213 device evaluation board.

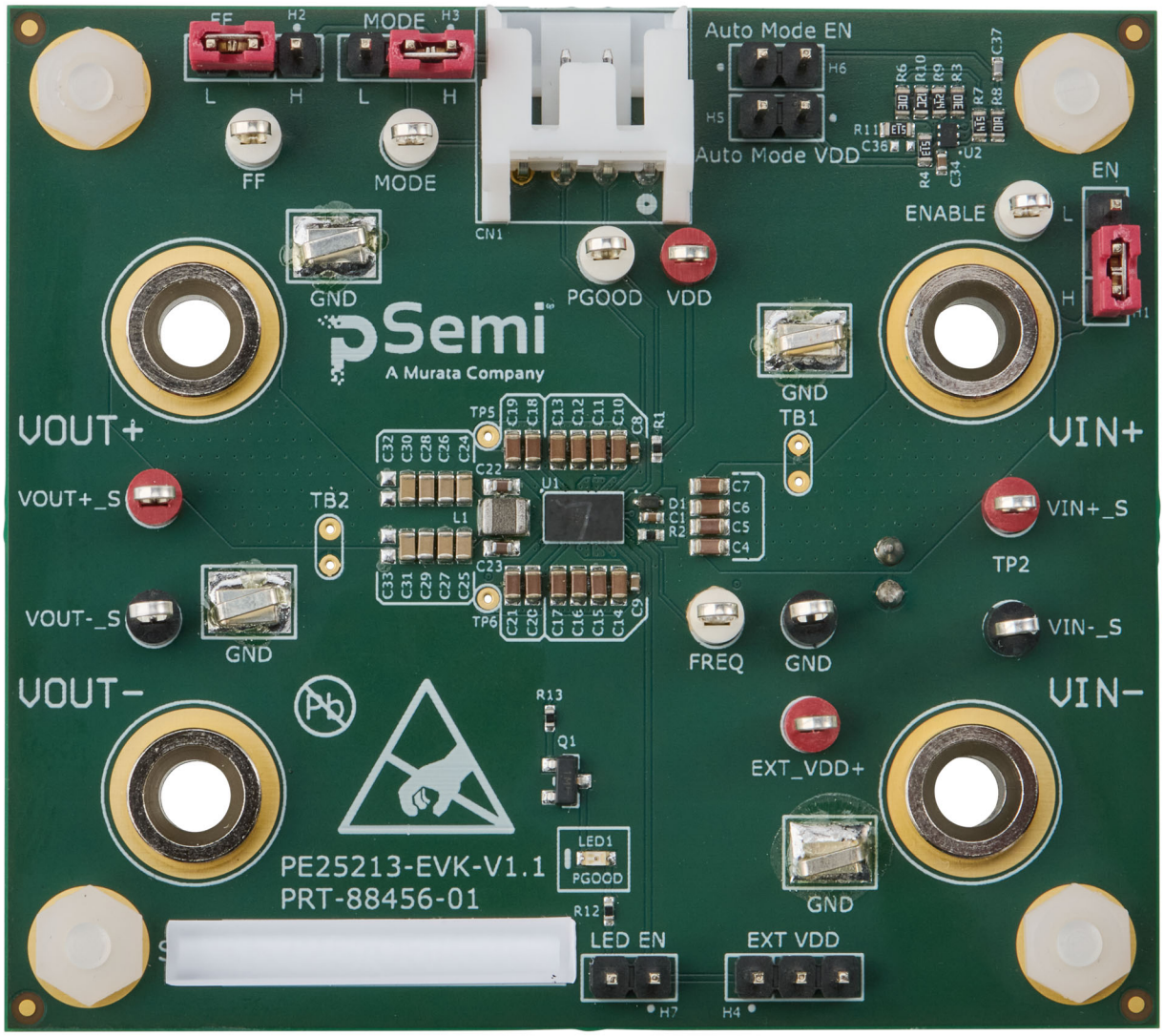


Figure 42. Device Evaluation Board (EVK)

Component Selection

This section describes the PE25213 required components.

Flying Capacitors

The PE25213 requires two sets of flying capacitors: the “CB” and “CA” capacitors. The CB capacitors connect between the C*B (C1B, C2B) and P*B (P1B, P2B) pins while the CA capacitors connect between the C*A (C1A, C2A) and P*A (P1A, P2A) pins. Both the CA and CB capacitors are important components for efficiency and must be placed as close to the PE25213 as possible.

The steady state voltage across the CB capacitors is 2* V_{OUT} for divide-by-3 mode and 1* V_{OUT} for divide-by-2. The steady state voltage across the CA capacitors is 1* V_{OUT} for both divide-by-3 and divide-by-2 modes. To take ripples and spikes into account, choose the capacitors so that the component voltage rating is higher than the steady state voltage. For example, for 15V V_{IN} and divide-by-3 operation, CB capacitors with a voltage rating of 16V, and CA capacitors with a 10V rating, are good choices.

The capacitance value at the applied voltage across the capacitors has a direct impact on the maximum efficiency that can be achieved. The nominal capacitance value typically drops as the voltage across the capacitor increases, depending on the voltage coefficient of the selected capacitors.

The recommended effective capacitance for CB and CA capacitors must have a typical value of 10 µF for nominal voltages. pSemi recommends that both CA and CB have similar effective capacitance under biased conditions within your operating voltage range.

While selecting the capacitor values for maximum efficiency, the switching frequency must also be taken into consideration so that the self-resonant frequency (SRF) of the capacitors is higher than the maximum charge pump switching frequency.

At maximum power, the PE25213 could reach a junction temperature of up to 125 °C (at 85 °C ambient). This can heat the surroundings of the die and potentially the flying capacitors. The choice of the temperature rating of the capacitors is dependent on the temperature gradient across the board and the placement of the capacitors with respect to the die.

Vx Capacitor

The Vx capacitor connects between the VX pin and the board-level power ground. Setting the Vx capacitor rating to exceed the Vx over voltage protection (V_{XOVP}) value is recommended so that the on-chip device protection circuits can activate before damage is caused to the Vx capacitor. This increases system robustness to fault situations. The Vx capacitor function is to reduce the voltage ripple at VX, but it can also cause higher charge redistribution loss and reduction of efficiency. The Vx capacitor value must be optimized around those criteria.

The recommended effective capacitance used for Vx capacitors must have a typical value of 2.5 µF for nominal voltages.

Lx Inductor

The Lx inductor connects Vx to V_{OUT} (and the load). V_{OUT} is a filtered version of Vx. Lx reduces the charge distribution loss when switching between the two complementary switching phases used by the PE25213. The higher the inductance value, the lower the charge distribution loss, but also the higher the voltage ripple on Vx. Choose an optimum value of Lx to minimize the charge distribution loss while supporting acceptable voltage ripple at Vx and V_{OUT}. The recommended inductance value is 100 nH.

The Lx inductor must support the full load output current. For robust system design, the Lx inductor must support the ILOAD output current limit (I_{LIM}) of 12A. This allows the on-chip protection circuits to activate before causing inductor damage if a fault situation occurs. The path from Vx to V_{OUT} through the Lx inductor must be achieved with minimum parasitic resistance because losses in the inductor or in the system-level routing can directly impact on the system efficiency.

Output Capacitor

The output capacitor reduces the ripple applied to the load at V_{OUT}. The higher the capacitor value, the lower the ripple at V_{OUT}. Increasing the output capacitor value increases the soft-start duration and could cause the PE25213 to timeout during soft start. The soft-start current must charge the chosen output capacitor value within the soft-start timeout duration.

The recommended effective capacitance for the C_{OUT} capacitors is 40 µF for nominal voltages.

VDD Capacitor

The recommended effective capacitance for the VDD capacitor is 0.5 µF for 3.6V, which is the typical VDD voltage.

Input Capacitor

The input capacitor connects V_{IN} and GND. It reduces the ripple on V_{IN} as the PE25213 switches. To reduce any parasitic inductance effects, place the input capacitor as close to the device as possible. The voltage rating of the capacitor must be as high as the absolute maximum voltage rating for the system and the effect of the capacitor voltage coefficient must be considered to determine the effective capacitance value at the applied V_{IN}.

pSemi recommends 7 µF or higher effective capacitance for the C_{IN} capacitors for the nominal voltages.

The recommended effective capacitance values from this section are for the components used in table 10. For an optimized value selection based on your application, contact pSemi.

Sample Layout

Figure 43–Figure 46 show a Type-III PCB layout example using a 4-layer board. The trace width and spacing are 0.1 mm/0.1 mm. The via size is a 0.2-mm hole and a 0.4-mm pad.

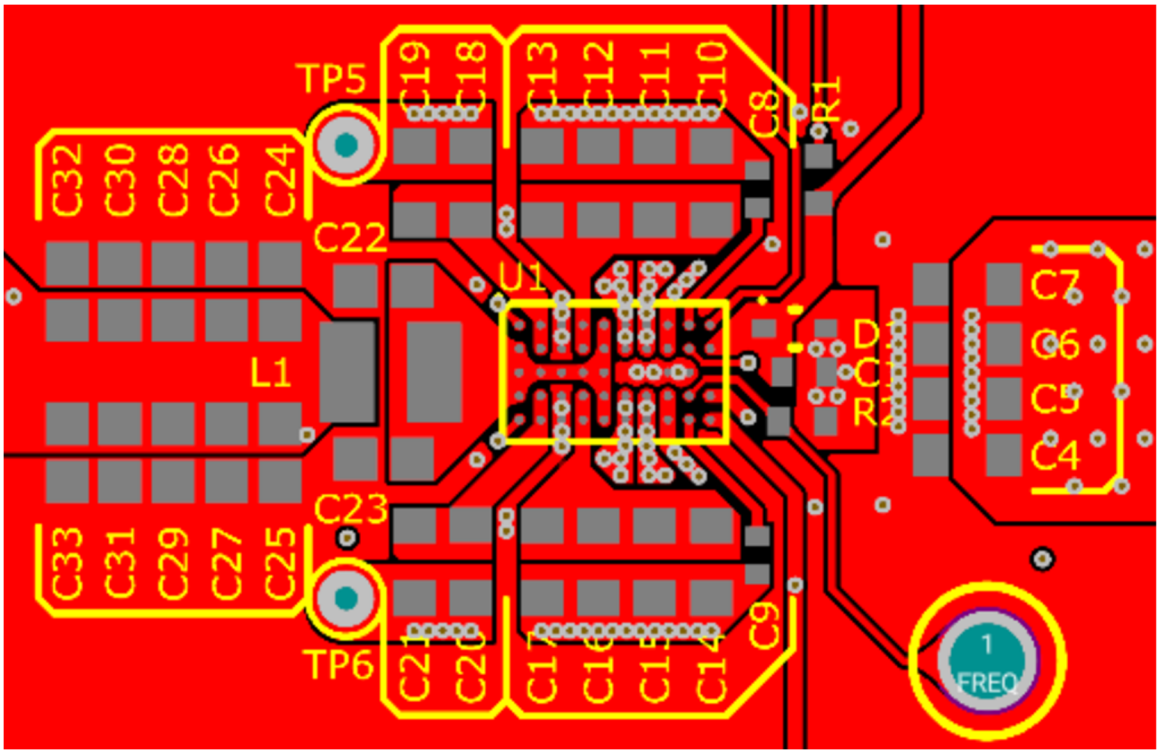


Figure 43. Top Layer

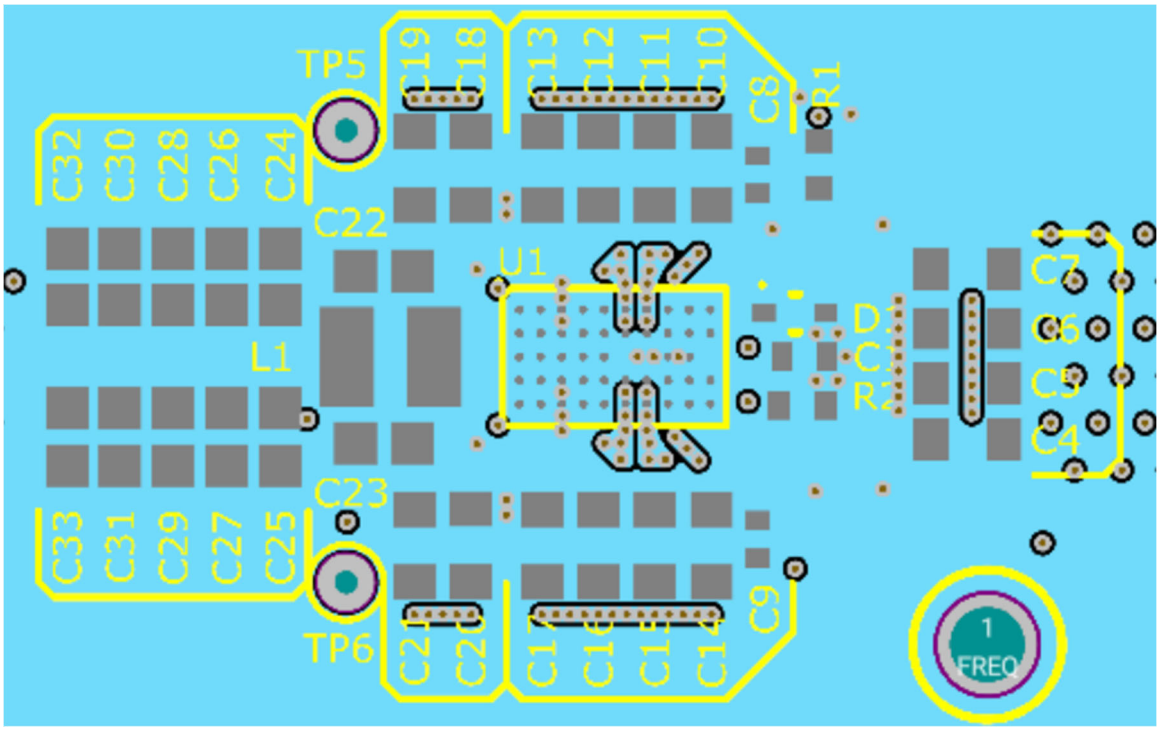


Figure 44. Inner Copper Layer 1

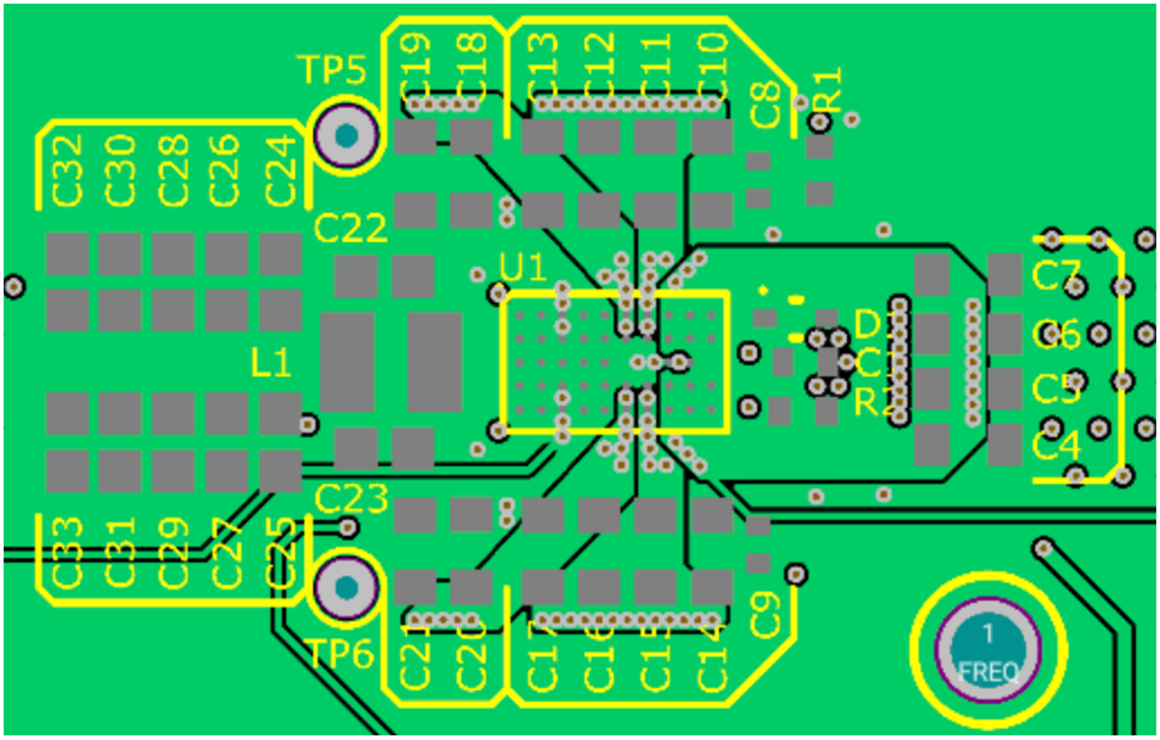


Figure 45. Inner Copper Layer 2

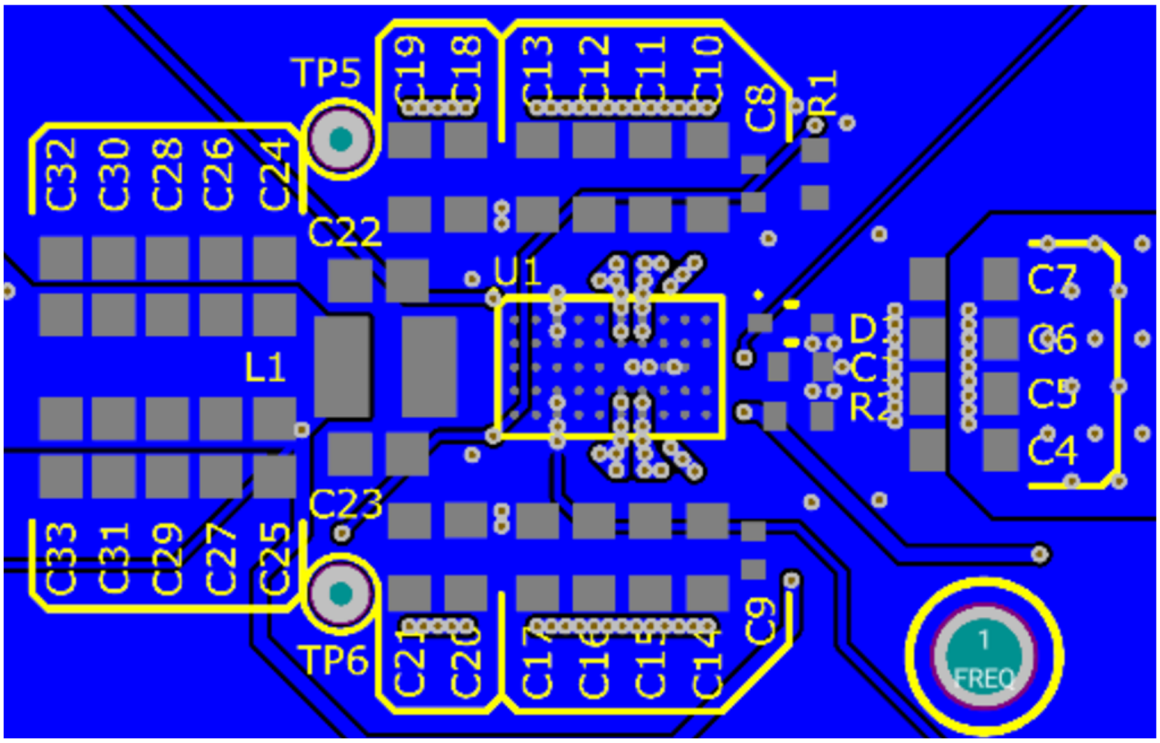


Figure 46. Bottom Copper Layer

Packaging Information

This section provides the following packaging data:

- Moisture sensitivity level (MSL)
- Package drawing
- Package marking
- Tape-and-reel information

Moisture Sensitivity Level

The PE25213 moisture sensitivity level rating for the 4.545 mm × 2.715 mm WLCSP is MSL 1.

Package Drawing

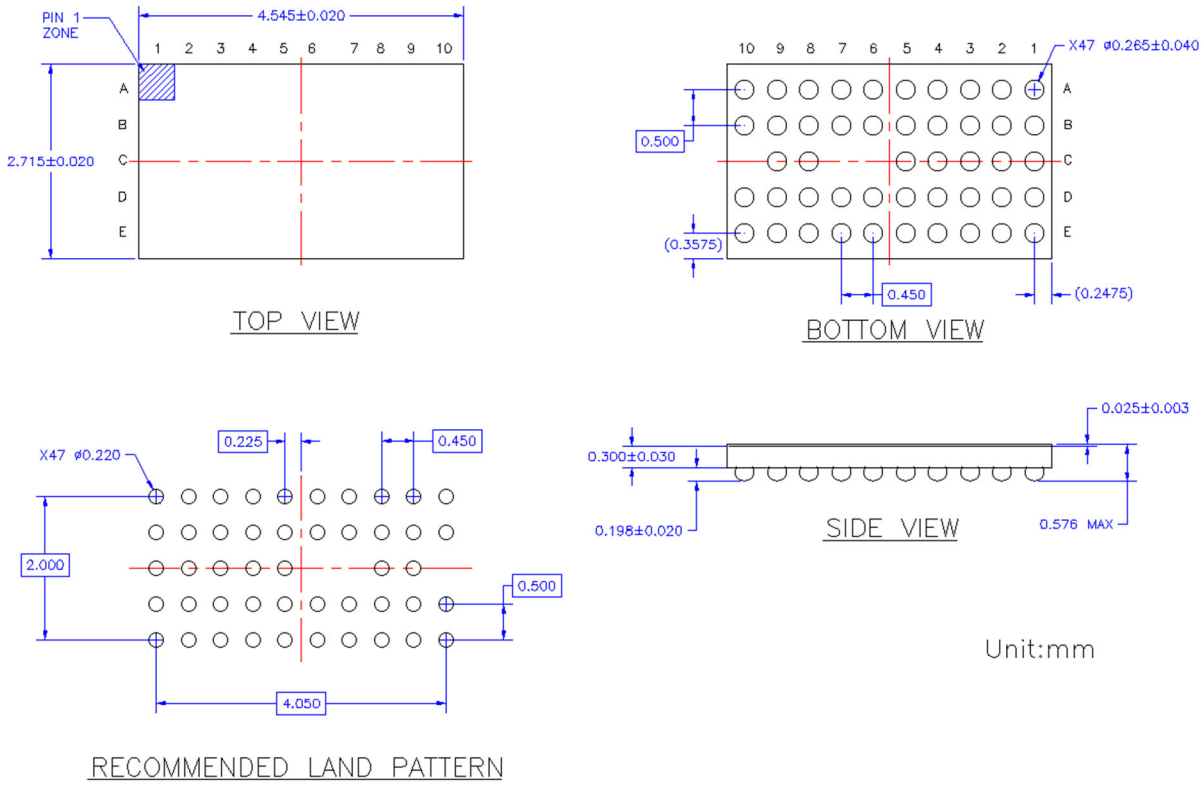


Figure 47. Package Outline Drawing

Top-marking Specification

● = Pin 1 indicator
PPPPP = Product part number
ZZZZZZ = Assembly lot code (maximum six characters)
YY = Last two digits of assembly year (2022 = 22)
WW = Assembly Work Week (01,02,03,...,52)

Figure 48. PE25213 Package Marking Specification

Tape and Reel Specification

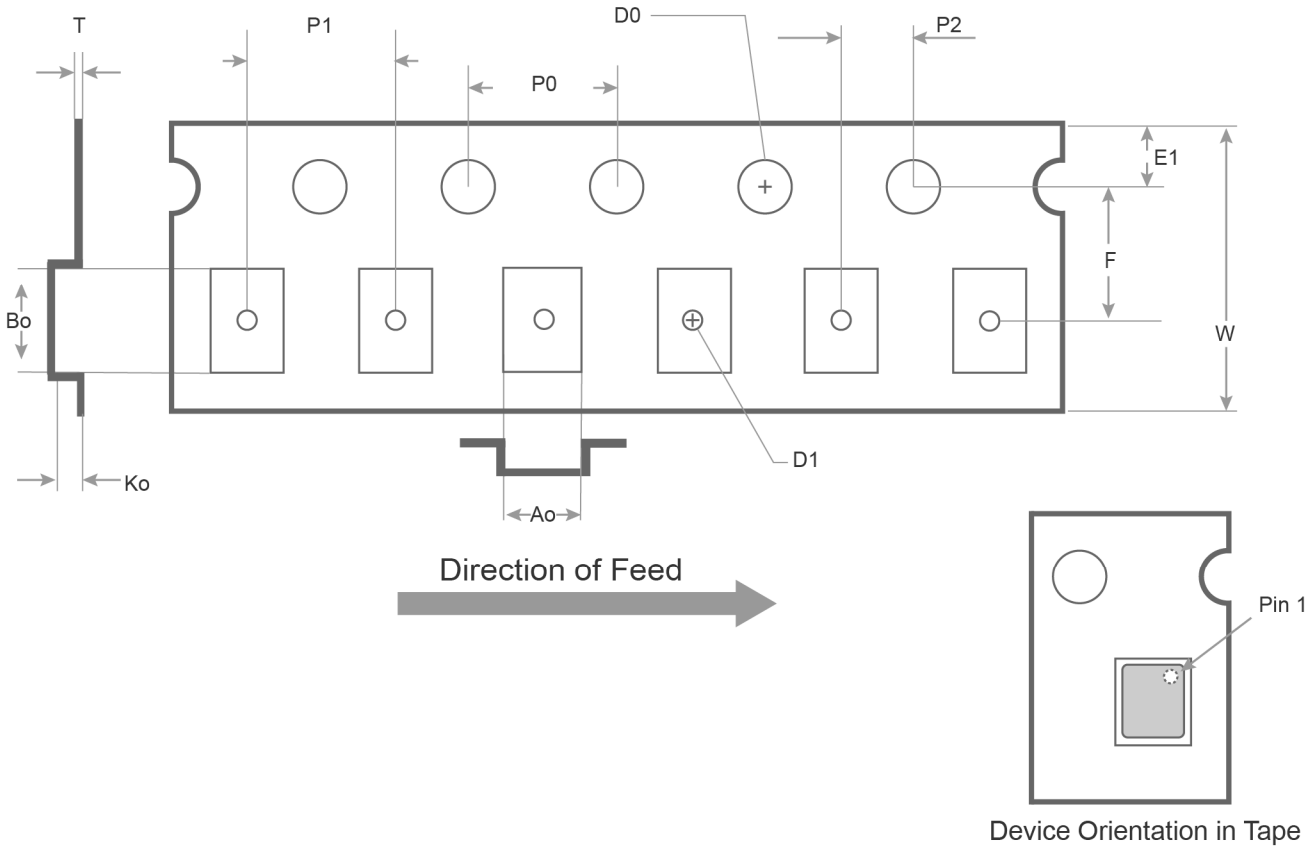


Figure 49. Tape and Reel Specifications for the 4.545 mm × 2.715 mm WLCSP

Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 10. Tape and Reel Dimensions

Carrier tape dimensions					
Pocket	**Nominal**	**Tolerance**	**Pocket**	**Nominal**	**Tolerance**
Ao	2.97	±0.05	D1	1.00	±0.05
Bo	4.80	±0.05	D0	1.50	+0.10/-0
Ko	0.91	±0.05	E1	1.75	±0.10
P1	8.00	±0.10	P0	4.00	±0.10
W	12.00	+0.30/-0.10	P2	2.00	±0.05
F	5.50	±0.05	T	0.25	±0.02

Ordering Information

Table 11. Order Codes and Shipping Methods

Order code	Description	Packaging	Shipping method
PE25213A-V	10A Charge Pump Divide by 2 or 3	WLCSP on tape and reel	250 Units/T&R
PE25213A-R			5000 Units/T&R
EK25213-01	PE25213 DC-DC Converter Evaluation Board	Populated PCB	1 Unit

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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