

PE25304

Document category: Preliminary Specification

Ultra-thin, high-efficiency 72W DC-DC converter module



Features

- Open drain power-good output
- Over-current and over-temperature protections
- Compensation loop-less charge pump
- Synchronizes to an external clock
- Stackable up to four modules
- Wide input voltage: 20V to 60V (DIV4)
- Suitable for 48V bus systems
- Efficiency:
 - Up to 96.5%
 - Up to 95.0% with 48V_{IN}/6A
- Up to 6A
- Package: Ultra-thin/small 11.5 × 9.5 × 2.0 mm LGA with T = 2.1 mm (maximum)

Applications

- Data center/server
- Networking equipment
- Base station
- Optical equipment
- Test equipment
- LED signage

Efficiency

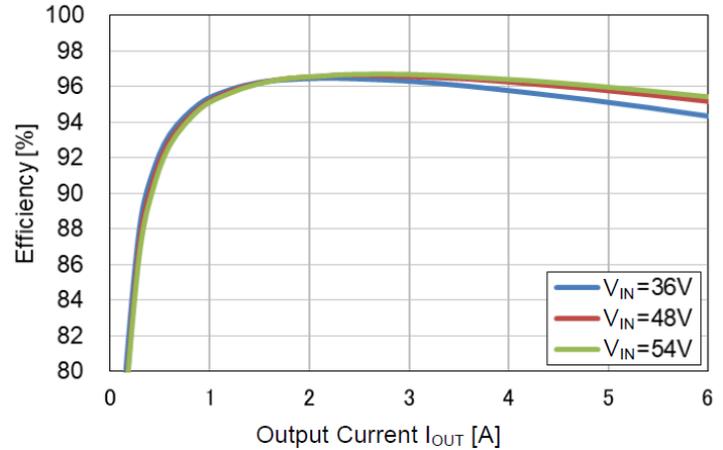


Figure 1. Efficiency curve at T_A = 25 °C

Simplified application

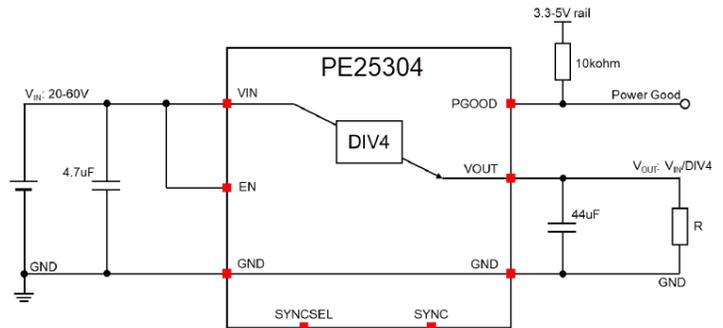


Figure 2. Simplified circuit diagram

Product description

The pSemi PE25304 is an ultra-thin, high-efficiency, integrated power solution that combines a 72W DC-DC converter with components. This total power solution can be used in a system without loop compensation and with just three external components in the minimum case.

This fully integrated module provides up to 96.5% efficiency despite its small and thin 11.5 × 9.5 × 2.0 mm LGA package. The pSemi easy-to-use module pinout design allows simple power layout and provides maximizing efficiency by minimizing routing parasitic resistance.

This module is fixed divide-by-4 conversion ratio from input voltage to output voltage. The 20–60V input voltage range supports 48V bus systems.

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Absolute maximum ratings

 Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

 When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Table 1. PE25304 absolute maximum ratings⁽¹⁾

Parameter	Symbol	Min	Max	Unit
V _{IN}	V _{IN}	-0.3	61	V
EN	–	-0.3	V _{IN} + 0.3	V
SYNC, SYNCSEL, and PGOOD	–	-0.3	5.5	V
V _{OUT}	V _{OUT}	-0.3	V _{IN} /4 + 0.1	V
Output current	I _{OUT}	0	8	A
Storage temperature	T _{STG}	-40	125	°C
Soldering and reflow temperature	–	–	260	°C
Maximum number of reflows allowed	–	–	2	–
ESD tolerance, HBM ⁽²⁾	–	–	1000	V

-  1. The above absolute maximum ratings are stress ratings only; the notation of these conditions does not imply functional operation of the PE25304 at these or any other conditions that fall outside the range identified by the operational sections of this specification.
2. Human body model, per JEDEC standard JS-001-2012.

Recommended operating conditions

Table 2 lists the PE25304 recommended operating conditions.

 Do not operate the device outside the operating conditions listed below.

Table 2. PE25304 recommended operating conditions⁽¹⁾

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{IN}	20	60	V
Ambient temperature ⁽²⁾	T_A	-40	105	°C
Junction temperature ⁽²⁾	T_J	-40	120	°C
Output current	I_{OUT}	0	6	A

-  1. The reliability is tested at the maximum voltage of the recommended operating condition. Operation above the recommended range could reduce the reliability of the device.
2. See the temperature derating curves in the [Thermal deratings](#). However, do not condensate.

Package thermal characteristics

Table 3. PE25304 package thermal characteristics⁽¹⁾⁽²⁾

Parameter	Symbol	Typ	Unit
Junction-to-case-top at heat junction	Θ_{JCT}	15.9	°C/W
Junction-to-case-bottom at heat junction	Θ_{JCB}	4.7	°C/W

-  1. The package thermal characteristics were modeled and simulated in a manner consistent with JEDEC standards JESD51-8 and JESD51-12. See also pSemi [Application Note 57: Thermal Characterization](#).
2. The junction-to-ambient thermal resistance (Θ_{JA}) is a function not only of the device, but it is also extremely sensitive to the environment, which includes—but is not limited to—board thickness, planes, copper weight, copper routes, and air flow. To realize the expected thermal performance, pay close attention to the board layout.

Electrical characteristics

Table 4 lists the PE25304 key electrical specifications under the following conditions, unless otherwise specified: $V_{IN} = 48V$, $I_{OUT} = 6A$, and $T_A = 25\text{ }^\circ\text{C}$.

Table 4. PE25304 electrical characteristics⁽¹⁾

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<i>Input supply</i>						
Input voltage range	V_{IN}	–	20	–	60	V
Input voltage start-up slew rate ⁽²⁾	V_{IN_SR}	–	0.2	–	–	V/ms
Input voltage under-voltage lockout (UVLO) threshold with V_{IN} rising	V_{IN_UVH}	$I_{OUT} = 0A$	–	18.1	–	V
Input voltage UVLO hysteresis	V_{IN_UVL}	$I_{OUT} = 0A$	–	0.9	–	V
Input voltage switching supply current	I_{IN_SW}	$V_{IN} = 48V$, no load	–	11	–	mA
Input voltage shutdown supply current	I_{IN_SD}	$V_{IN} = 48V$, $EN = 0V$	–	0.15	–	μA
<i>Enable input (EN) pin</i>						
Enable threshold high ⁽²⁾	V_{TH_ENH}	–	2.6	–	–	V
Enable threshold low ⁽²⁾	V_{TH_ENL}	–	–	–	0.6	V
Enable input rising duration ⁽²⁾	t_{R_EN}	0V to V_{TH_ENH}	–	–	1	ms
Enable pin input current	I_{EN}	$EN = V_{IN} = 48V$, $T_A = 125\text{ }^\circ\text{C}$, no load	–	42	–	μA
<i>Power good (PGOOD) pin</i>						
PGOOD output pulldown low level ⁽²⁾	V_{PG_LOW}	$I_{PG} = 20\text{ mA}$	–	–	0.25	V
PGOOD input high voltage ⁽²⁾	V_{PGH}	–	3.0	–	–	V
PGOOD V_{OUT} threshold	V_{TH_PGH}	V_{OUT} rising, no fault	–	$0.95 \times V_{IN}/4$	–	V
PGOOD released V_{OUT} threshold	V_{TH_PGL}	V_{OUT} falling after $PGOOD = H$	–	$0.8 \times V_{IN}/4$	–	V
<i>SYNCSEL pin</i>						
Threshold low ⁽²⁾	V_{TH_SYNL}	–	–	–	0.4	V
<i>Output</i>						
Efficiency peak	EFF_{PK}	$V_{IN} = 48V$, $I_{OUT} = 2.4A$	–	96.5	–	%
Efficiency full load	EFF_{FULL}	$V_{IN} = 48V$, $I_{OUT} = 6A$	–	95.0	–	%
Switching frequency	f_{SW}	–	–	270	–	kHz
Soft start input current limit ⁽³⁾	I_{IN_SS}	–	–	134	–	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Soft start timeout duration ⁽³⁾	t_{TO_SS}	–	–	100	–	ms
Output current, continuous ⁽³⁾	I_{OUT}	Inside recommended OP range	–	–	6	A
Output current, start-up ⁽³⁾	I_{OUT_START}	–	–	–	20	mA
Output voltage	V_{OUT}	$V_{IN} = 48V$, full load condition, DC	–	$96\% \times V_{IN}/4$	–	V
Equivalent output resistance ⁽⁴⁾	R_{OUT}	$V_{IN} = 48V$, $I_{OUT} = 6A$	–	0.086	–	Ω
Total external output capacitance ⁽²⁾	C_{OUT}	–	44	–	400	μF
Total external output capacitance with parallel operation ⁽²⁾	C_{OUT_P}	n = the number of parallel devices	$44 \times n$	–	400	μF

Protection

Thermal shutdown threshold ⁽²⁾	T_{TH_OTP}	Temperature rising	125	150	–	$^{\circ}C$
Thermal shutdown hysteresis	T_{HYS_OTP}	–	–	16	–	$^{\circ}C$
Over-current protection	I_{TH_OCP}	–	–	10	–	A
Short circuit protection	I_{TH_SHORT}	–	–	15	–	A

Environmental

Moisture sensitivity level	MSL	–	3			
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1. The minimum and maximum specifications are 100% production tested at $T_A = 25^{\circ}C$, unless otherwise noted. Limits over the operating range are guaranteed by design.
2. Guaranteed by design.
3. The load currents could cause start-up failure due to the soft-start timeout fault. Devices supplied power from this device must start up after the PGOOD signal is in the high state.
4. $R_{OUT} = (V_{IN}/4 - V_{OUT})/I_{OUT}$.

Pin configuration

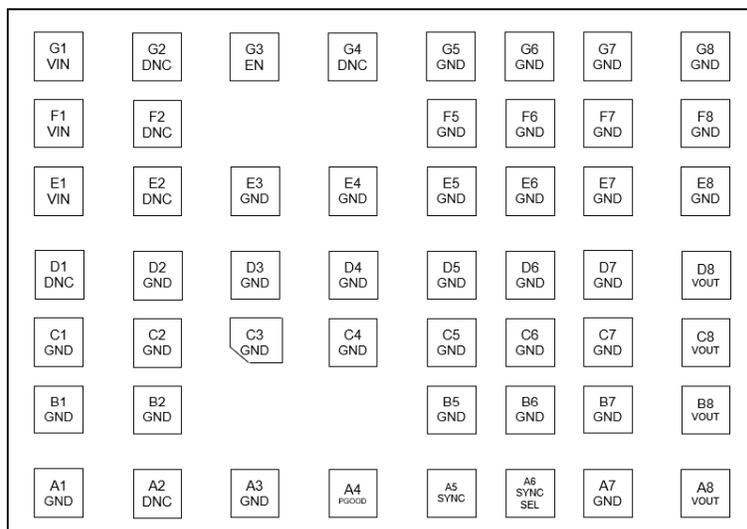


Figure 3. Module terminals, top view

Pin description

Table 5. Pin description

Pin number	Pin name	Description
A1, A3, A7, B1, B2, B5-7, C1-7, D2-7, E3-8, F5-8, G5-8	GND	Ground for power and thermal. Connect the ground plane in low impedance.
E1, F1, G1	VIN	Power input terminal
A8, B8, C8, D8	VOUT	Power output terminal
G3	EN	Device enable terminal. Do not leave this terminal open. High = ON, Low = OFF
A5	SYNC	CLOCK IN/OUT terminal. The direction is configured by the SYNCSEL terminal potential.
A6	SYNCSEL	SYNC terminal control. Low = CLKOUT, Open = CLKIN.
A4	PGOOD	Power good terminal. Connect a 10 kΩ resistor from PGOOD to an external bus voltage between 3.0–5.5V.
A2, D1, E2, F2, G2, G4	DNC	Do not connect these pins electrically. These pins must be soldered to the board but must be left floating electrically with respect to each other.

Functional block diagram

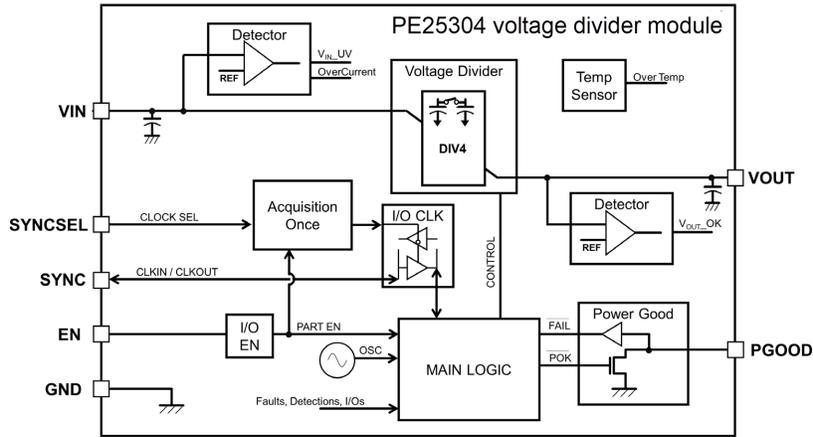


Figure 4. Functional block diagram

Application circuit

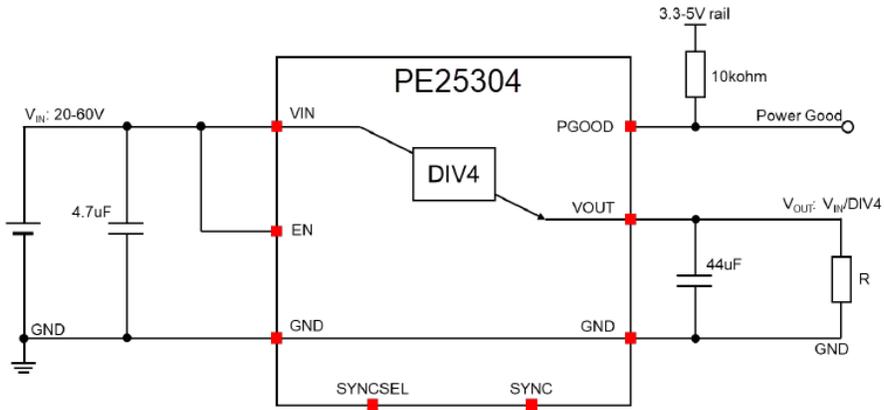


Figure 5. Application circuit

Typical performance characteristics

In this data sheet, all characteristics were measured with the application board shown in [Figure 26](#). [Figure 25](#) shows the board schematic, and [Table 9](#) lists the board parts. The board is under $T_A = 25\text{ }^\circ\text{C}$ with no airflow, unless otherwise noted.

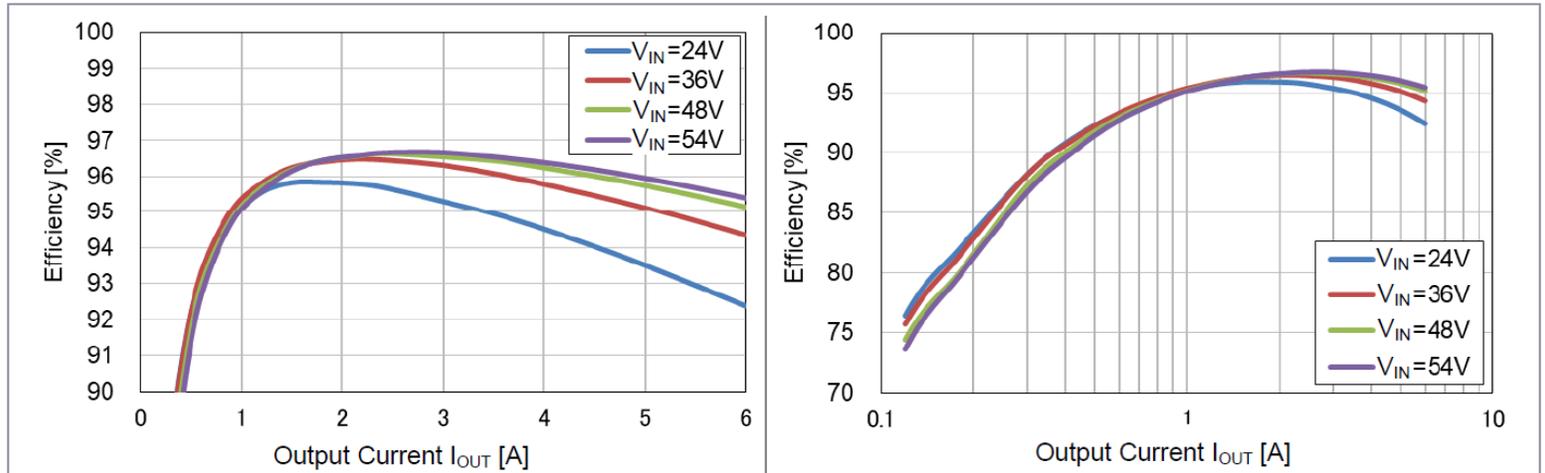


Figure 6. Efficiency, linear and log scale

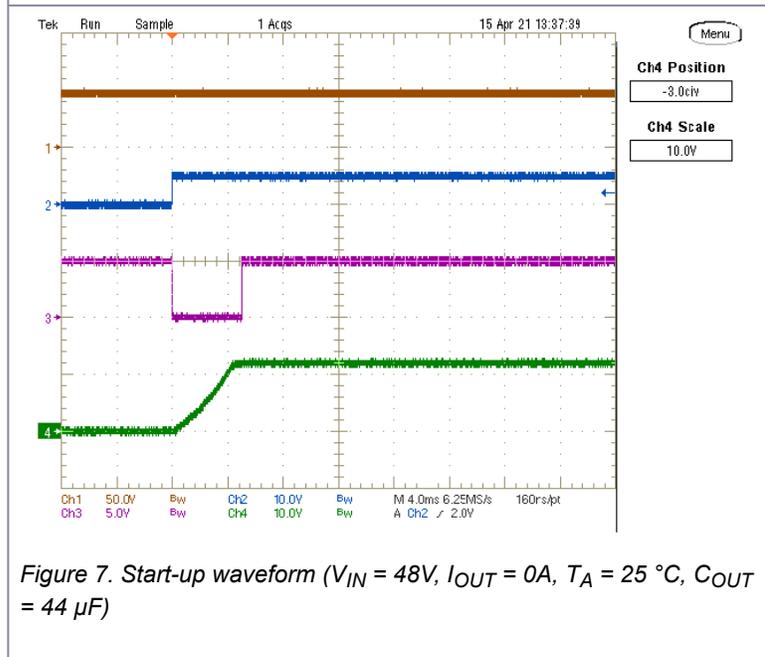


Figure 7. Start-up waveform ($V_{IN} = 48\text{V}$, $I_{OUT} = 0\text{A}$, $T_A = 25\text{ }^\circ\text{C}$, $C_{OUT} = 44\text{ }\mu\text{F}$)

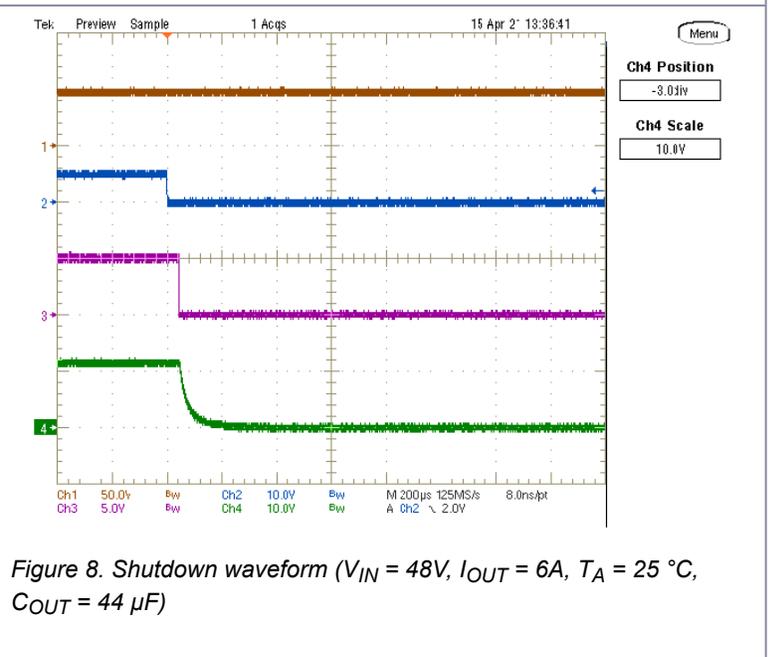


Figure 8. Shutdown waveform ($V_{IN} = 48\text{V}$, $I_{OUT} = 6\text{A}$, $T_A = 25\text{ }^\circ\text{C}$, $C_{OUT} = 44\text{ }\mu\text{F}$)

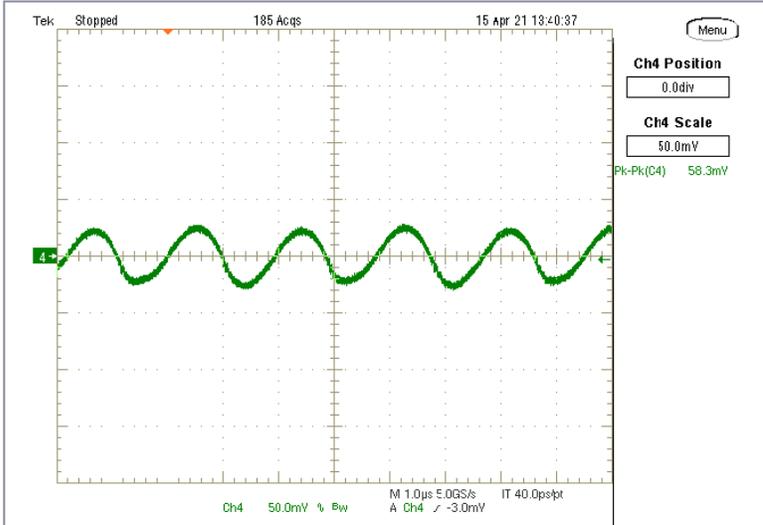


Figure 9. V_{OUT} ripple waveform ($V_{IN} = 48V$, $I_{OUT} = 0A$, $T_A = 25^\circ C$, $C_{OUT} = 44 \mu F$)

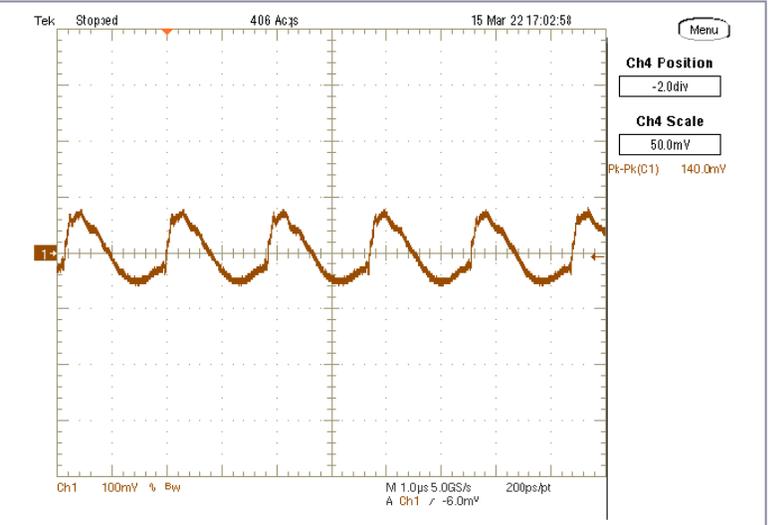


Figure 10. V_{IN} ripple waveform ($V_{IN} = 48V$, $I_{OUT} = 0A$, $T_A = 25^\circ C$, $C_{IN} = 9.4 \mu F$)

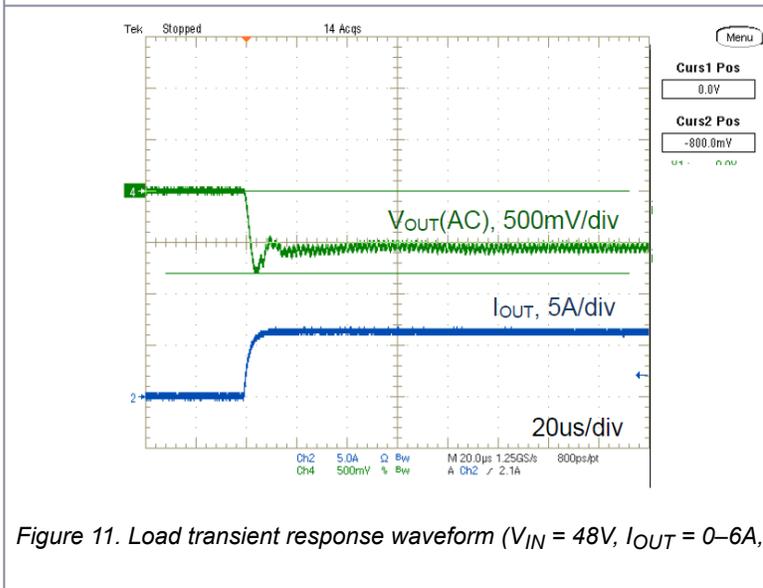
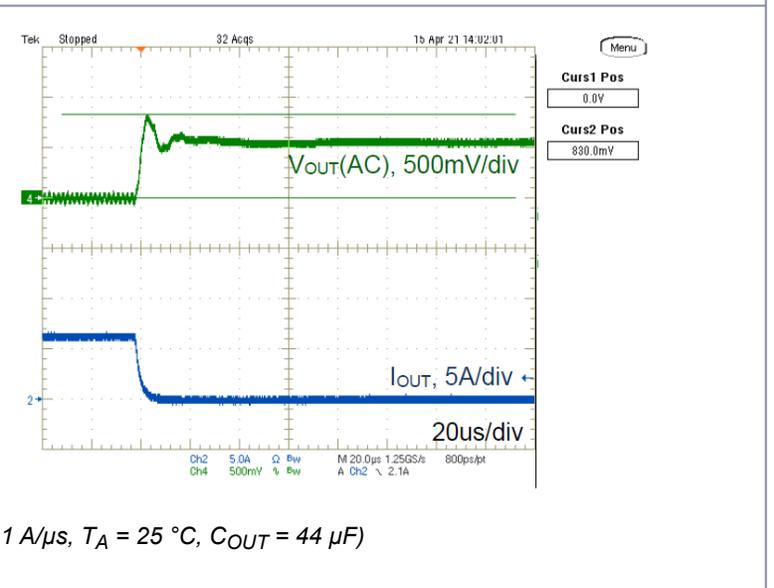


Figure 11. Load transient response waveform ($V_{IN} = 48V$, $I_{OUT} = 0-6A$, $1 A/\mu s$, $T_A = 25^\circ C$, $C_{OUT} = 44 \mu F$)



Thermal deratings (reference data)

The thermal deratings are evaluated in following conditions:

- The product is mounted on a 114.5 × 101.5 × 1.6 mm FR-4 board:
 - Layers 1 and 4 are 2-ounce copper.
 - Layers 2 and 3 are 1-ounce copper.
- The product surface temperature is 116 °C, maximum.

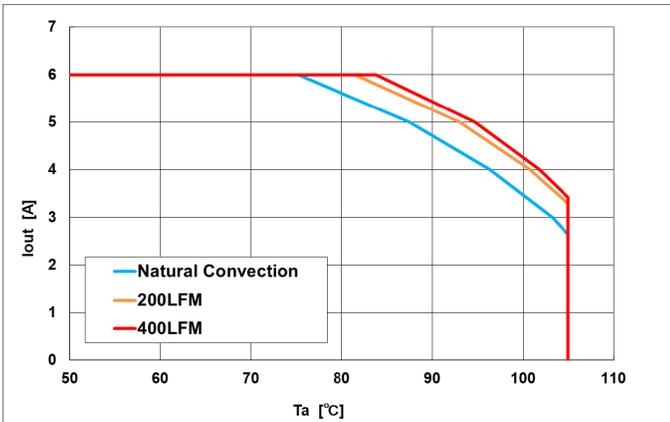


Figure 12. Thermal deratings, $V_{IN} = 48V$

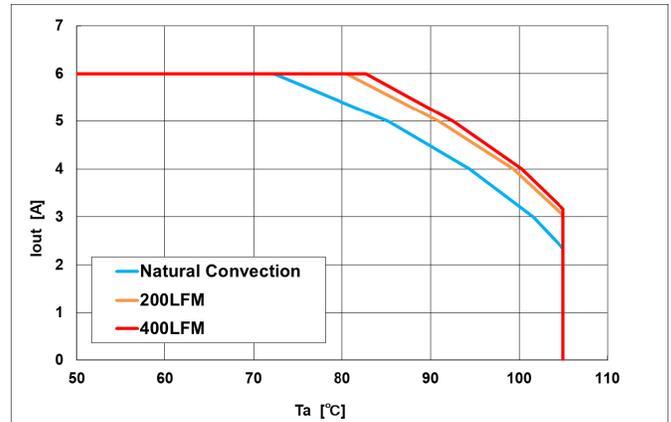


Figure 13. Thermal deratings, $V_{IN} = 54V$

Detailed description

The PE25304 is a divide-by-4, two-phase charge pump-based DC-DC converter, so any change in its input voltage is reflected at the output. The PE25304 can be powered from the 20–60V input voltage range. The supported output voltage range is 5–15V with load currents of 6A.

The SYNCSEL pin can be tied to ground or left floating:

- If tied to ground, the device uses an internal clock, and this clock signal appears at the SYNC pin.
- If left floating, the SYNC pin acts as an input. For details, see [Table 7](#).

The pin configurations are sampled when the PE25304 starts up and before the charge pump stage is enabled. The configuration pins are not designed to be driven dynamically, so they must be in a fixed state at power up.

Start-up EN and V_{IN} relationship

The PE25304 has an enable input pin, EN, which pSemi designed to be compatible with typical low-voltage digital I/O levels so that it can be easily driven by an external controller. EN can be also connected to the VIN pin. If external power sequencing or control is not required, tie EN to the VIN pin.

If the EN pin is held low until V_{IN} reaches its nominal voltage, the PE25304 follows the initialization sequence in Figure 14.

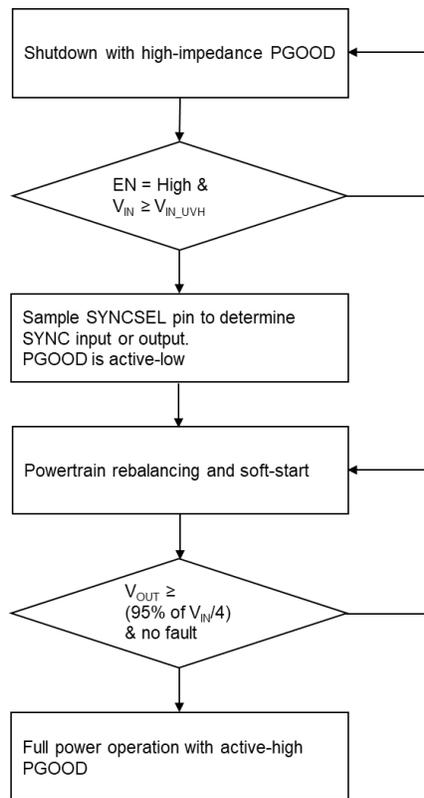


Figure 14. Initialization sequence

Enable (EN)

The PE25304 is enabled by an active-high EN input pin when a voltage higher than 2.6V is applied. The PE25304 is disabled when the voltage at the EN pin falls below 0.6V. The EN pin can be shorted to the VIN pin to automatically enable the part with a minimal number of external components and PCB routing. When using multiple PE25304 devices in parallel, all their EN pins must be connected to a single EN signal. [Figure 7](#) and [Figure 8](#) are scope plots that show the enable and disable behaviors.

Input under-voltage lockout (UVLO)

The PE25304 continuously monitors the V_{IN} input using a fixed under-voltage lockout (UVLO) threshold. The PE25304 is enabled when V_{IN} rises above 18.1V typical. When V_{IN} falls below the fixed under-voltage lockout threshold minus an additional 0.9V hysteresis, the charge pump switching is disabled.

Pre-charge operation

Before enabling the soft-start switching sequence, the PE25304 pre-charges the internal flying capacitors to make a balanced state based on the divider ratio. This is so that when the soft-start phase begins, the voltage across the capacitors is at their nominal voltage and known state. The adaptive pre-charge system takes pre-charging time, depending on the external voltages present on the circuit.

The output voltage cannot rise monotonically during the pre-charge period.

Soft-start operation

After the pre-charge phase completes, the device enters soft-start mode and charges the output capacitor at 134 mA typical value input current. It exits this state when the V_{OUT} voltage reaches the PGOOD V_{OUT} threshold. The PGOOD pin can go high at the same time. [Figure 7](#) shows a typical power-up sequence.

As the device goes through a soft-start sequence, do not apply load current to the device until the PGOOD pin is high. If a load is connected before this, the device does not start up. If the output current is loaded, V_{OUT} might not reach the target during the soft-start phase. As a result, the system detects a soft-start timeout, latches off the device, then requires the EN pin to be toggled to restart. The soft-start timeout is typically 100 ms. A similar situation can also occur if there is too much C_{OUT} capacitance.

PGOOD operation

The power good (PGOOD) pin is a bidirectional open drain pin. When the output voltage is above the PGOOD V_{OUT} threshold, the PGOOD pull-down field-effect transistor (FET) is turned off to allow the external pull-up resistor to pull up the node. The PGOOD pin must be pulled up externally. If another device or digital I/O is also pulling down on this pin, the PE25304 remains in soft-start mode, and high-power mode is not enabled. When the PE25304 allows PGOOD to be pulled high, the charge pump is ready to support the full load current.

When using multiple PE25304s in parallel, all their PGOOD pins must be connected. In this case, all PE25304 devices must complete soft start *before* PGOOD is asserted and full power operation is allowed. In the event of a fault in one or more parallel PE25304s, the PGOOD pin is pulled low by the faulted PE25304 device(s).

The PGOOD pin of a disabled device is NOT pulled low if the device is not enabled. In effect, if $EN = 0$, the PGOOD pin can be ignored. Table 6 lists the PGOOD pin operation and [Figure 15](#) shows the PGOOD sequence diagram. The V_{OUT} pre-biased condition would enable the PGOOD function to pull low if the part enabled.

Table 6. PGOOD pin operation

VIN	EN	State	PGOOD
$V_{IN} \leq V_{TH_UVH}$	X	X	X ⁽¹⁾
$V_{IN} > V_{TH_UVH}$	Low	Shutdown	High ⁽²⁾⁽³⁾⁽⁴⁾
$V_{IN} > V_{TH_UVH}$	High	After start-up and normal (fault free) operation	High ⁽⁵⁾
–	–	Others	Low



1. If $V_{IN} \leq UVLO$, PGOOD can be ignored.
2. Pulled high when the module is in stopped state shutdown.
3. The EN signal changes from high-to-low (shutdown period). It indicates low for 60 ms (typical). After that, PGOOD is pulled high.
4. If PGOOD is pulled up by divided V_{OUT} , it indicates low.
5. Indicates low during soft-start operation.

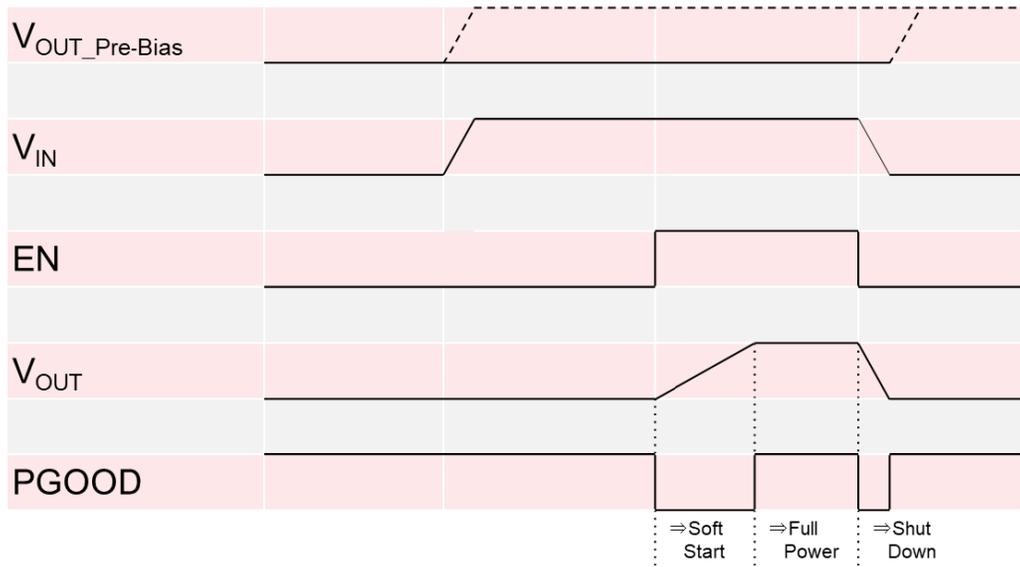


Figure 15. PGOOD sequence diagram

Figure 16 shows a PGOOD application circuit example. If there is no 3.3-5V rail, PGOOD can be pulled up by the divided V_{OUT} . Using 100 k Ω and 47 k Ω resistors with 1% tolerance for the V_{OUT} dividing resistors supports a wide V_{IN} range. In this case, the PGOOD voltage varies with the V_{OUT} voltage.

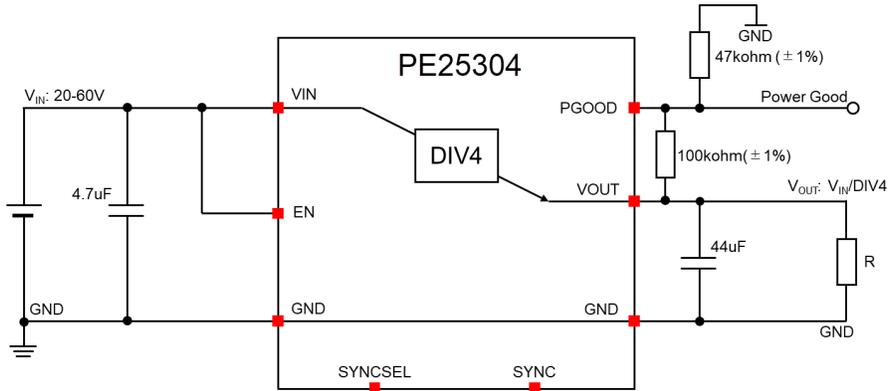


Figure 16. PGOOD application circuit

External and internal clock modes and the SYNCSEL pin

In most applications, the PE25304 operates using its internal oscillator. Table 7 lists the SYNC pin operation.

Table 7. SYNC pin operation

Detector	SYNC	Effect of fault
GND	Output	The internal clock is sent to the SYNC pin as an output.
Open	Input	An external clock can be applied to the sync input. If there is no external clock, the internal clock is used.

The charge pump operates at half the frequency of the SYNC pin input/output clock. Because the PE25304 internal components are optimized for efficiency with the internal oscillator frequency, do not inject an external clock for single-device applications. If configured to use an external clock (SYNCSEL = open circuit), and the external clock stops or is not present for any reason, an internal watchdog detects the missing clock and causes the PE25304 to use its internal clock source. When the expected external clock source resumes, the PE25304 reverts to using the external clock.

When the SYNCSEL pin is tied to GND, the internal clock is present on the SYNC pin.

Because the SYNC pin is high impedance and can be affected by external noise, if an external clock out function is not used in the application, leave the SYNCSEL to float and tie the SYNC pin to GND using a resistor.

For parallel operation, the SYNCSEL pin on one of the parallel devices must be GND to provide the clock for the other devices. Leave the other parallel devices floating to receive the shared clock to synchronize all the parallel devices.

Protections

 Protections are designed to prevent any damage or issues on the module as a best practice. This does not guarantee safety or no damages in your system. pSemi highly recommends having primary protection—such as adding a fuse—and regarding those protections as supportive functions in your systems. For more information, see [Fail-safe function](#).

The PE25304 is a high-power device. To protect systems and the PE25304 internal circuitry, multiple fault detection circuits are built in, as listed in Table 8. In each case, the response time is in microseconds (μs).

Table 8. Protections

Detector	Latched off or automatic retry	Effect of fault
Over temperature	Automatic retry	PGOOD goes low and the power stage switches off until the temperature reduces below the hysteresis threshold. At this point, the device automatically restarts. To automatically restart, the device must restart into no load.
V_{IN} under voltage	Automatic retry	PGOOD goes low and the charge pump is disabled until V_{IN} returns above the UVLO threshold and is enabled. To automatically restart, the device must restart into no load.
I_{OUT} over current	Automatic retry	If the load current exceeds the over-current limit, PGOOD goes low and the charge pump is disabled for a certain period to cool down. If the device is still over current after the cooldown period, after the cooldown period it automatically restarts.
I_{OUT} short circuit	Latched off	If the load current exceeds the short-current limit, the device is immediately latched off and shuts down. To restart the device, toggle EN.
Soft-start timeout	Latched off	If V_{OUT} does not reach the target voltage of V_{IN} divided by 4 within the soft-start timeout period, the device shuts down and EN must be toggled to restart it.
PGOOD held low	Automatic retry	If the charge pump is operating at full power and if PGOOD is pulled down externally, the device enters soft-start mode. If the PGOOD pin is held low for less than the soft-start period, the charge pump returns to full power operation. If the PGOOD pin is held low for longer than the soft-start duration, the charge pump completes a soft-start cycle before returning to normal operation and must not be loaded during this period.
V_{OUT} under voltage	Automatic retry	If the output of the device is under the V_{OUT} threshold, the PGOOD pin is pulled low. The device switches off and enters a cooldown period. After the cooldown period, the charge pump restarts into soft start mode.

V_{IN} under-voltage and thermal shutdown faults

The V_{IN} under-voltage and thermal shutdown faults are grouped because they have a similar effect on the charge pump. If either of these faults is present when the charge pump is first enabled, the charge pump cannot start up.

The charge pump holds in this state until both faults are clear, regardless of how long this takes.

The V_{IN} under-voltage and thermal shutdown faults are considered *persistent* because they hold the charge pump disabled until the fault clears.

In the case of V_{IN} under-voltage, it is unlikely that the charge pump can support the full load current when V_{IN} —and therefore V_{OUT} —is too low. Having the PE25304 or the load operating in this condition is not ideal, so the charge pump holds off waiting for V_{IN} to improve or recover.

An over-temperature fault is likely to occur only when the PE25304 is dissipating too much internal power, which normally results from another fault condition, such as an overload. In the event of over-temperature, the PE25304 could start to drift out of its guaranteed performance specifications, which would not be ideal for the system. To recover from over temperature, the power dissipation in the PE25304 must be reduced to lower the internal temperature.

When a V_{IN} under-voltage or over-temperature fault is detected during normal operation, the PE25304 enters a controlled shutdown sequence with an unlimited cool-down period. When the faults clear, the PE25304 enters a soft-start sequence.

I_{OUT} overcurrent protection

Over-current protection operates by sensing the V_{IN} current drain. The over-current protection trips when the PE25304 is operated outside the recommended operating conditions. Typically, the device trips when the output current exceeds 10A. The over-current protection has two separate protection methods:

- If the current exceeds the over-current protection threshold of 10A typical, then when triggered, the device enters a cool-down period and after this automatically restarts. During this time the PGOOD pin is pulled low.
- If the current exceeds 15A typical, the device immediately shuts down and latches off. During this time, the PGOOD pin is pulled low. To restart the device, toggle the EN pin.

The PE25304 reacts to an over-current fault by entering a controlled shutdown sequence. The device is then latched off until EN is toggled. After EN is toggled and the pre-charge is complete, the PE25304 enters a normal soft-start sequence and attempts to restart.

 Some persistent fault conditions could prevent the charge pump from restarting successfully, such as a hard fault to GND at V_{OUT} .

V_{OUT} under-voltage protection

The V_{OUT} under-voltage fault detector measures the value at V_{OUT} with the expected value derived from $V_{IN}/4$. pSemi designed the V_{OUT} under-voltage fault to be slow and represent an average value.

The V_{OUT} under-voltage flag trips when V_{OUT} goes below 80% of the target voltage (V_{OUT_UVP}). Choose external components so that the expected transient loads do not trip the V_{OUT_UVP} threshold. In effect, the application must ensure that the load dependency causes a less than 20% deviation from the nominal V_{OUT} .

Soft-start timeout

When the PE25304 first tries to supply power to the load, the power is limited by soft-start circuit. Using soft start has no significant side effects if the start-up is *normal*.

If the PE25304 starts up into a fault, the soft start helps to manage the power supplied to the fault and limits the power dissipation in the PE25304. In normal, fault-free operation, the soft-start timeout is invisible if the soft-start current can ramp V_{OUT} to the target voltage within 100 ms. In the case of a fault, the soft-start timeout occurs when V_{OUT} does not ramp to the target voltage within the expected time. In this case, the soft-start timeout stops power to the load and the PE25304 enters a controlled shutdown sequence. The device then latches off, and EN must be toggled to restart it.

PGOOD low detection

In a standalone PE25304 implementation, the PGOOD signal is likely to have only one driver. When the PE25304 is ready for full power, PGOOD goes high and stays high for as long as the single PE25304 remains enabled and fault-free.

In parallel operation, the PGOOD signal must be connected in a wired OR configuration with the other devices. When all devices are ready for full power, the PGOOD signal goes high. In the event of a fault, the PGOOD signal is pulled low and switches off all the parallel devices. To restart the devices, toggle EN.

Application information

The charge-pump based DC-DC converter is a high efficiency bus converter that does not have regulation capability. Because of its architecture, there are some differences from conventional inductive buck converters. Some of the behaviors could cause critical issues if not handled correctly.

Charge pump architecture basics

A charge pump is a capacitive voltage converter configured by multiple switches and capacitors, as shown in Figure 17, which shows a divide-by-four configuration.

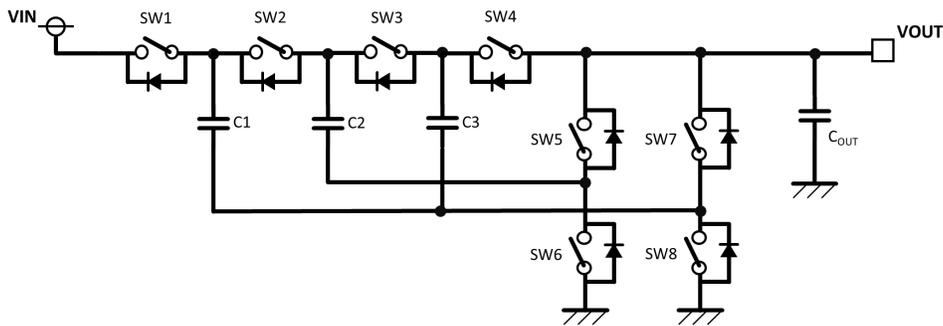


Figure 17. Divide-by-four charge pump configuration

A charge pump usually has two main switch states. The PE25304 also has the two main switch states shown in Figure 18 and Figure 19.

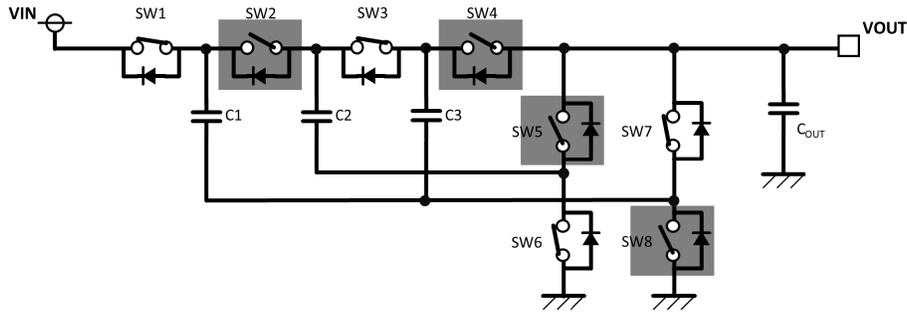


Figure 18. Divide-by-four charge pump phase one configuration

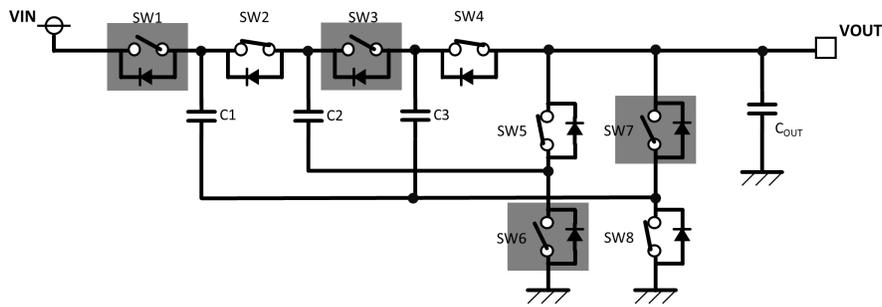


Figure 19. Divide-by-four charge pump phase two configuration

In phase one:

- Flying capacitor C1 connects between V_{IN} and V_{OUT} .
- Flying capacitors C2 and C3 connect between V_{OUT} and GND.

In phase two:

- Flying capacitors C1 and C2 connect between V_{OUT} and GND.
- Flying capacitor C3 connects between V_{OUT} and GND.

Figure 21 shows these two states of capacitor connection and charged voltage relationship. After the charge pump finishes soft start, each capacitor has the $V_{IN}/4$, $V_{IN} \times 2/4$, and $V_{IN} \times 3/4$ voltage. This voltage is maintained to keep switching between phases one and two. To improve the charge pump efficiency, increase the flying capacitor capacitance. Also, minimize the switch resistance and parasitic resistance. Because the PE25304 has optimized C_{FLY} , power switch resistance, and routing parasitic resistance, there is no need to care about such a detail.

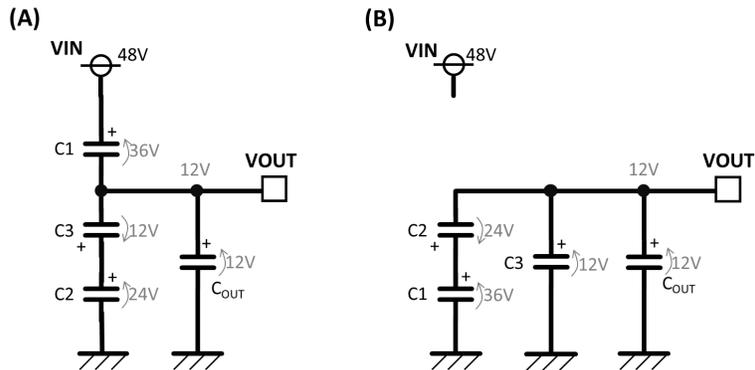


Figure 20. Divide-by-four charge pump capacitor connection

The PE25304 is based around a high efficiency, charge-pump based DC-DC converter with an unregulated output voltage. Because of this architecture, some important characteristics are different from conventional inductive buck converters. To avoid damage to the system or the device, it is important to understand some of the key architecture differences compared to conventional buck converters. For more information, see [Charge Pump Architecture and Important Notice](#).

Application performance

Figure 21–Figure 24 show the typical performance at $T_A = 25\text{ }^\circ\text{C}$ based in the application board in [Figure 26](#).

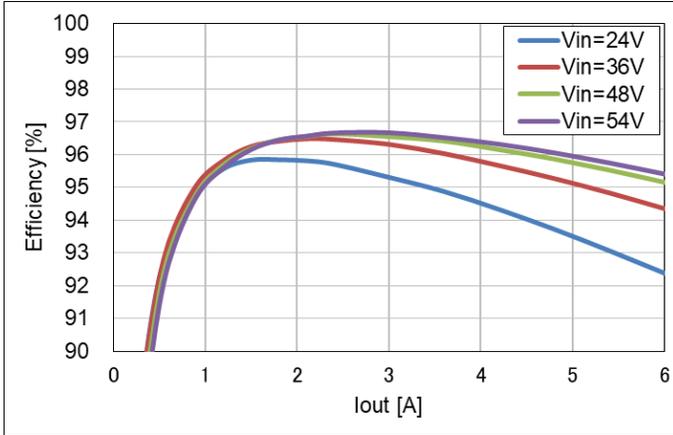


Figure 21. Efficiency

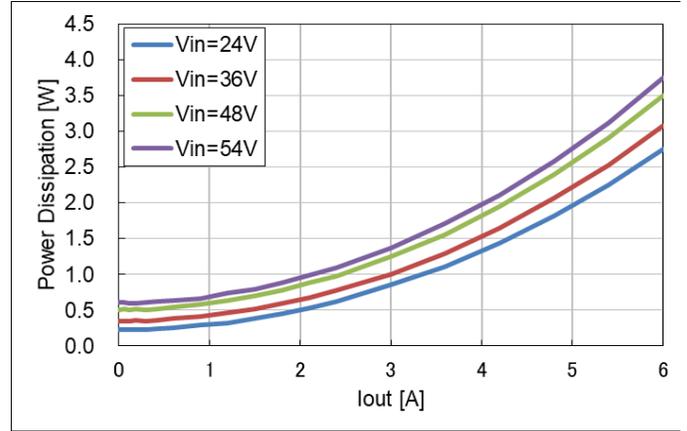


Figure 22. Power dissipation

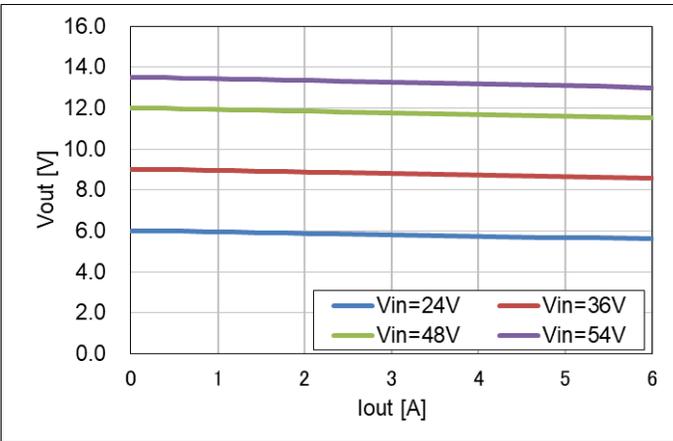


Figure 23. V_{OUT} load regulation

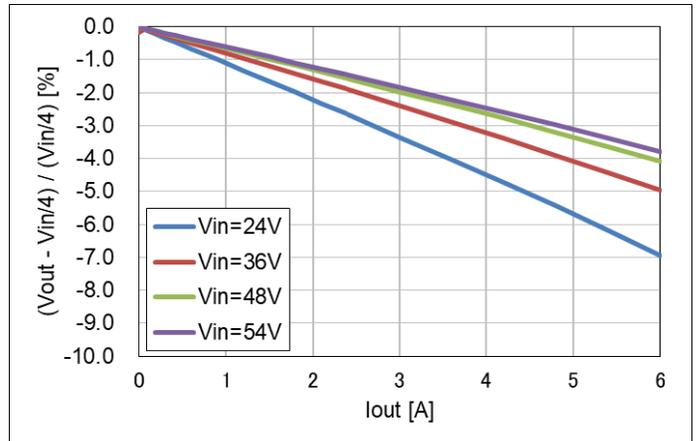


Figure 24. V_{OUT} drop ratio

Application schematic

Figure 25 shows the PE25304 standalone schematic.

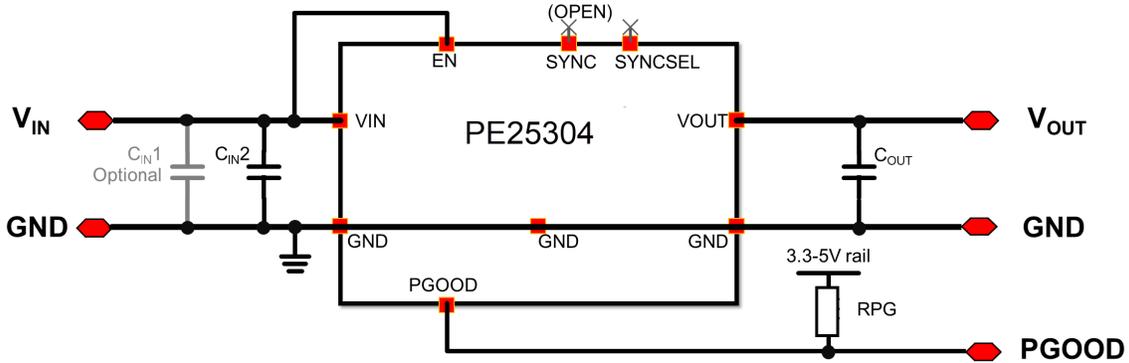


Figure 25. Application schematic

Application circuit parts list

Table 9 lists the standard application circuit components. Choose components based on the system requirements, such as voltage and temperature.

Table 9. Application circuit parts list

Reference	Value	Description	Part number
C _{IN1}	100 μF	Electrolytic capacitor, optional(*)	—
C _{IN2}	4.7 μF	Input capacitor, ceramic, 4.7 μF, 100V, ±10%, X7S	Murata GRM31CC72A475KE11
C _{OUT}	22 μF × two pieces	Input capacitor, ceramic, 22 μF, 25V, ±20%, X7S	Murata GRM31CC71E226ME15
RPG	10 kΩ	Pull-up resistor for PGOOD indication, chip resistor, 10 kΩ, 0.10W, ±5%	KOA RK73B1ETTP103J

i * If there is a non-negligible parasitic impedance between the power supply and the converter—such as during evaluation—optional input capacitor C_{IN1} might be required to reduce the impedance. The 100 μF value shown here is an example, so consider the optimum value for your application. This capacitor is usually an aluminum electrolytic type, and it is not necessary to place the capacitor near the input terminal of the converter.

Application board example

All performance data in this data sheet was measured using this board.

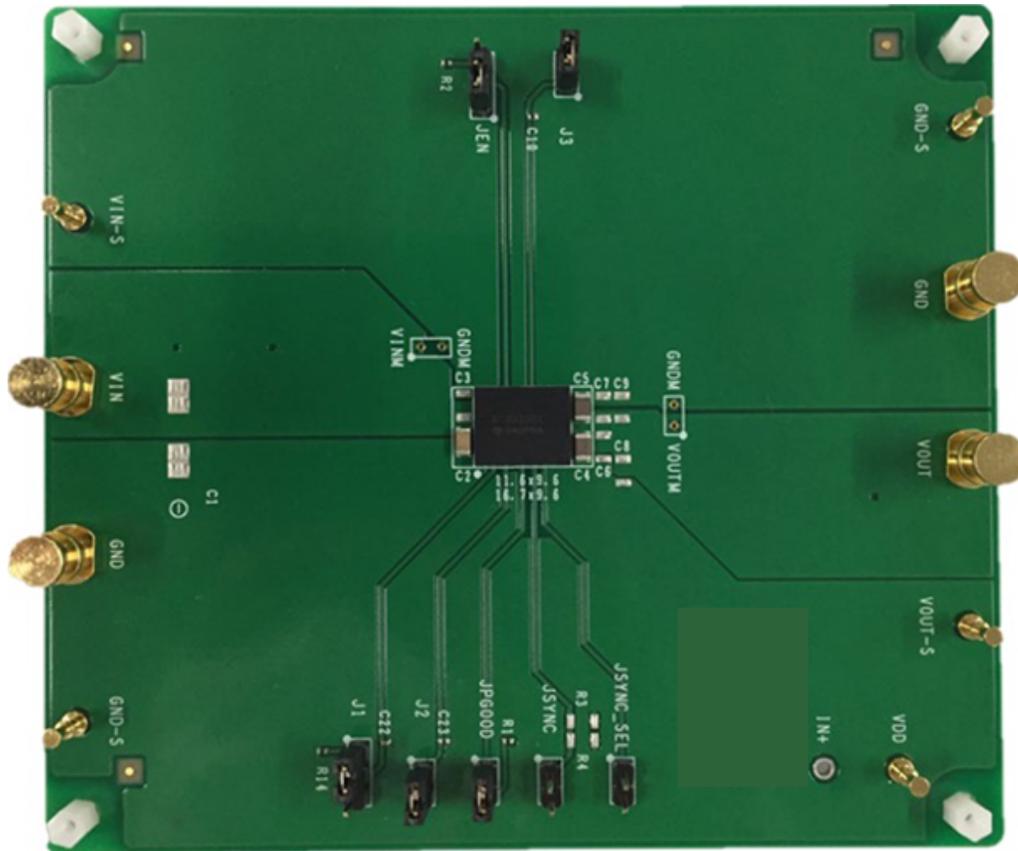


Figure 26. Application board example

Component selection

Input capacitor

The input capacitor connected between V_{IN} and GND reduces the ripple on V_{IN} . Place the input capacitor as close to the device as possible to reduce any parasitic inductance effects. The voltage rating of the capacitor must be at least as high as the absolute maximum voltage rating for the system and consider the effect of the capacitor voltage coefficient to determine the effective capacitance value at the applied V_{IN} . Because the charge pump is not a regulator, ripple voltage on V_{IN} could affect the output voltage.

Output capacitor

The output capacitor reduces the ripple on V_{OUT} . The higher the capacitor value, the lower the ripple at V_{OUT} becomes. Increasing the output capacitor value increases the soft-start duration and could cause the module to time out during soft-start. Take this into account when considering the C_{OUT} value for your system. Following the system's input capacitance would be the C_{OUT} of the PE25304.

Input fuse

Certain applications or safety agencies might require fuses at the inputs of power conversion components. Fuses must also be used when there is the possibility of sustained input voltage reversal, which is not current limited. For the greatest safety, pSemi recommends a fast-blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with your applicable safety standards.

Application schematic with a secondary

Figure 27 shows an example PE25304 schematic with a secondary.

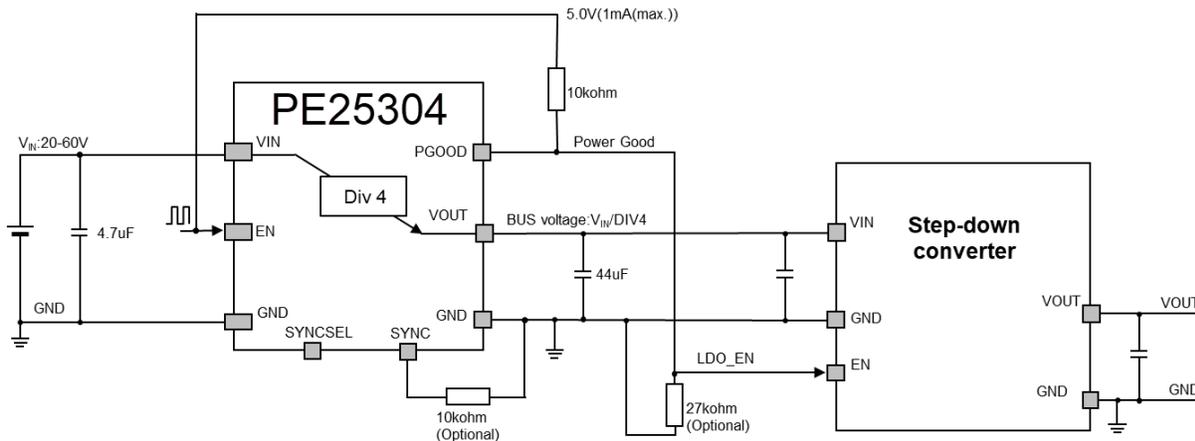


Figure 27. Application schematic with a secondary

Parallel operation

The PE25304 can run in parallel in a multi-device configuration as shown in [Figure 28](#) to increase the output power. In parallel operation mode, pay careful attention to some important things described in this section.

Current and thermal balance

As with standard inductive DC-DC converters, a paralleled charge pump must also take care of the current and thermal balance. The PE25304 divides the output voltage from input voltage. The output voltage relates to the input voltage, and the output voltage is not regulated. Therefore, the charge pump provides natural droop based on the equivalent output resistance (R_{OUT}).

When the load applied to the paralleled charge pump modules, each output voltage of the modules starts to droop. The voltage drop from the ideal output voltage (V_{IN}/DIV) is decided by $(R_{OUT} + \text{parasitic resistance}) \times I_{OUT}$. And the load current of each module is decided by the relationship of the $R_{OUT} + \text{parasitic resistance}$. For the charge pumps to effectively load share—and to reduce the parasitic resistance variation of the input and output power tracks—pay close attention to the layout.

The PE25304 is capable of up to 6A unless limited by other factors. Therefore, when in parallel operation, an imbalance in the load sharing caused by parasitic impedances can result in one module current limiting before another. This could restrict the total amount of power available to the system.

The power loss generated by the module results in heat rise in the module to maintain load sharing so that the modules must share the same thermal structure.

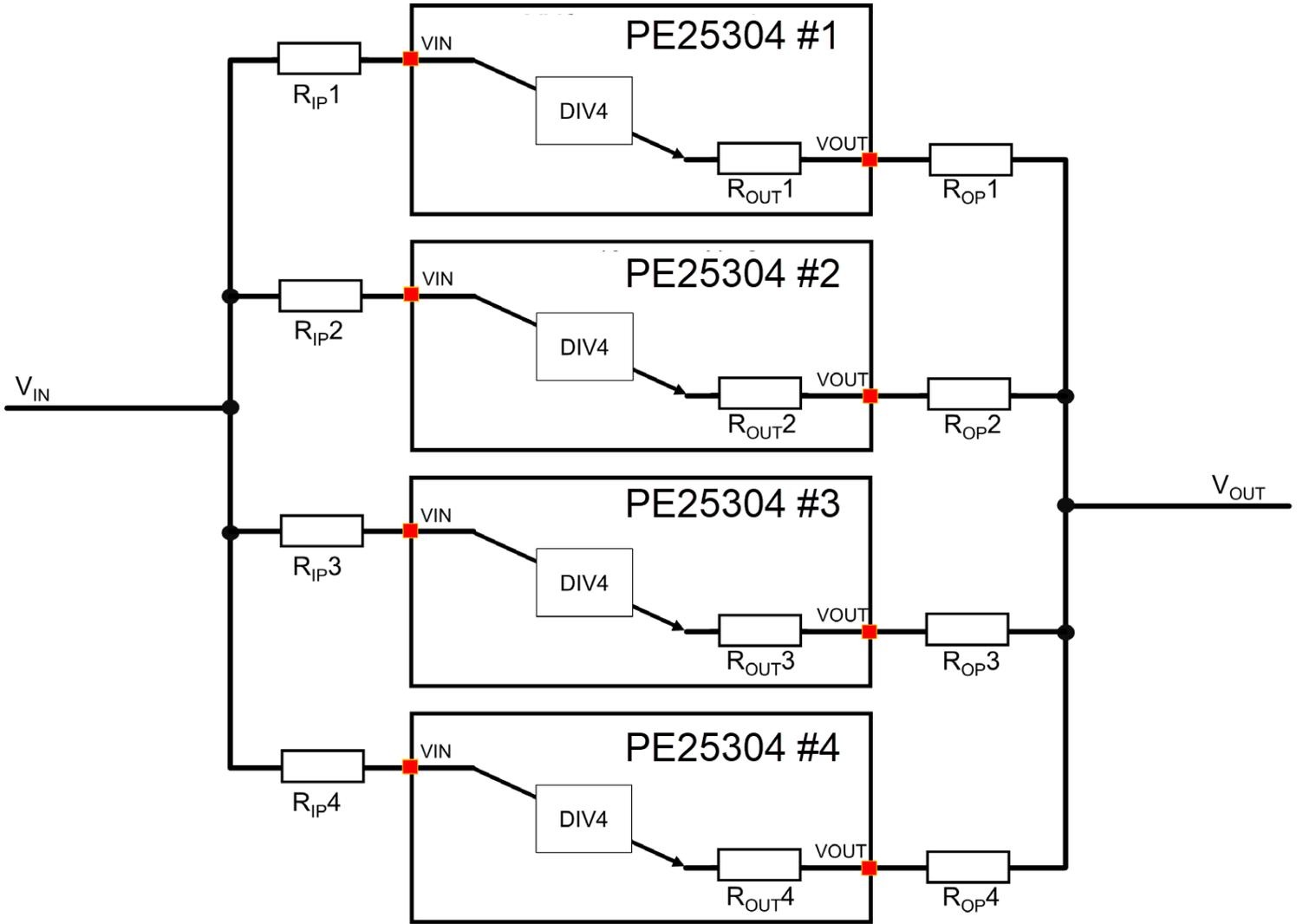


Figure 28. Multi-module current sharing

Pin connections for parallel operation

Pin connection limitation is slightly different from the single module operation. When following these instructions, see Figure 29.

The PGOOD outputs must be pulled up together and combined in a wired OR configuration. The load following the charge pump must not be switched on until all PGOOD outputs are high, and the load must be immediately switched off if any of the PGOOD outputs switch low after starting up.

Ground the SYNCSEL pin on one of the paralleled modules to provide the clock for the others. Leave the other paralleled modules floating to receive and synchronize using the shared clock.

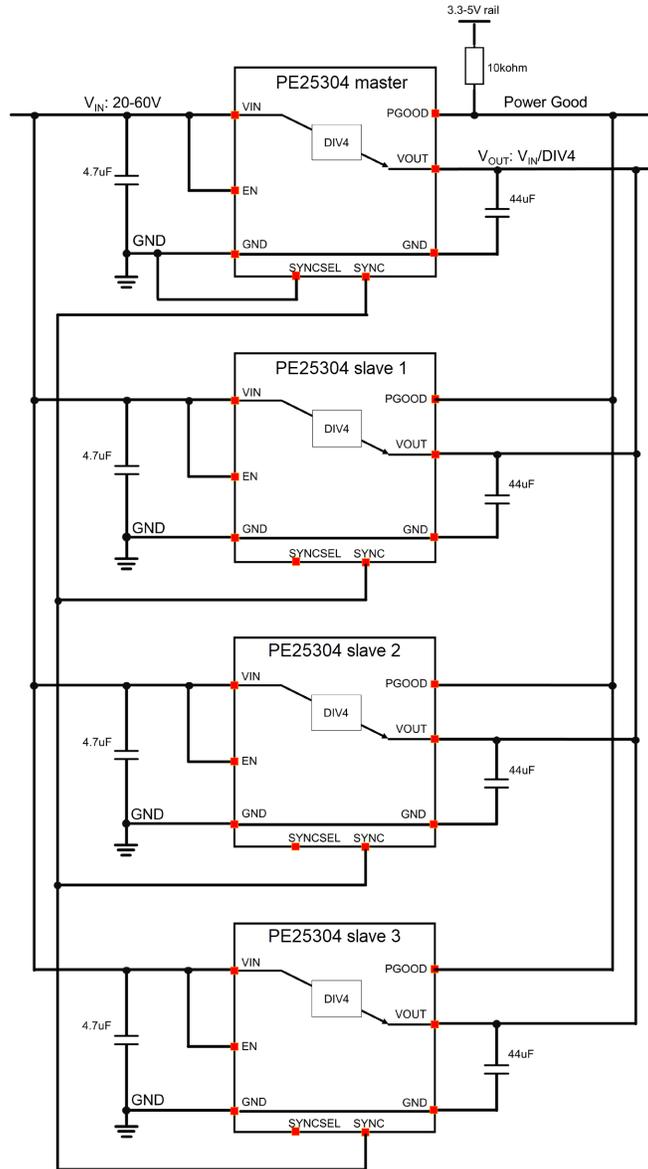


Figure 29. Multi-module application circuit

Charge pump architecture and important notice

The PE25304 uses multiple low-impedance switches to take advantage of the higher energy density available in capacitors—as compared to inductors—to transfer power. The keys to optimizing charge pump efficiency include the following:

- Reduce charge redistribution losses, and
- Minimize thermal losses

The PE25304 reduces the charge redistribution loss with patented, *almost loss-less*, architectures. The thermal losses are minimized by using lower voltage-rated (internal) power FETs which take advantage of the reduced voltage as the input supply is divided.

These two key features make the PE25304 very efficient. In exchange for the high efficiency and to avoid permanent damage to the device, pay close attention to the differences to conventional buck converters.

- Figure 30 shows an inductive regulator called a buck converter. The inductor between the switching node to VOUT would prevent a transient change of current if a hard short happened.
- For Figure 31, it would be high di/dt condition with a hard short because the PE25304 does not have a large inductor but has the low impedance of power FETs.

In general, the inductance would be reduced by the current slope of the inductor, and the impedance of the power FETs would be reduced by the peak current. For more information, see [Hard short-circuit condition](#).

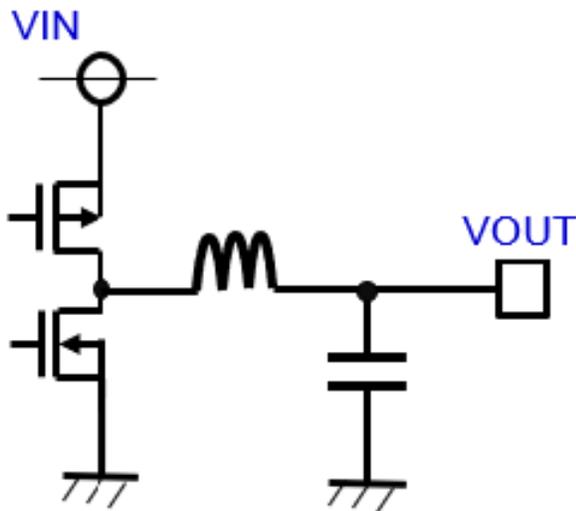


Figure 30. Inductive regulator

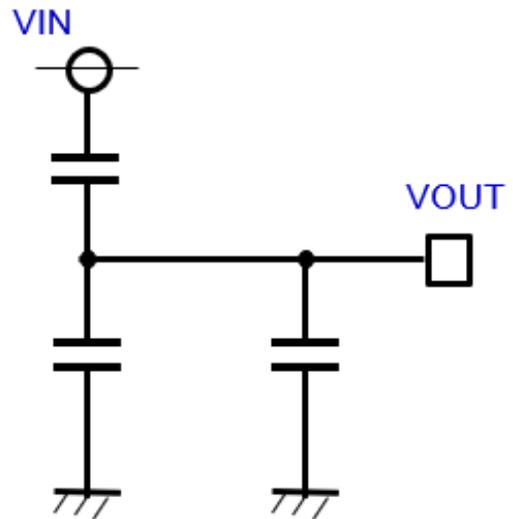


Figure 31. Charge pump

Hard short-circuit condition

The PE25304 is a capacitive DC-DC converter that has low inductance at the output to optimize its efficiency. As a result of the low output inductance, a hard short at this product output can result in a di/dt condition which can be much higher than a conventional, inductive buck converter would allow.

The PE25304 has a built-in output current protection. However, hard output short circuits with very low impedance could cause permanent damage to the device and must therefore be avoided. If such faults must be considered, it might be necessary to add primary protection (external to the device) to ensure adequate protection of the device and if the condition might be varied over environment and use cases.

Soft start and capacitor charge balancing

The charge pump is an open-loop capacitive DC-DC converter. The output voltage is generated using “flying” capacitors (C_{FLY}), which move the charge from one voltage level to another. The voltage across the flying capacitors in normal operation is limited to V_{OUT} . The voltage balancing between and across the flying capacitors is important to maintain stability. The pSemi charge pump has several internal states which specifically enhance stability, including *pre-charge* and *soft start*.

- During pre-charge, each of the C_{FLY} capacitors is charged to the appropriate DC voltage bias level (depending on V_{OUT}) to ensure a balanced state at start-up.
- During soft start, the charge pump starts switching with a controlled current (134 mA typical input current) to ramp V_{OUT} to the target voltage, depending on V_{IN} .

The controlled start-up avoids an inrush of current and EMI issues during turn on while ensuring V_{OUT} reaches the PGOOD V_{OUT} threshold before full-power operation is enabled. As a further safety measure, the soft-start time is also monitored to ensure that the system does not contain any unexpected leakage paths, such as V_{OUT} or C_{FLY} shorts. As a result of the limited soft-start current, the system does not support starting up into a full power load. A high on the PGOOD pin indicates that the system is ready for full load after the soft start has finished and V_{OUT} has reached the PGOOD V_{OUT} threshold. The soft-start timeout protection also means that the maximum output capacitance must be limited to ensure a reliable startup. Increasing C_{OUT} beyond the recommended level could cause the charge pump to not start up.

A current-limited soft-start consumes larger power than standard operation. Therefore, any temperature rise during the soft-start condition must be controlled.

Reverse-direction current flow and operation

The PE25304 is designed to divide the input voltage by four. Parasitic diodes, which are parts of the internal power switches, are based on the power flow from V_{IN} to V_{OUT} . To avoid forward bias of the internal diodes—and potentially damaging high current levels—reverse power flow (from V_{OUT} to V_{IN}) must be avoided. Inductive buck converters are protected from very high di/dt conditions by the filtering effect of the power inductor. To optimize efficiency, the PE25304 has much lower inductance, very low-impedance internal switches, and reverse diodes. Reverse power flow could be triggered if V_{OUT} is greater than $V_{IN}/4$.

The PE25304 is designed to safely start up into a pre-biased output if the condition $V_{OUT} \leq V_{IN}/4$ is met. Do not start up into a pre-biased output with the condition $V_{OUT} > V_{IN}/4$.

One condition which could cause reverse power flow is a rapid decrease in the V_{IN} voltage level while the PE25304 remains enabled. It could also result in an unexpected shutdown. To avoid them, do not reduce V_{IN} rapidly while the PE25304 is enabled. Also, reducing V_{IN} while $EN = 0$ and then re-enabling again with a lower V_{IN} could result in reverse power flow if the V_{OUT} capacitor still holds the previous V_{OUT} charge level.

Input voltage transient

The PE25304 over-current protection operates by sensing the V_{IN} current drain. A rapid increase in V_{IN} generates a voltage difference between the input and the C_{FLY} , resulting in an excessive input current, which could result in an unexpected shutdown. To avoid it, do not increase V_{IN} rapidly while the PE25304 is enabled.

Packaging information

This section provides packaging data, including the moisture sensitivity level, package drawing, package marking, and tape-and-reel information.

Moisture sensitivity level

The PE25304 moisture sensitivity level rating for the 52-pin 11.5 × 9.5 × 2.0 mm LGA package is MSL3.

Package drawing

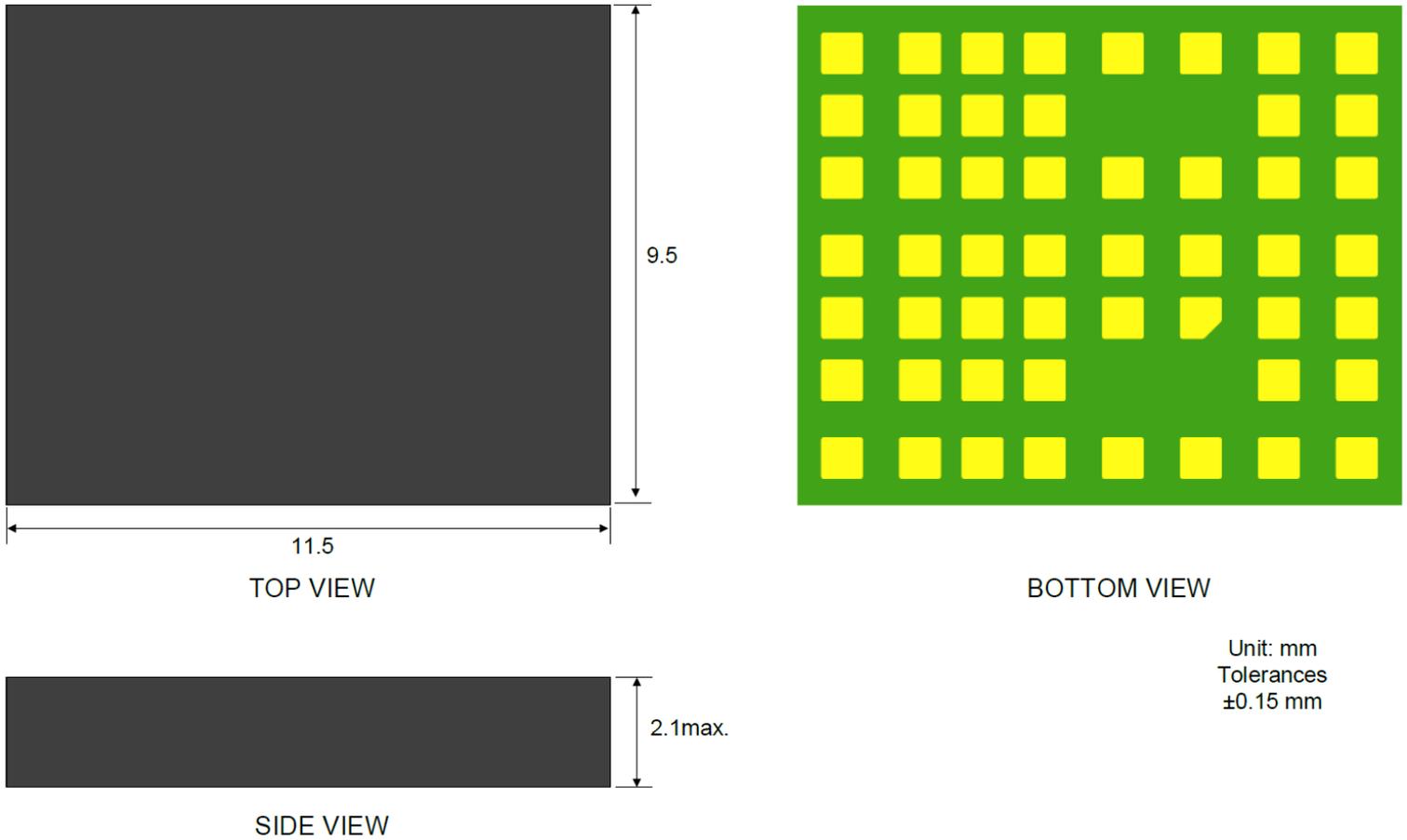


Figure 32. Package drawing

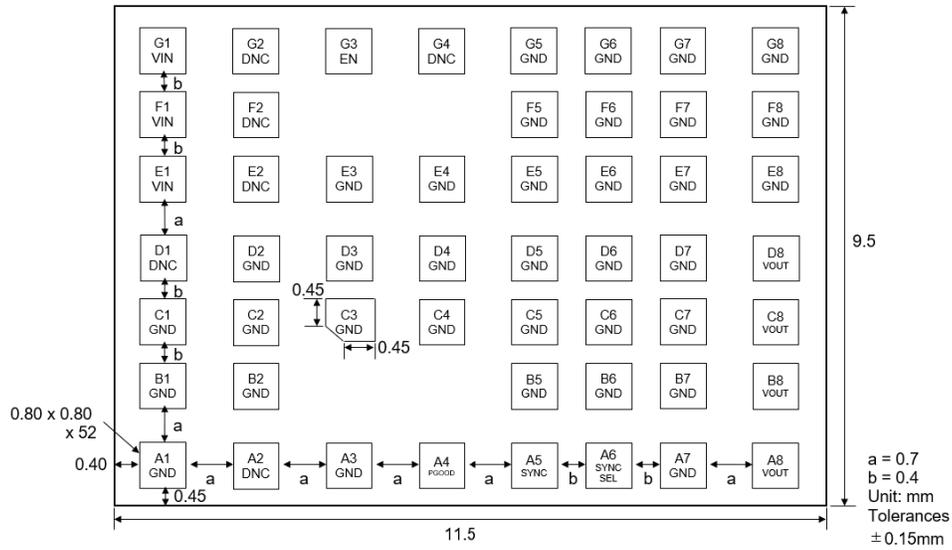


Figure 33. Package footprint and dimensions, top view

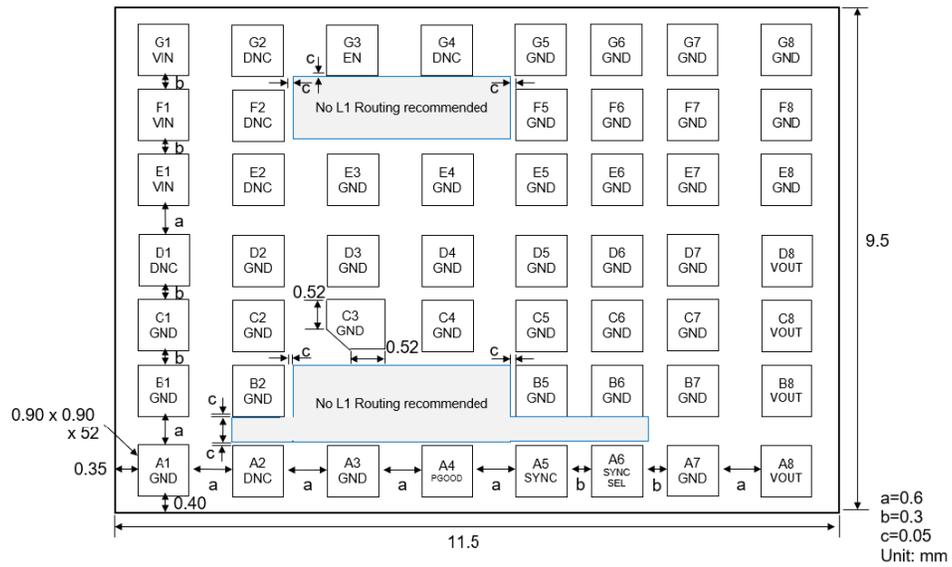


Figure 34. Recommended board land pattern and dimensions, top view

Top-marking specification

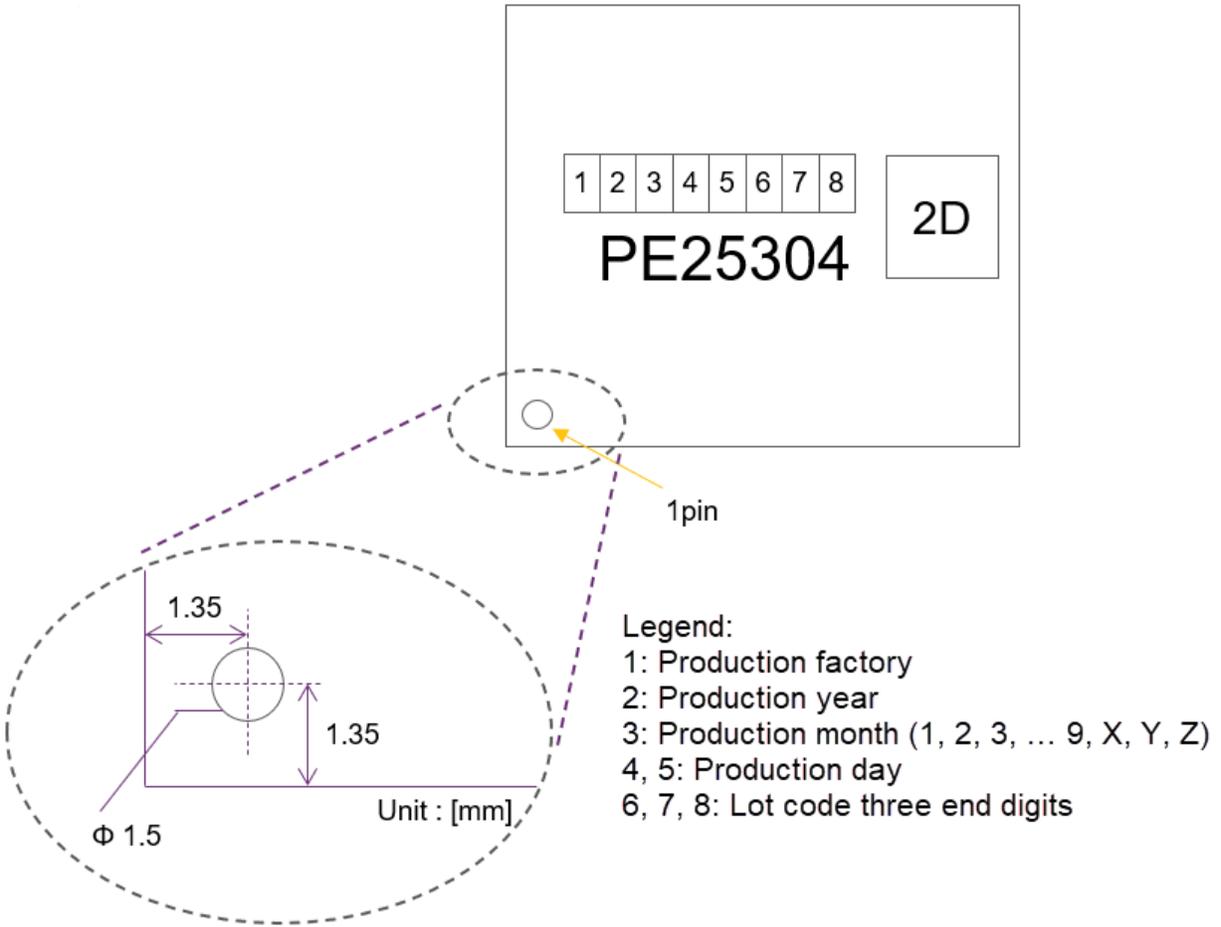


Figure 35. Top-marking specification

Tape and reel specification

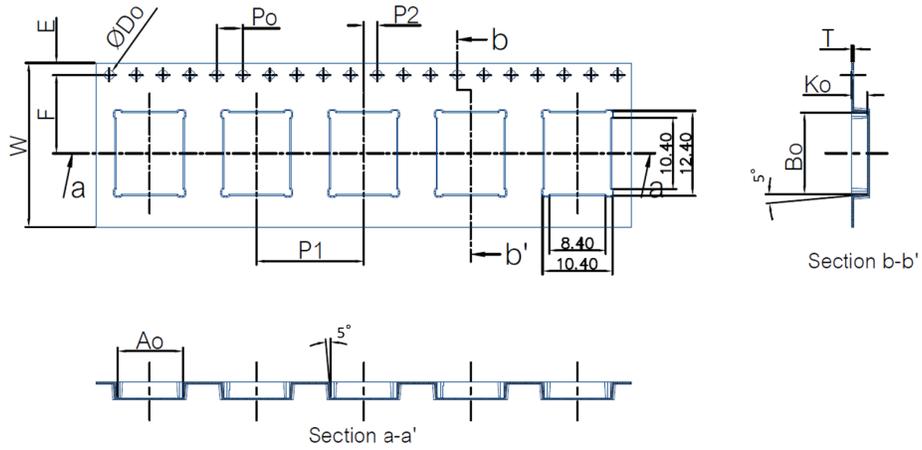


Figure 36. Tape dimensions

Table 10. Tape dimensions

Symbol	Value	Tolerance	Unit
A0	9.90	±0.10	mm
B0	11.90		
K0	2.30		
P1	16.00		
ØD0	1.50	+0.10/-0.00	
ØD1	-		
P0	4.00	±0.10	
P2	2.00		
E	1.75		
SO	-		
F	11.50		
W	24.00	+0.30/-0.10	
T	0.30	±0.05	

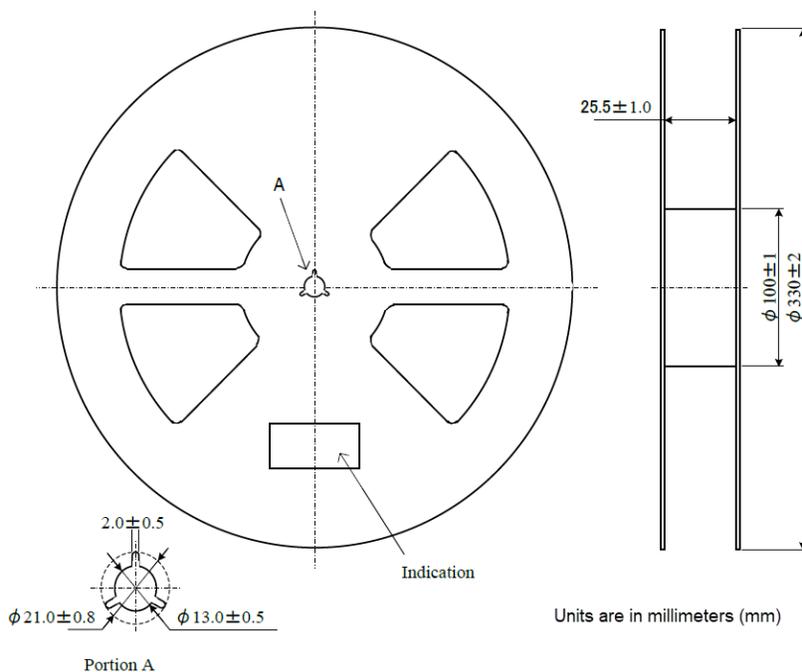


Figure 37. Reel dimensions

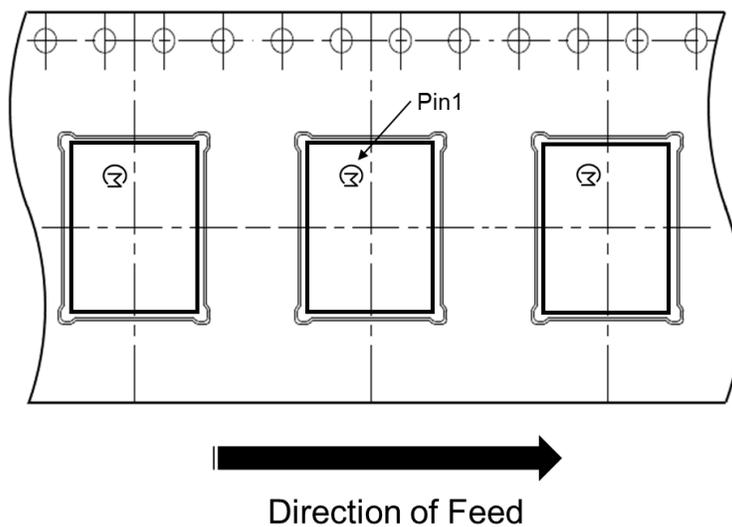


Figure 38. Module orientation in the tape

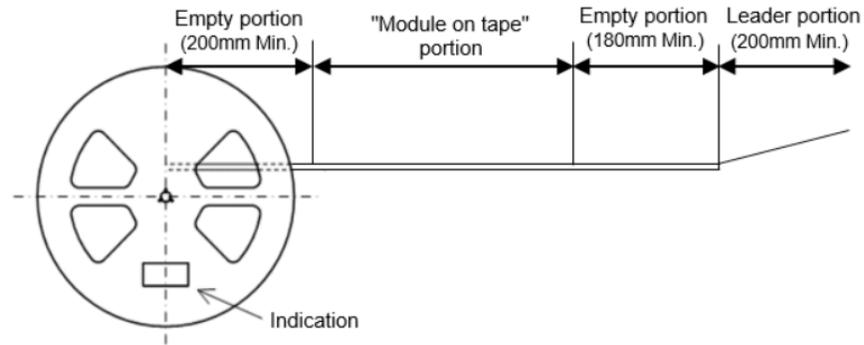


Figure 39. Taping specification

- The adhesive strength of the protective tape is within 0.3-1.0N.
- Each reel contains 400 units.
- Each reel is set in moisture-proof packaging because of MSL3.
- No vacant pockets in the "Module on tape" portion.
- The reel is labeled with the pSemi part number and quantity.
- The reel color is not specified.

Soldering guidelines

When installing the DC-DC converter, follow the specifications in Table 11. These specifications can vary, depending on the type of solder used. Exceeding these specifications could cause damage to the product. Because your production environment could differ, thoroughly review these guidelines with your process engineers. This product can be reflowed twice.

Table 11. Reflow solder operations for surface-mount products

For Sn/Ag/Cu-based solders	
Preheat temperature	Less than 1 °C per second
Time over liquidus	45–75 seconds
Maximum peak temperature	260 °C
Cooling rate	Less than 3 °C per second

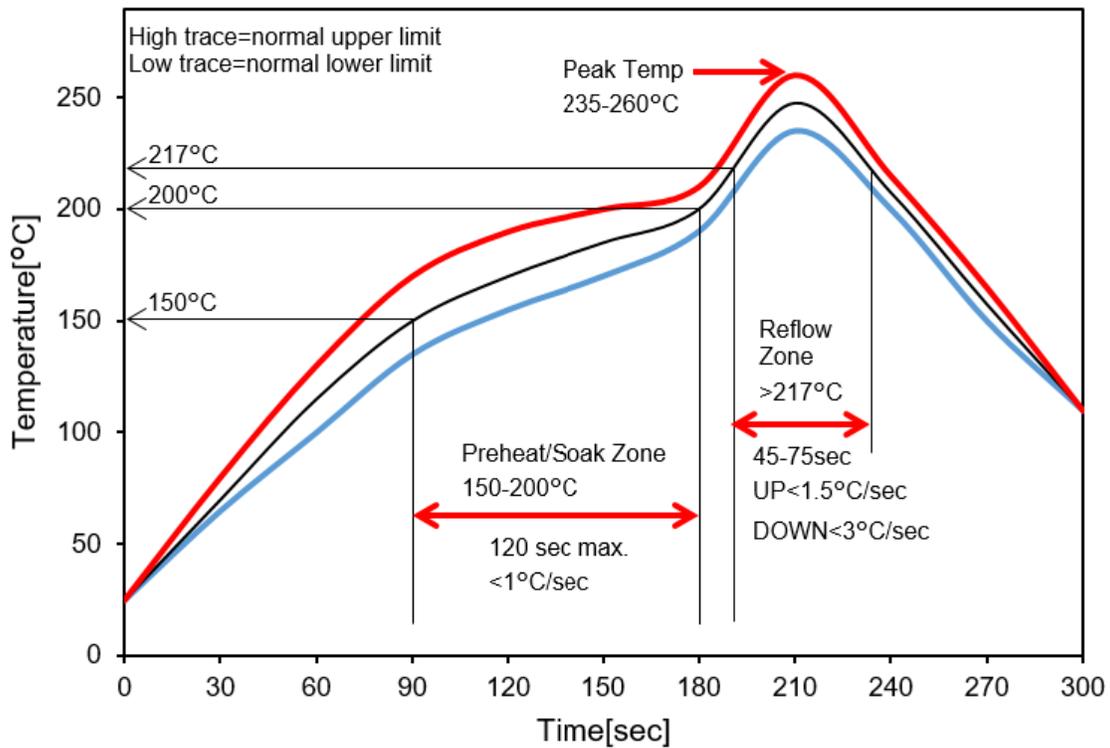


Figure 40. Sn/Ag/Cu solder reflow profile

Fail-safe function

To prevent secondary damage in the unlikely event of an abnormality or malfunction in our product, add a proper fail-safe function to your finished product.

Connect the input terminal by the right polarity. If the connection is incorrect, it could damage the DC-DC converter. If the DC-DC converter inside is damaged, an input over-current could flow. To protect this, add a diode and fuse as shown in Figure 40. Select the diode and fuse after you confirm the operation.

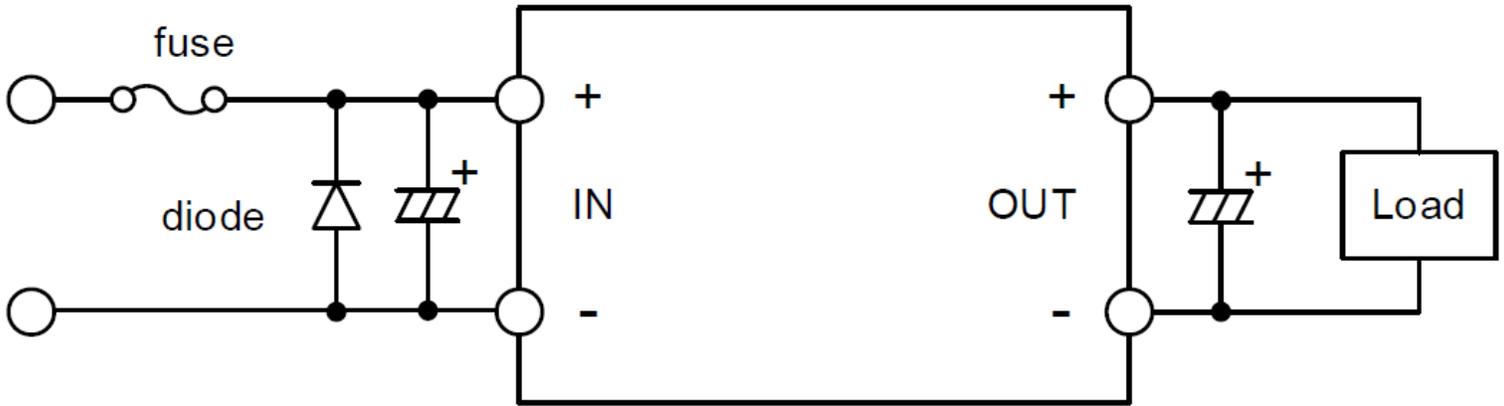


Figure 41. Example circuit with a diode and fuse.

Ordering information

Order code	Description	Packaging	Shipping method
PE25304A-P	PE25304 ultra-thin, high efficiency, 72W, DC-DC converter module	11.5 x 9.5 x 2.0 mm LGA	400 units/T&R
EK25304-01	PE25304 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com .

Contact and legal information

Sales contact	For additional information, contact Sales at sales@psemi.com .
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Patent statement	pSemi products are protected under one or more of the following U.S. patents: http://patents.psemi.com

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