

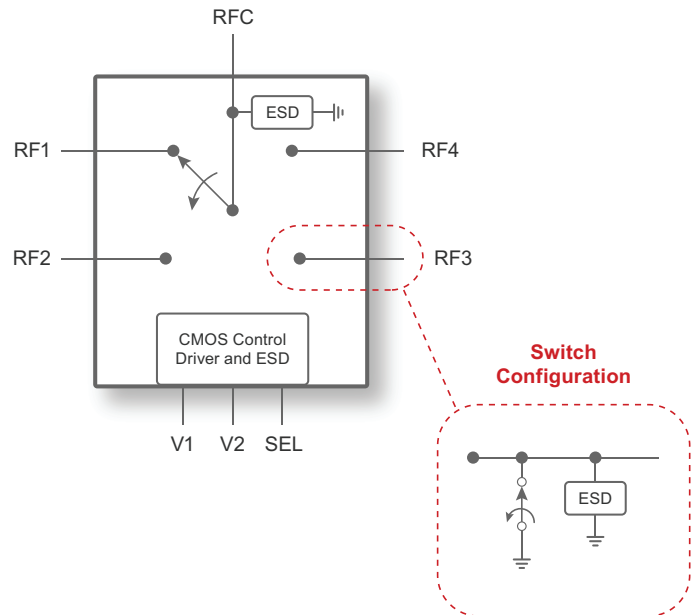
## Features

- Low insertion loss:
  - 0.42 dB at 2.6 GHz
  - 0.6 dB at 3.8 GHz
- High linearity IIP3: 88.5 dBm
- High power handling: 39.5 dBm RMS with 11 dB PAR
- Operating temperature: +115 °C
- Packaging: 20-lead 4 × 4 mm LGA

## Applications

- Analog hybrid beamforming RF front end
- 5G massive MIMO active antenna system (AAS)
- 4G/4.5G TD-LTE macro/micro cell/RRH

Figure 1 • PE42448 Functional Diagram



## Product Description

The PE42448 is a HaRP™ technology-enhanced SP4T RF switch that supports a frequency range from 10 MHz to 6 GHz. It delivers extremely low insertion loss and high linearity with high input power handling capability making this device ideal for hybrid analog beamforming and in 5G massive multi-input, multi-output (MIMO) applications. No blocking capacitors are required if no DC voltage is present on the RF ports.

The PE42448 is manufactured on pSemi's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology.

## Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in **Table 1** could cause permanent damage. Restrict operation to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

### ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

### Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

**Table 1 • PE42448 Absolute Maximum Ratings**

Parameter or Condition	Min	Max	Unit
VDD positive supply voltage	-0.3	5.5	V
Digital input voltage	-0.3	3.6	V
Storage temperature	-45	150	°C
ESD voltage HBM, all pins <sup>(1)</sup>	–	1500	V
ESD voltage, CDM, all pins <sup>(2)</sup>	–	1000	V
Thermal resistance: <sup>(3)</sup> Junction to base bottom Junction to case top	– –	39 10	°C/W
Maximum junction temperature <sup>(3)</sup>	–	150	°C
Power handling: 9W average power with following condition at same time: Within operating temperature range. 20 MHz TD-LTE signal with 11 dB PAR, duty cycle 8.8 ms, 88%	–	9	W
No damage power handling requirement: Average power 42.5 dBm; peak power 52 dBm; keep 10s in one time; frequency is one time/month; total 120 times in 10 years; lifetime.	–	42.5	dBm
<b>Notes:</b> 1) Human body model (MIL-STD 883 Method 3015). 2) Charged device model (JEDEC JESD22-C101). 3) Maximum junction temperature $\leq 115^{\circ}\text{C} + (\text{power dissipation of insertion loss-induced power}) \times \text{thermal resistance}$ .			

## Recommended Operating Conditions

**Table 2** lists the PE42448 recommending operating conditions. Do not operate the device outside the operating conditions listed below.

*Table 2 • PE42448 Recommended Operating Conditions*

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage	–	4.5	5	5.5	V
Supply current	VDD = 5V	–	75	200	μA
Digital input leakage current	–	–	1	2	μA
Operating temperature range	–	-40	25	115	°C
Switching pins logic levels, 1.8V JEDEC compliant	Logic low	0	–	0.63	V
	Logic high	1.17	1.8	3.6	

## Electrical Specifications

**Table 3** lists the PE42448 key electrical specifications at +25 °C  $T_{CASE}$  and  $V_{DD} = 5V$  ( $Z_S = Z_L = 50\Omega$ ), unless otherwise specified.

*Table 3 • PE42448 Electrical Specifications*

Parameter	Condition	Min	Typ	Max	Unit
Frequency range	–	0.01	–	6	GHz
Port impedance	–	–	50	–	$\Omega$
Insertion loss <sup>(*)</sup>	Frequency range: 0.01–0.52 GHz	–	0.25	0.35	dB
	Frequency range: 0.52–1 GHz	–	0.29	0.40	
	Frequency range: 1–2.3 GHz	–	0.38	0.60	
	Frequency range: 2.3–2.7 GHz	–	0.42	0.60	
	Frequency range: 3.3–3.8 GHz	–	0.61	0.85	
	Frequency range: 3.8–5 GHz	–	1.11	1.55	
	Frequency range: 5–6 GHz	–	2.13	3.00	
Return loss <sup>(*)</sup>	Frequency range: 0.01–0.52 GHz	–	40.0	–	dB
	Frequency range: 0.52–1 GHz	–	30.0	–	
	Frequency range: 1–2.3 GHz	–	22.0	–	
	Frequency range: 2.3–2.7 GHz	–	20.0	–	
	Frequency range: 3.3–3.8 GHz	–	15.0	–	
	Frequency range: 3.8–5 GHz	–	10.0	–	
	Frequency range: 5–6 GHz	–	7.0	–	
Isolation <sup>(*)</sup>	Frequency range: 0.01–0.52 GHz	43.0	45.0	–	dB
	Frequency range: 0.52–1 GHz	37.0	39.0	–	
	Frequency range: 1–2.3 GHz	29.0	30.0	–	
	Frequency range: 2.3–2.7 GHz	28.0	29.0	–	
	Frequency range: 3.3–3.8 GHz	24.0	25.0	–	
	Frequency range: 3.8–5 GHz	19.0	20.0	–	
	Frequency range: 5–6 GHz	16.0	18.0	–	
Input IP3 <sup>(*)</sup>	Two-tone CW input power $\leq 31$ dBm continuous wave per tone. Frequency range: 2.3–2.7 GHz	87.5	88.5	–	dBm
	Two-tone CW input power $\leq 34$ dBm continuous wave per tone. Frequency range: 3.3–5 GHz	81.0	84.0	–	
Second harmonic <sup>(*)</sup>	Single-tone CW input power = 34 dBm Frequency range: 2.3–2.7 GHz	–	-118.0	-108.0	dBc
	Single-tone CW input power = 37 dBm Frequency range: 3.3–5 GHz	–	-112.0	-105.0	

Table 3 • PE42448 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Third harmonic <sup>(*)</sup>	Single-tone CW input power = 34 dBm Frequency range: 2.3–2.7 GHz	–	-112.0	-104.0	dBc
	Single-tone CW input power = 37 dBm Frequency range: 3.3–5 GHz	–	-108.0	-99.0	
Relative phase error <sup>(*)</sup>	Relative phase error for a single port Frequency range: 0.01–0.52 GHz	–	–	±0.3	deg
	Relative phase error for a single port Frequency range: 0.52–1 GHz	–	–	±0.5	
	Relative phase error for a single port Frequency range: 1–2.3 GHz	–	–	±1.0	
	Relative phase error for a single port Frequency range: 2.3–2.7 GHz	–	–	±1.2	
	Relative phase error for a single port Frequency range: 3.3–3.8 GHz	–	–	±1.7	
	Relative phase error for a single port Frequency range: 3.8–5 GHz	–	–	±2.4	
	Relative phase error for a single port Frequency range: 5–6 GHz	–	–	±2.7	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 0.01–0.52 GHz	–	–	±1.0	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 0.52–1 GHz	–	–	±1.5	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 1–2.3 GHz	–	–	±3.0	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 2.3–2.7 GHz	–	–	±4.0	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 3.3–3.8 GHz	–	–	±5.0	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 3.8–5 GHz	–	–	±5.7	
	Port-to-port variation (RFc to RFn (N = 1, 2, 3, 4)) Frequency range: 5–6 GHz	–	–	±5.1	

Table 3 • PE42448 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Group delay ripple	Frequency range: 0.01–0.52 GHz, every 200 MHz	–	–	0.6	ps
	Frequency range: 0.52–1 GHz, every 200 MHz	–	–	0.7	
	Frequency range: 1–2.3 GHz, every 200 MHz	–	–	3.8	
	Frequency range: 2.3–2.7 GHz, every 200 MHz	–	–	2.4	
	Frequency range: 3.3–3.8 GHz, every 200 MHz	–	–	4.8	
	Frequency range: 3.8–5 GHz, every 200 MHz	–	–	5.7	
	Frequency range: 5–6 GHz, every 200 MHz	–	–	4.3	
Settling time	Insertion loss within $\pm 0.1$ dB deviation from the final value	–	–	3.0	$\mu$ s
<b>Note:</b> * All minimum and maximum values are reported over temperature and process.					

## SP4T Control Logic

**Table 4** lists the PE42448 control logic truth table.

*Table 4 • PE42448 Truth Table*

ON Port	V2	V1	SEL
RF1	0	0	0
RF2	0	1	0
RF3	1	0	0
RF4	1	1	0
<b>Transpose</b>			
RF1	1	1	1 or no-connect
RF2	1	0	1 or no-connect
RF3	0	1	1 or no-connect
RF4	0	0	1 or no-connect

## Typical Performance Data

Figure 2–Figure 10 show the typical performance data at +25 °C  $T_{CASE}$  and  $V_{DD} = 5V$  ( $Z_S = Z_L = 50\Omega$ ), unless otherwise specified.

Figure 2 • Insertion Loss vs. Switch Path

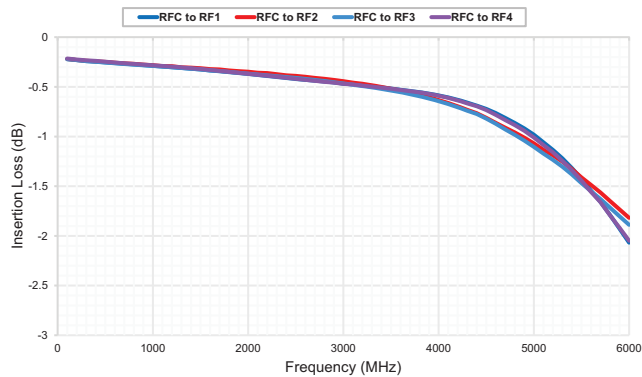


Figure 3 • Insertion Loss vs. Temperature

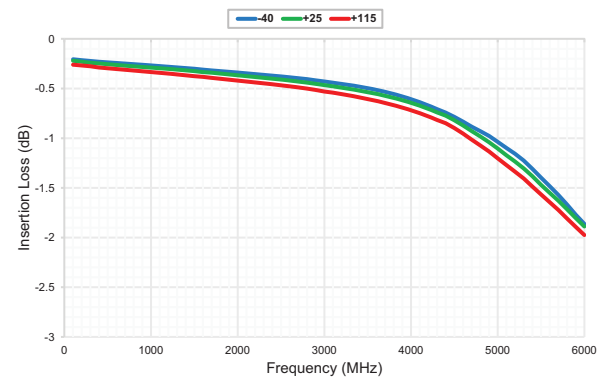


Figure 4 • Input Return Loss vs. Switch Path

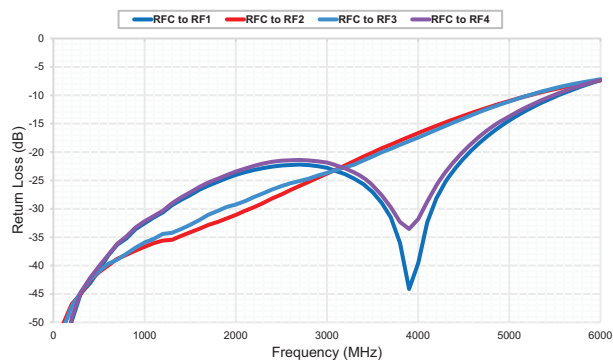


Figure 5 • Output Return Loss vs. Switch Path

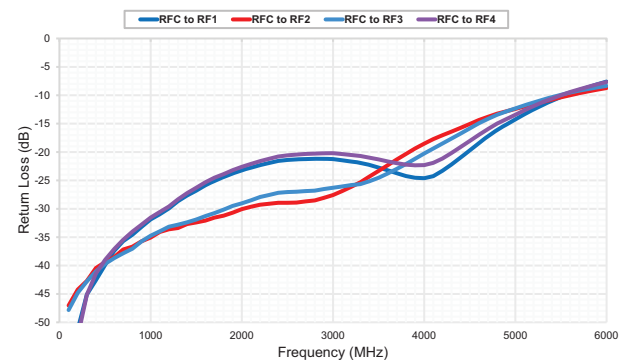


Figure 6 • Output Return Loss vs. Switch Path (Port OFF)

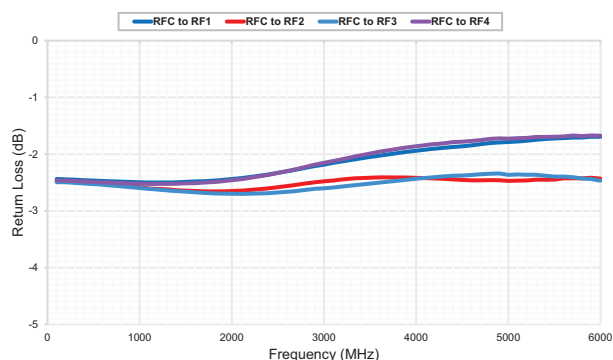


Figure 7 • Isolation When RF1 is Active (RFC-RFx)

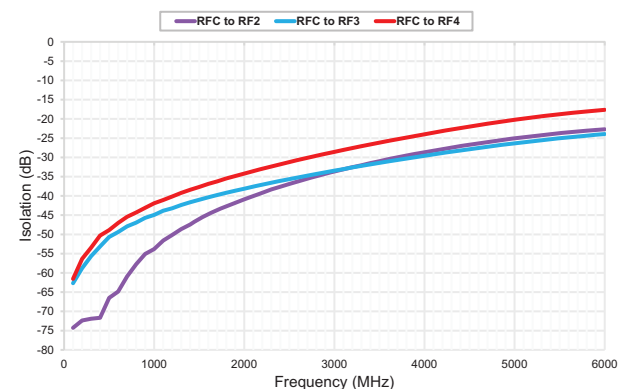




Figure 8 • Isolation When RF2 is Active (RFC-RFx)

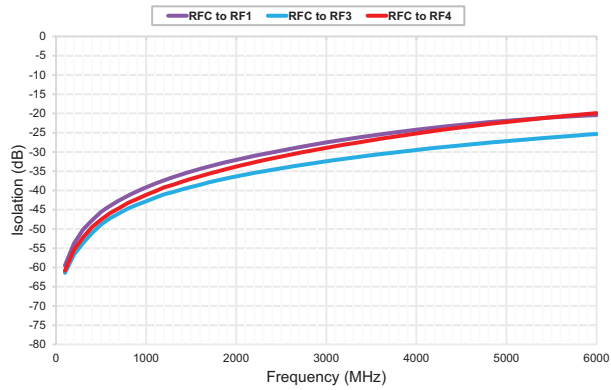


Figure 9 • Isolation When RF3 is Active (RFC-RFx)

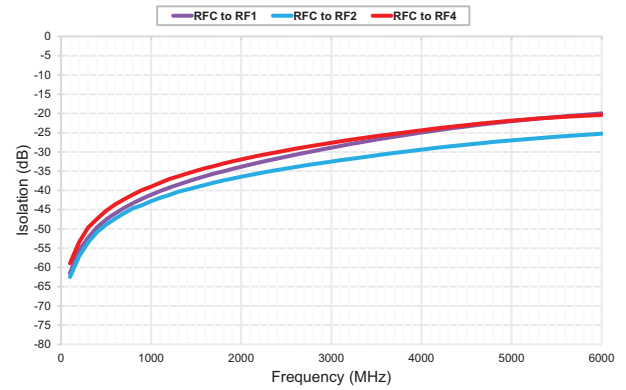
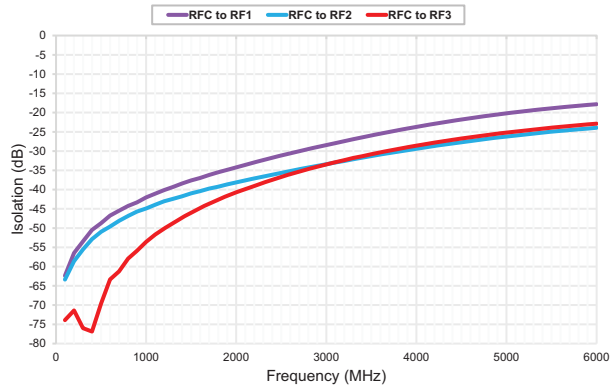


Figure 10 • Isolation When RF4 is Active (RFC-RFx)



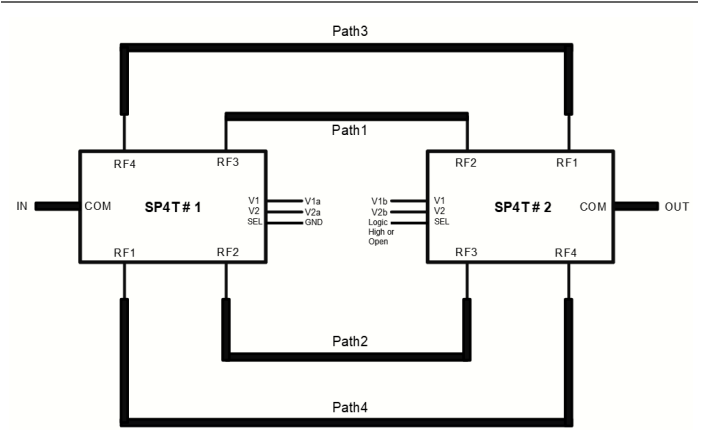
Application Diagram

Table 5 • Application Diagram Lookup Table

Phase State	ON Ports		Path
	SP4T #1	SP4T #2	
State 1	RF3	RF2	Path 1
State 2	RF2	RF3	Path 2
State 3	RF4	RF1	Path 3
State 4	RF1	RF4	Path 4

**Figure 11** shows an application diagram for a phase shifter application using two SP4T switches. To characterize the relative phase, relative phase error, and relative phase variation parameters between paths, all four paths had the exact same delay line lengths.

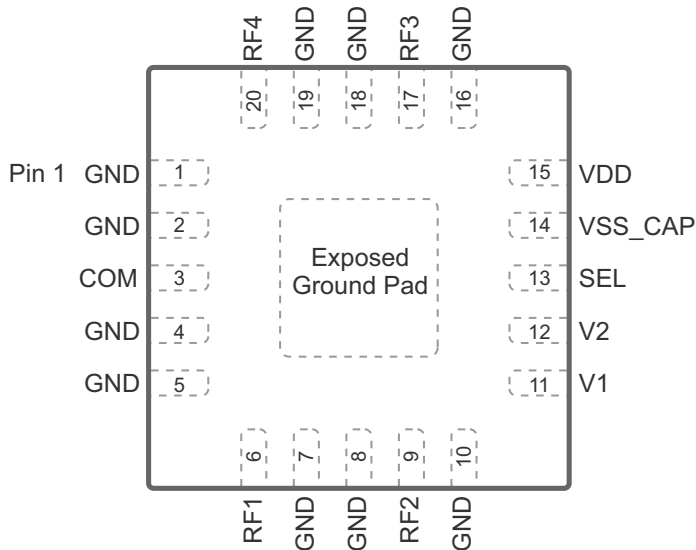
Figure 11 • PE42448 Application Diagram Used in a Phase Shifter



## Pin Information

**Figure 12** shows the PE42448 pin map for the 20-lead 4 × 4 mm LGA package, and **Table 6** lists the description for each pin.

**Figure 12 • Pin Configuration (Top View)**



**Table 6 • PE42448 Pin Descriptions (Cont.)**

Pin No.	Pin Name	Description
15	VDD	Supply voltage
16	GND	Ground
17 <sup>(1)</sup>	RF3	RF port 3
18	GND	Ground
19	GND	Ground
20 <sup>(1)</sup>	RF4	RF port 4
Pad	GND	Exposed pad: Ground for proper operation

1) RF pins 3, 6, 9, 17, and 20 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met.

2) An internal pull-up resistor sets SEL (pin 13) to a logic high if the pin is floating. Ground the pin to set to a logic low.

3) Install a capacitor on VSS\_CAP (pin 14) to GND. Do not apply DC voltage to or ground this pin. Either leave the pin open or connect a ≥100 nF supply capacitor on this pin on the application board. The larger the capacitor value, the longer the circuit startup time.

**Table 6 • PE42448 Pin Descriptions**

Pin No.	Pin Name	Description
1	GND	Ground
2	GND	Ground
3 <sup>(1)</sup>	COM	RF common port
4	GND	Ground
5	GND	Ground
6 <sup>(1)</sup>	RF1	RF port 1
7	GND	Ground
8	GND	Ground
9 <sup>(1)</sup>	RF2	RF port 2
10	GND	Ground
11	V1	Digital control logic input 1
12	V2	Digital control logic input 2
13 <sup>(2)</sup>	SEL	Logic select: Determines the definition for the V1 and V2 pins
14 <sup>(3)</sup>	VSS_CAP	Bypass capacitor for VSS

## Packaging Information

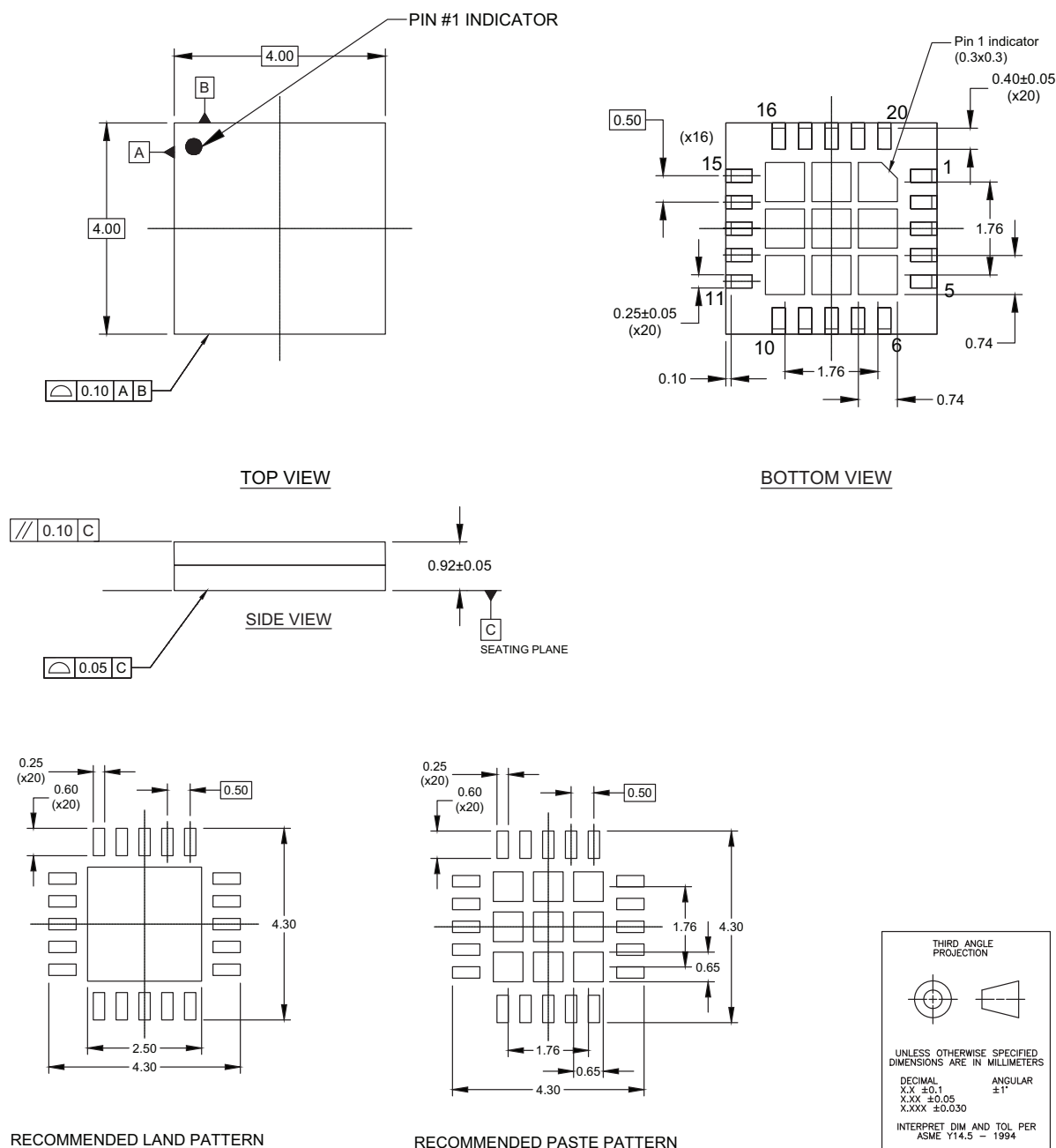
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

### Moisture Sensitivity Level

The PE42448 moisture sensitivity level rating for the 20-lead 4 × 4 mm LGA package is MSL3.

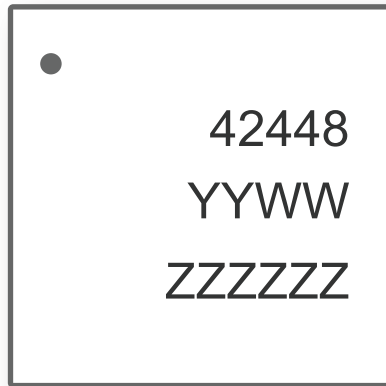
### Package Drawing

Figure 13 • Package Mechanical Drawing for the 20-lead 4 × 4 mm LGA Package



## Top-Marking Specification

Figure 14 • PE42448 Package Marking Specifications

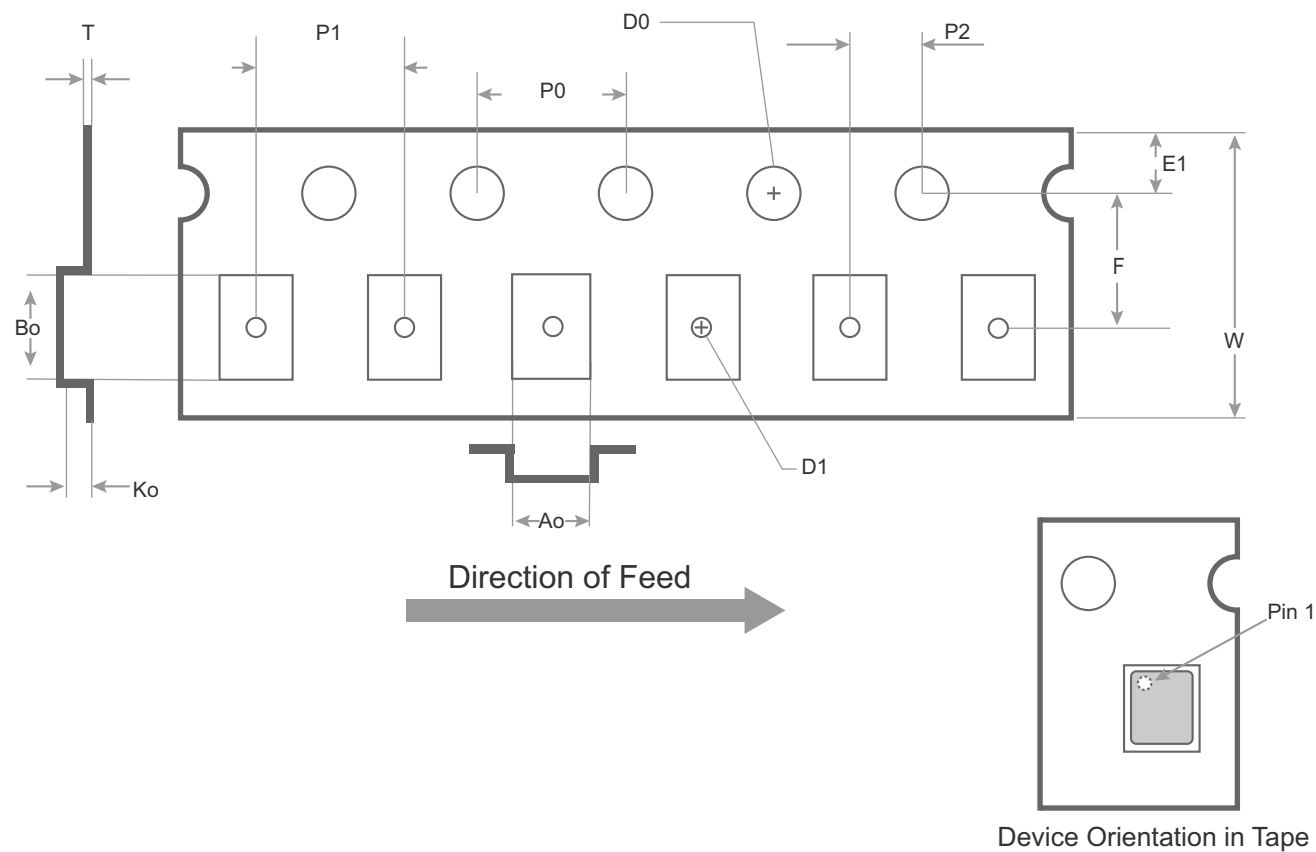


- = Pin 1 indicator
- 42448 = Product part number
- YY = Last two digits of assembly year (2025 = 25)
- WW = Work week of assembly lot start date (01, ..., 52)
- ZZZZZZ = Assembly lot code (max six characters)

DOC-119237-1

Tape and Reel Specification

Figure 15 • Tape and Reel Specification for the 20-lead 4 × 4 mm LGA Package



Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 7 • Tape and Reel Dimensions

Carrier Tape Dimensions					
Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	4.35	±0.1	D1	1.50	Min.
Bo	4.35	±0.1	D0	1.55	±0.05
Ko	1.10	±0.1	E1	1.75	±0.1
P1	8.00	±0.1	P0	4.00	±0.1
W	12.00	+0.3	P2	2.00	±0.1
F	5.50	±0.1	T	0.30	±0.05

## Ordering Information

Table 8 • PE42448 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE42448A-Z	PE42448 SP4T switch	Green 20-lead 4 × 4 mm LGA	3000 units/T&R
EK42448-01	PE42448 evaluation kit	Evaluation kit	1/box

## Document Categories

### Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

### Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

### Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact [sales@psemi.com](mailto:sales@psemi.com).

## Sales Contact

For additional information, contact Sales at [sales@psemi.com](mailto:sales@psemi.com).

## Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

## Patent Statement

pSemi products are protected under one or more of the following U.S. patents: [patents.psemi.com](https://patents.psemi.com)

## Copyright and Trademark

©2024–2025, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.