

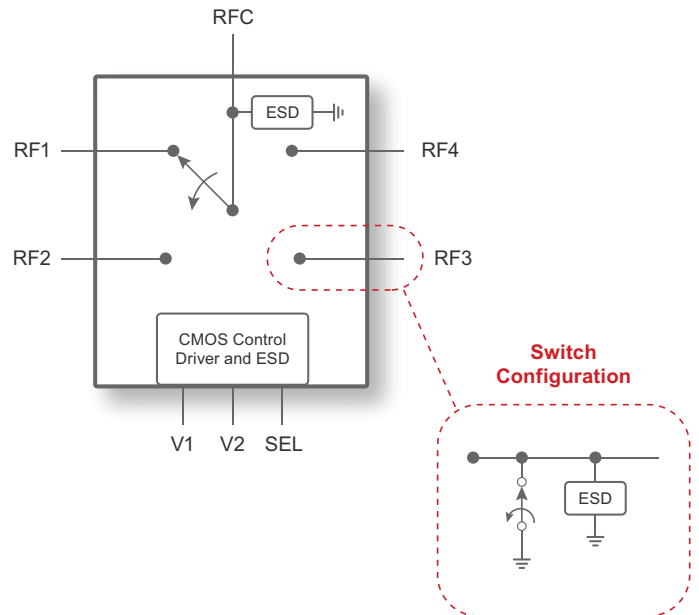
Features

- Low insertion loss:
 - 0.6 dB at 2.6 GHz
 - 0.7 dB at 3.8 GHz
- High linearity IIP3: 88.5 dBm
- High power handling: 39.5 dBm RMS with 11 dB PAR
- Operating temperature: +115 °C
- Packaging: 20-lead 4 × 4 mm LGA

Applications

- Analog hybrid beamforming RF front end
- 5G massive MIMO active antenna system (AAS)
- 4G/4.5G TD-LTE macro/micro cell/RRH

Figure 1 • PE42448 Functional Diagram



Product Description

The PE42448 is a HaRP™ technology-enhanced SP4T RF switch that supports a frequency range from 10 MHz to 6 GHz. It delivers extremely low insertion loss and high linearity with high input power handling capability making this device ideal for hybrid analog beamforming and in 5G massive multi-input, multi-output (MIMO) applications. No blocking capacitors are required if no DC voltage is present on the RF ports.

The PE42448 is manufactured on pSemi's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** could cause permanent damage. Restrict operation to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • PE42448 Absolute Maximum Ratings

Parameter or Condition	Min	Max	Unit
VDD positive supply voltage	-0.3	5.5	V
Digital input voltage	-0.3	3.6	V
Storage temperature	-45	150	°C
ESD voltage HBM, all pins ⁽¹⁾	–	1000	V
ESD voltage, CDM, all pins ⁽²⁾	–	500	V
Thermal resistance ⁽³⁾	–	16	°C/W
Maximum junction temperature ⁽³⁾	–	150	°C
Power handling: 9W average power with following condition at same time: Within operating temperature range. 20 MHz TD-LTE signal with 11 dB PAR, duty cycle 8.8 ms, 88%	–	9	W
No damage power handling requirement: Average power 42.5 dBm; peak power 52 dBm; keep 10s in one time; frequency is one time/month; total 120 times in 10 years; lifetime.	–	52	dBm
Notes: 1) Human body model (MIL-STD 883 Method 3015). 2) Charged device model (JEDEC JESD22-C101). 3) Maximum junction temperature $\leq 115^{\circ}\text{C} + (\text{power dissipation of insertion loss-induced power}) \times \text{thermal resistance}$.			

Recommended Operating Conditions

Table 2 lists the PE42448 recommending operating conditions. Do not operate the device outside the operating conditions listed below.

Table 2 • PE42448 Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Supply voltage	–	–	5	–	V
Supply current	VDD = 5V	–	65	200	μA
Control voltage	–	–	1.8	–	V
Operating temperature range	–	-40	25	115	°C
Switching pins logic levels, 1.8V JEDEC compliant	Logic low	0	–	0.62	V
	Logic high	1.17	–	3.6	V

Electrical Specifications

Table 3 list the PE42448 key electrical specifications at +25 °C T_{CASE} , $V_{DD} = 5V$ ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 3 • PE42448 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Frequency range	–	10 MHz	–	6 GHz	As shown
Port impedance	–	–	50	–	Ohm
Return loss	On-state frequency range: 0.01–2.3 GHz	–	21	–	dB
	On-state frequency range: 2.3–2.7 GHz	–	22	–	dB
	On-state frequency range: 3.3–3.8 GHz	–	16	–	dB
	On-state frequency range: 3.8–5 GHz	–	10	–	dB
	On-state frequency range: 5–6 GHz	–	7	–	dB
SP4T insertion loss (RFC to RFn (n=1,2,3,4) on-state)	Frequency range: 0.01–2.3 GHz over temperature, over process	–	–	0.5	dB
	Frequency range: 2.3–2.7 GHz over temperature, over process	–	–	0.6	dB
	Frequency range: 3.3–3.8 GHz over temperature, over process	–	–	0.7	dB
	Frequency range: 3.8–5 GHz over temperature, over process	–	–	1.5	dB
	Frequency range: 5–6 GHz over temperature, over process	–	–	2.2	dB
Isolation (RFn to RFn)	Frequency range: 0.01–2.3 GHz over temperature, over process	–	30	–	dB
	Frequency range: 2.3–2.7 GHz over temperature, over process	–	28	–	dB
	Frequency range: 3.3–3.8 GHz over temperature, over process	–	24	–	dB
	Frequency range: 3.8–5 GHz over temperature, over process	–	19	–	dB
	Frequency range: 5–6 GHz over temperature, over process	–	18	–	dB
Input IP3	Two-tone CW input power ≤ 31 dBm continuous wave per tone. Frequency range: 2.3–2.7 GHz over temperature, over process	87.5	88.5	–	dBm
	Two-tone CW input power ≤ 34 dBm continuous wave per tone. Frequency range: 3.3–5 GHz over temperature, over process	81	84	–	dBm
HD2	Single-tone CW input power = 34 dBm Frequency range: 2.3–2.7 GHz over temperature, over process	100	–	–	dBm
	Single-tone CW input power = 37 dBm Frequency range: 3.3–5 GHz over temperature, over process	100	–	–	dBm
HD3	Single-tone CW input power = 34 dBm Frequency range: 2.3–2.7 GHz over temperature, over process	100	–	–	dBm
	Single-tone CW input power = 37 dBm Frequency range: 3.3–5 GHz over temperature, over process	100	–	–	dBm
Relative phase error	Relative phase error for one port over temperature, over process	–	–	± 2	deg
	Different ports variation (RFC to RFn (N=1,2,3,4)) in same condition	–	–	± 3	deg

Table 3 • PE42448 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Group delay ripple	Every 200 MHz	–	–	10	ps
Switching speed	Insertion loss within 0.1 dB deviation from the final value. Phase within 1 degree from the final value.	–	–	1.8	μs

SP4T Control Logic

Table 4 lists the PE42448 control logic truth table.

Table 4 • PE42448 Truth Table

ON Port	V2	V1	SEL
RF1	0	0	0
RF2	0	1	0
RF3	1	0	0
RF4	1	1	0
Transpose			
RF1	1	1	1 or no-connect
RF2	1	0	1 or no-connect
RF3	0	1	1 or no-connect
RF4	0	0	1 or no-connect

Application Diagram

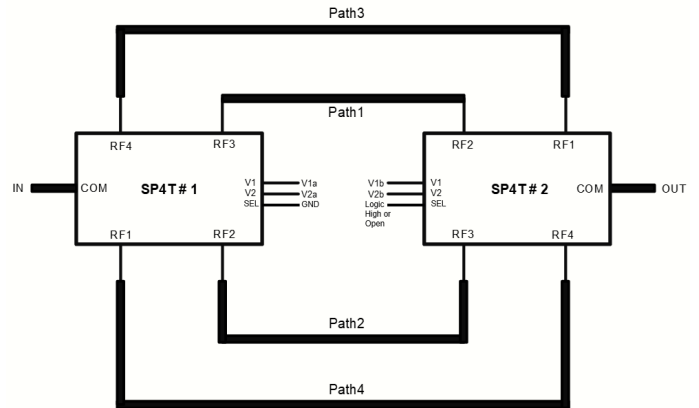
Table 5 • Application Diagram Lookup Table

Phase State	ON Ports		Path
	SP4T #1	SP4T #2	
State 1	RF3	RF2	Path 1
State 2	RF2	RF3	Path 2
State 3	RF4	RF1	Path 3
State 4	RF1	RF4	Path 4

Figure 2 shows an application diagram for a phase shifter using two SP4T switches.

To characterize the relative phase, relative phase error, and relative phase variation parameters between paths, all four paths had the exact same delay line lengths.

Figure 2 • PE42448 Application Diagram Used in a Phase Shifter



Pin Information

Figure 3 shows the PE42448 pin map for the 20-lead 4 × 4 mm LGA package. **Table 6** lists the description for each pin.

Figure 3 • Pin Configuration (Top View)

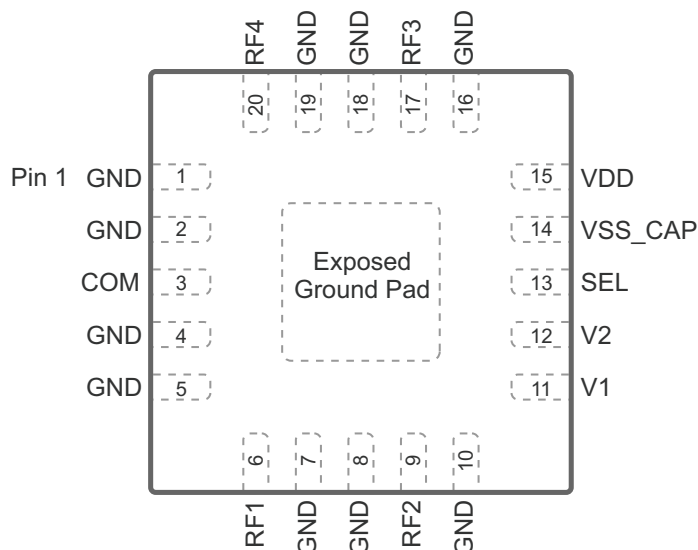


Table 6 • PE42448 Pin Descriptions (Cont.)

Pin No.	Pin Name	Description
15	VDD	Supply voltage
16	GND	Ground
17	RF3 ⁽¹⁾	RF port 3
18	GND	Ground
19	GND	Ground
20	RF4 ⁽¹⁾	RF port 4
Pad	GND	Exposed pad: ground for proper operation.

1) RF pins 3, 6, 9, 17, and 20 must be at 0 V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

2) An internal pull-up resistor sets the pin to a logic high if the pin is floating. Ground the pin to set to a logic low.

3) Install a capacitor on VSS_CAP (pin 14) to GND. Do not apply DC or ground this pin. Either leave the pin open or connect a ≥100 nF supply capacitor on this pin on the application board. The larger the capacitor value, the longer the circuit startup time.

Table 6 • PE42448 Pin Descriptions

Pin No.	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	COM ⁽¹⁾	RF common port
4	GND	Ground
5	GND	Ground
6	RF1 ⁽¹⁾	RF port 1
7	GND	Ground
8	GND	Ground
9	RF2 ⁽¹⁾	RF port 2
10	GND	Ground
11	V1	Digital control logic input 1
12	V2	Digital control logic input 2
13	SEL ⁽²⁾	Logic select—determines the definition for the V1 and V2 pins
14	VSS_CAP ⁽³⁾	Bypass capacitor for VSS

Packaging Information

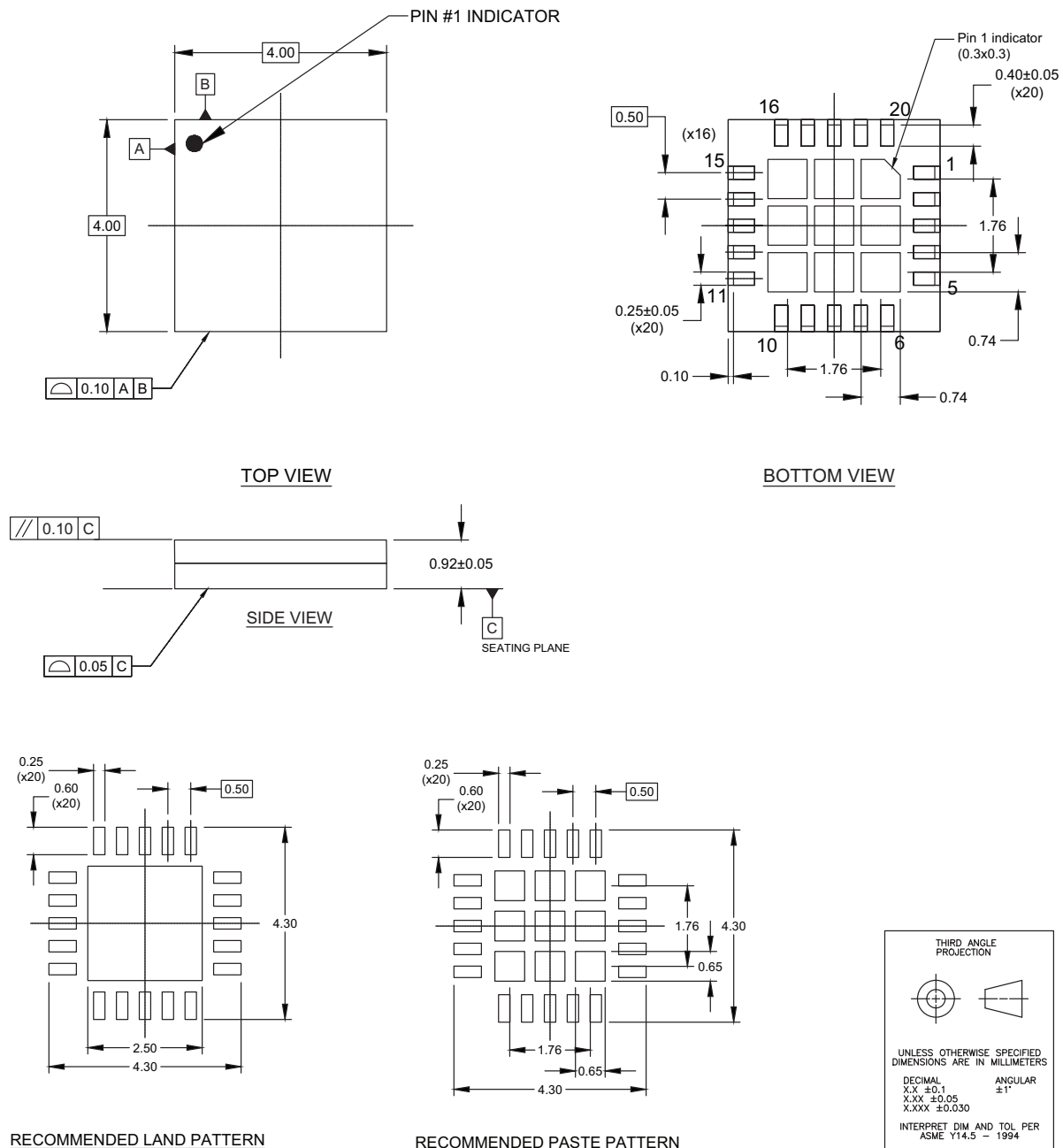
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The PE42448 moisture sensitivity level rating for the 20-lead 4 × 4 mm LGA package is MSL 3.

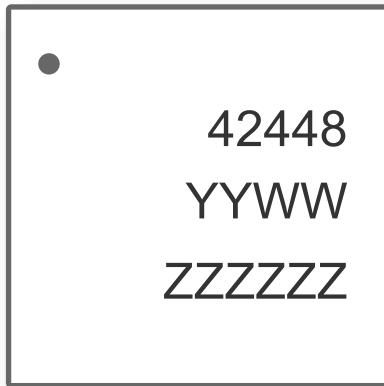
Package Drawing

Figure 4 • Package Mechanical Drawing for the 20-lead 4 × 4 mm LGA Package



Top-Marking Specification

Figure 5 • PE42448 Package Marking Specifications

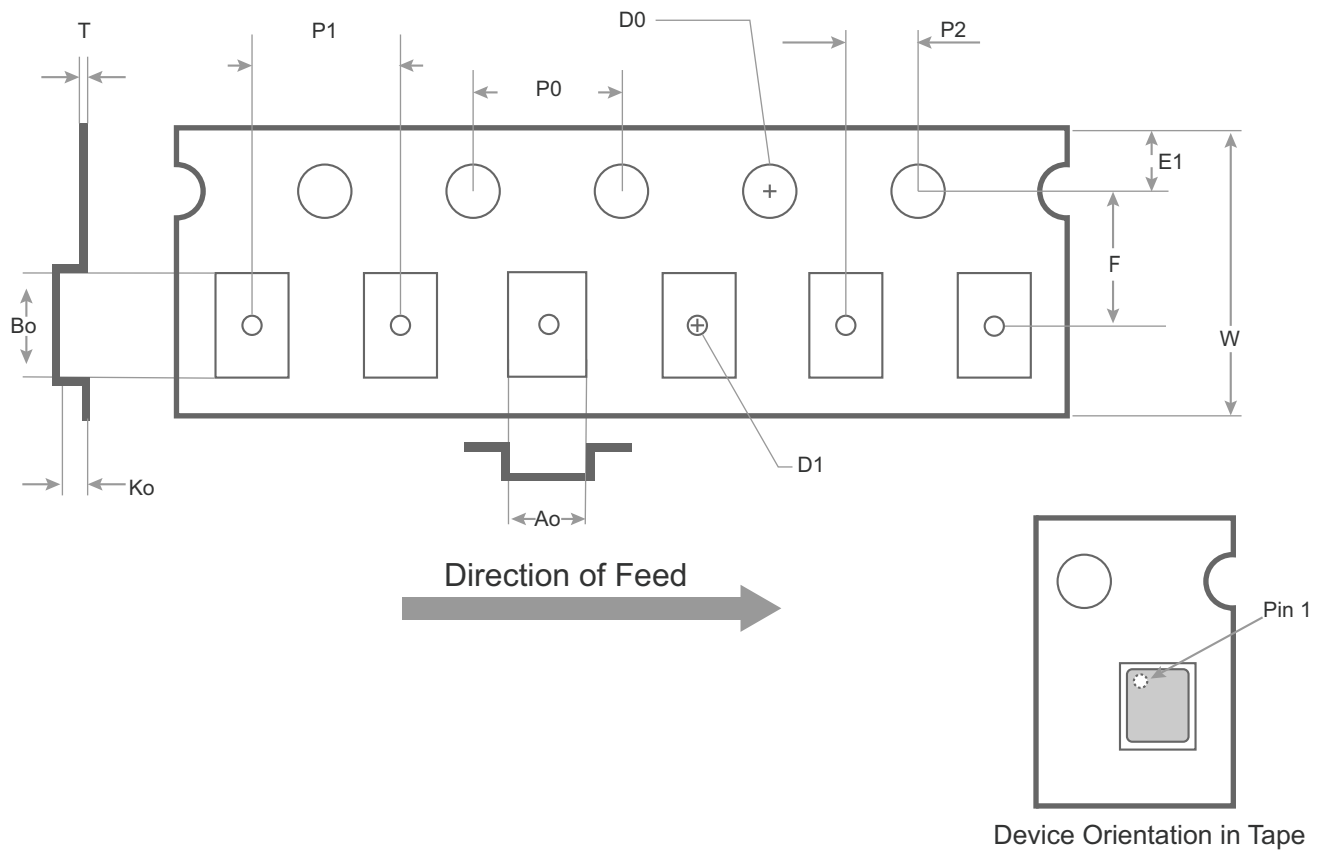


- = Pin 1 indicator
- 42448 = Product part number
- YY = Last two digits of assembly year (2025 = 25)
- WW = Work week of assembly lot start date (01, ..., 52)
- ZZZZZZ = Assembly lot code (max six characters)

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Tape and Reel Specification

Figure 6 • Tape and Reel Specification for the 20-lead 4 × 4 mm LGA Package



Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 7 • Tape and Reel Dimensions

Carrier Tape Dimensions					
Pocket	Nominal	Tolerance	Pocket	Nominal	Tolerance
Ao	4.35	±0.1	D1	1.50	Min.
Bo	4.35	±0.1	D0	1.55	±0.05
Ko	1.10	±0.1	E1	1.75	±0.1
P1	8.00	±0.1	P0	4.00	±0.1
W	12.00	+0.3	P2	2.00	±0.1
F	5.50	±0.1	T	0.30	±0.05

Ordering Information

Table 8 • PE42448 Order Codes and Shipping Methods

Order Codes	Description	Packaging	Shipping Method
PE42448A-Z	PE42448 SP4T switch	Green 20-lead 4 × 4 mm LGA	3000 units/T&R
EK42448-01	PE42448 evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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