PE44820

Document Category: Product Specification

UltraCMOS® RF Digital Phase Shifter 8-bit, 1.7–2.2 GHz

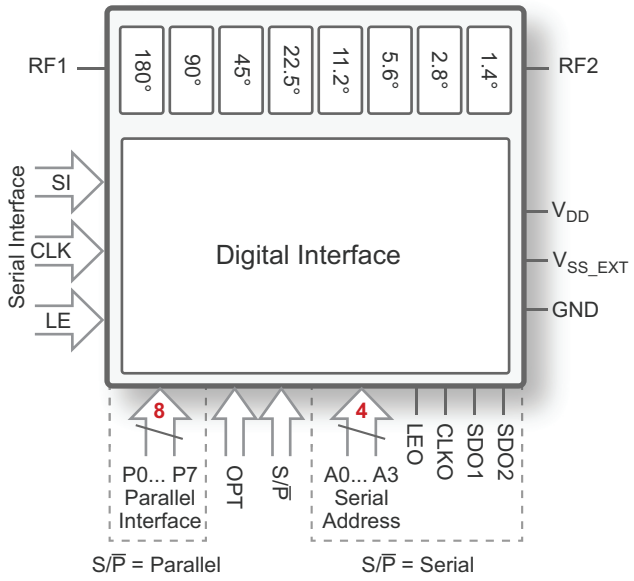
Features

- 8-bit full-range phase shifter of 358.6°; 180°, 90°, 45°, 22.5°, 11.2°, 5.6°, 2.8° and 1.4° bits
- Low RMS phase and amplitude error
  - RMS phase error of 1.0°
  - RMS amplitude error of 0.1 dB
- High linearity of +60 dBm IIP3
- Extended narrow band frequency operation of 1.1–3.0 GHz
- +105 °C operating temperature
- Packaging – 32-lead 5 × 5 × 0.85 mm QFN

Applications

- Base station transceivers
- Weather and military radar
- Active antenna arrays

Figure 1 ▪ PE44820 Functional Diagram



Product Description

The PE44820 is a HaRP™ technology-enhanced 8-bit digital phase shifter (DPS) designed for use in a broad range of applications including: beamforming networks, distributed antenna systems, active antenna systems and phased array applications. This DPS covers a phase range of 358.6 degrees in 1.4 degree steps, maintaining excellent phase and amplitude accuracy across the nominal frequency band of 1.7–2.2 GHz. The PE44820 is also capable of extended frequency operation from 1.1–3.0 GHz for narrow band applications, as detailed in Application Note 45. An integrated digital control interface supports both serial and parallel programming of the phase setting. The PE44820 also features an external negative supply option for a faster switching frequency, and is offered in a 32-lead 5 × 5 × 0.85 mm QFN package. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE44820 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS}

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for PE44820

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Negative supply voltage, V_{SS_EXT}	–3.6	–2.4	V
Digital input voltage	–0.3	3.6	V
Maximum input power		28	dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(*)		500	V

Note: * Human body model (MIL-STD 883 Method 3015).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE44820. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Conditions for PE44820

Parameter	Min	Typ	Max	Unit
Normal mode, V_{SS_EXT} = 0V(1)				
Supply voltage, V_{DD}	2.3		5.5	V
Supply current, I_{DD}		130	200	µA
Bypass mode, V_{SS_EXT} = –3.3V(2)				
Supply voltage, V_{DD}		3.3	5.5	V
Supply current, I_{DD}		50	80	µA
Negative supply voltage, V_{SS_EXT}	–3.6		–3.2	V
Negative supply current, I_{SS}	–40	–16		µA
Normal or Bypass mode				
Digital input high	1.17		3.6	V
Digital input low	–0.3		0.6	V
Digital input current			15	µA
Digital input current, D4–D7(3)		200		µA
RF input power, CW			25	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 20) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 20) to bypass and disable internal negative voltage generator.
3) Typical current draw 200 µA @ 3.6V. Recommended operation at 1.8V reduces input current draw to 0.6 µA.

Electrical Specifications

Table 3 provides the PE44820 key electrical specifications at +25 °C (Z_S = Z_L = 50Ω), unless otherwise specified. Normal mode(1) is at V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode(2) is at V_{DD} = 3.3V and V_{SS_EXT} = –3.3V.

Table 3 ▪ PE44820 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency		1.7	1.95	2.2	GHz
Phase shift range	LSB = 1.4°	+0	358.6		deg
Number of bits			8		bits
Insertion loss	Across all states		6	7.1	dB
RMS phase error	Over all 256 states		1.0		deg
RMS amplitude error	Over all 256 states		0.1		dB
Phase accuracy	Across all states		±3		deg
Attenuation variation	Across all states		±0.50		dB
Phase accuracy relative to reference phase @ 1.95 GHz	1.4° bit		–0.60		deg
	2.8° bit		–0.40		deg
	5.6° bit		+0.05		deg
	11.2° bit		+0.25		deg
	22.5° bit		+0.50		deg
	45° bit		+0.25		deg
	90° bit		+1.75		deg
	180° bit		–0.65		deg
Return loss			13		dB
Input 0.1dB compression point(3)			28		dBm
Input IP3			60		dBm
Settling time(4)	RF settled within 2 deg of final value		365		ns

Notes:
1) Normal mode: single external positive supply used.
2) Bypass mode: both external positive supply and external negative supply used.
3) The input P0.1dB compression point is a linearity figure of merit. Refer to Table 2 for the operating RF input power (50Ω).
4) Use of V_{SS_EXT} reduces the settling time.

Switching Frequency

The PE44820 has a maximum 25 kHz switching frequency in normal mode (pin 20 tied to ground). A faster switching frequency is available in bypass mode (pin 20 tied to V_{SS_EXT}).

Switching frequency describes the time duration between switching events. Switching time is the time between the point the control signal LE reaches 50% of its final value and the point the RF output signal reaches within 10% or 90% of its target value.

Control Logic

Table 4 and **Table 5** provide the Serial/Parallel selection truth table and the Serial and Parallel truth table for the PE44820.

Table 4 ▪ Serial/Parallel Selection Truth Table for PE44820

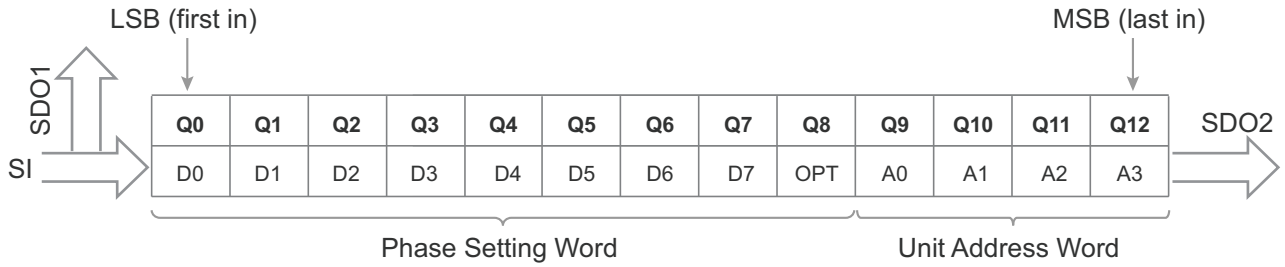
$\overline{P}$/S Pin	Control Mode
L	Parallel
H	Serial

Table 5 ▪ Serial and Parallel Truth Table(*)

Phase Control Setting									Phase Shift Setting RF1–RF2
D0	D1	D2	D3	D4	D5	D6	D7	OPT	
L	L	L	L	L	L	L	L	L	Reference phase
H	L	L	L	L	L	L	L	L	1.4 deg
L	H	L	L	L	L	L	L	L	2.8 deg
L	L	H	L	L	L	L	L	L	5.6 deg
L	L	L	H	L	L	L	L	L	11.2 deg
L	L	L	L	H	L	L	L	L	22.5 deg
L	L	L	L	L	H	L	L	L	45 deg
L	L	L	L	L	L	H	L	H	90 deg
L	L	L	L	L	L	L	H	L	180 deg
H	H	H	H	H	H	H	H	H	358.6 deg
L	L	L	L	L	L	L	L	H	1.4 deg

Note: * Normal mode operation uses the OPT bit to synchronize the 90 degree bit optimizing the phase accuracy across all states. For additional information on the OPT bit, reference Application Note 45.

Figure 2 ▪ Serial Control Register Map



Phase Setting Word is derived directly from the Phase Setting. For example, to program the 205.3 degree setting at unit address 3:

Unit Address Word: **1100** (Unit Address = 1 + 2)
Phase Setting Word: Multiply the degree desired by 256 states divided by 360° and convert to binary

205.3° × (256 states / 360°) = state 146
state 146 → 01001001
LSB→MSB (205.3 deg setting = 2.8° + 22.5° + 180°)

Program Word (LSB→MSB): 010010010 + **1100**, OPT bit is synchronized to 90° bit

Programming Options

Parallel/Serial Selection

Either a Parallel or Serial addressable interface can be used to control the PE44820. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the Parallel interface and $\overline{P}$/S = HIGH selecting the Serial-addressable interface.

Parallel Mode Interface

The Parallel interface consists of nine CMOS-compatible control lines that select the desired phase state, as shown in **Table 5**.

The Parallel interface timing requirements are defined by **Figure 5** (Latched Parallel/Direct Parallel Timing Diagram) and **Table 7** (Parallel and Direct Interface AC Characteristics).

For Latched Parallel programming, the Latch Enable (LE) should be held LOW while changing phase state control values, then pulse LE HIGH to LOW (per **Figure 5**) to latch new phase state into device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing a phase state control value will change the device state to a new phase. Direct mode is ideal for manual control of the device (using hardware, switches or jumpers).

Serial Interface

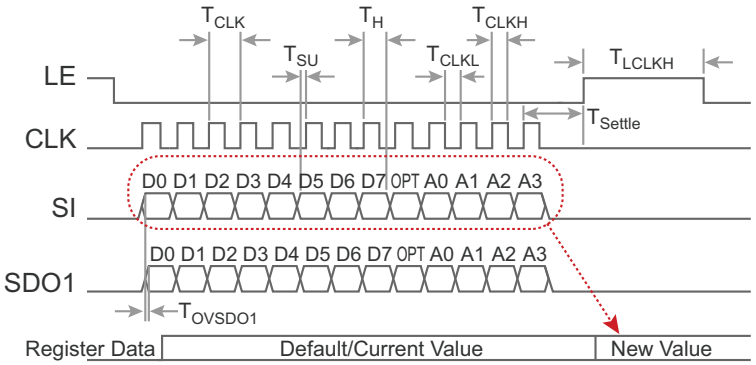
The Serial addressable interface is a 13-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 13 bits make up two words comprising 9 data and 4 address bits. The first word is the Phase Word, which controls the state of the DPS. The second Word is the Address Word, which is compared to the static (or programmed) logical states of the A0–A3 digital state; otherwise, its current state will remain unchanged. **Figure 4** and **Figure 6** illustrate examples of timing diagrams for programming a state.

The Serial interface is controlled using three CMOS-compatible signals: Serial In (SI), Clock (CLK) and Latch Enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the Phase Word.

SDO1 is provided to connect several devices in parallel to the serial bus. SDO1 is a non-inverting buffered output of SI. SDO1 changes state with SI without regard to CLK. This is useful to connect multiple devices with different serial addresses to the serial controller without the need for additional external logic buffers.

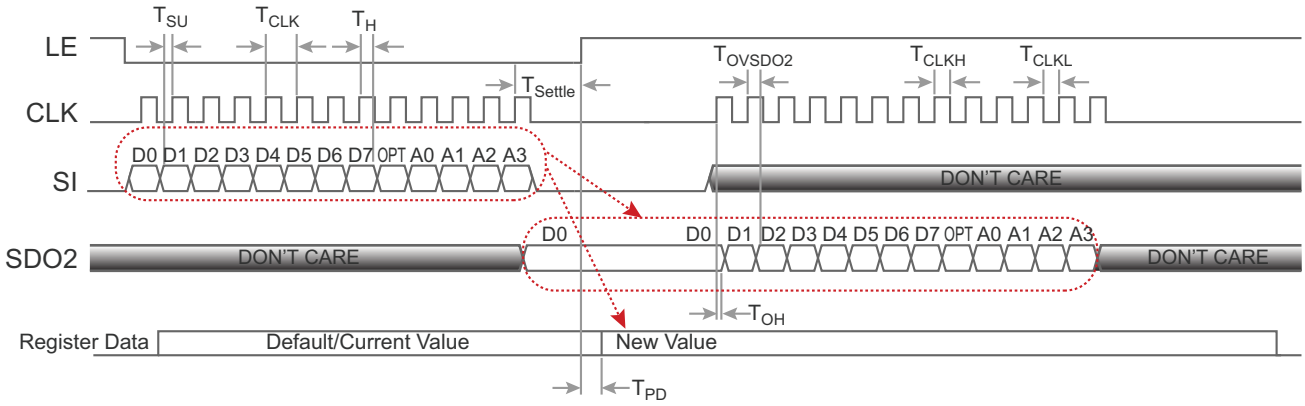
SDO2 is the buffered output of the last bit of the internal shift register and changes state on the rising edge of the clock.

Figure 3 ▪ Buffered SDO1 Serial Interface(*)



Note: * SDO1 data buffered with respect to SI and valid on rising edge of CLK.

Figure 4 ▪ SDO2 (Last Bit of Shift Register)—Single Write with Readback(*)



Note: * SDO2 data changes on rising edge of CLK and is valid on falling edge of CLK.

Table 6 ▪ Serial Interface AC Characteristics

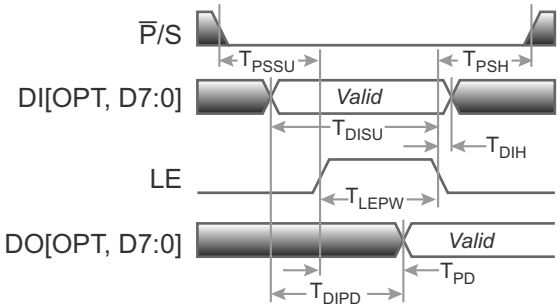
Parameter	Min	Max	Unit
Serial clock period, T_{CLK}	100		ns
Serial clock HIGH time, T_{CLKH}	30		ns
Serial clock LOW time, T_{CLKL}	30		ns
Last serial clock rising edge setup time to latch enable rising edge, T_{SETTLE}	10		ns
Latch enable min pulse width, T_{LEPW}	30		ns
Serial data setup time, T_{SU}	10		ns
Serial data hold time, T_H	10		ns
Digital register delay (internal), T_{PD}		10	ns
SD01 and SD02 drive strength(*)		25	pF
Serial data output propagation delay from SI to SDO1, T_{OVSD01}		25	ns
Serial data output propagation delay from CLK to SDO2, T_{OVSD02}		25	ns
Serial data output hold time from CLK rising edge, T_{OH}	1		ns

Note: * SD01/2 maximum capacitive load drive strength for clock period of 100 ns.

Table 7 ▪ Parallel and Direct Interface AC Characteristics

Parameter	Min	Max	Unit
Latch enable minimum pulse width, T_{LEPW}	30		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel data hold time, T_{DIH}	100		ns
Parallel/Serial setup time, T_{PSSU}	100		ns
Parallel/Serial hold time, T_{PSH}	100		ns
Digital register delay (internal), T_{PD}		10	ns
Digital register delay (internal, direct mode only), T_{DIPD}		5	ns

Figure 5 ▪ Latched Parallel/Direct Parallel Timing Diagram



Typical Performance Data

Figure 6–Figure 19 show the typical performance data at +25 °C, V_{DD} = 3.3V and V_{SS_EXT} = 0V, unless otherwise specified.

Figure 6 ▪ Relative Phase Error: OPT Bit

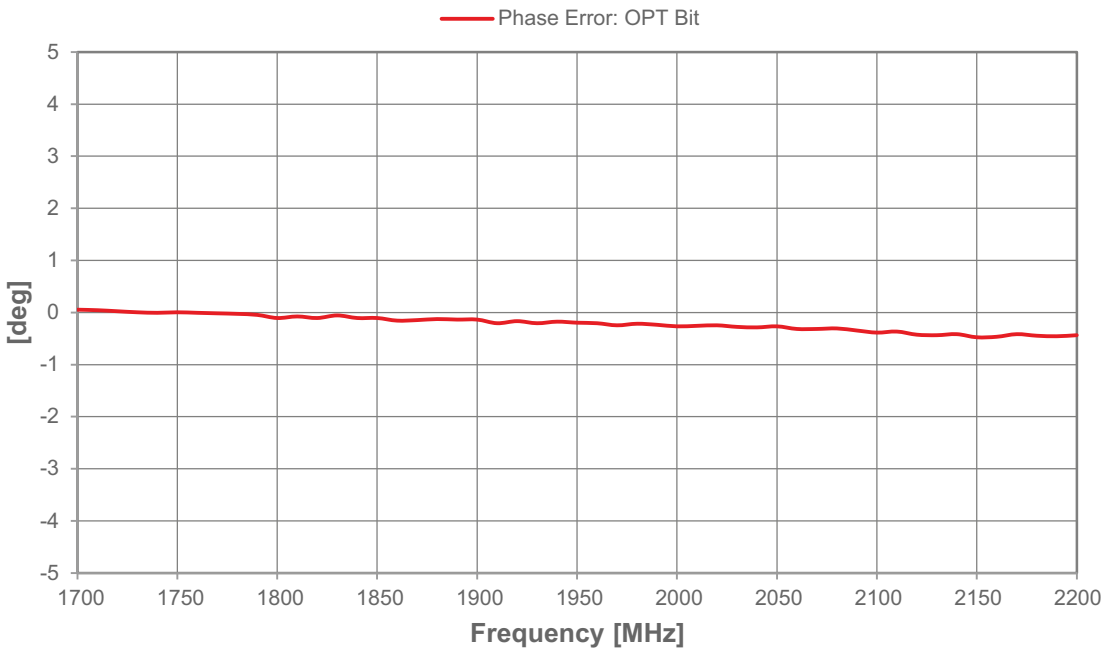


Figure 7 ▪ Relative Phase Error: 180 Deg Bit

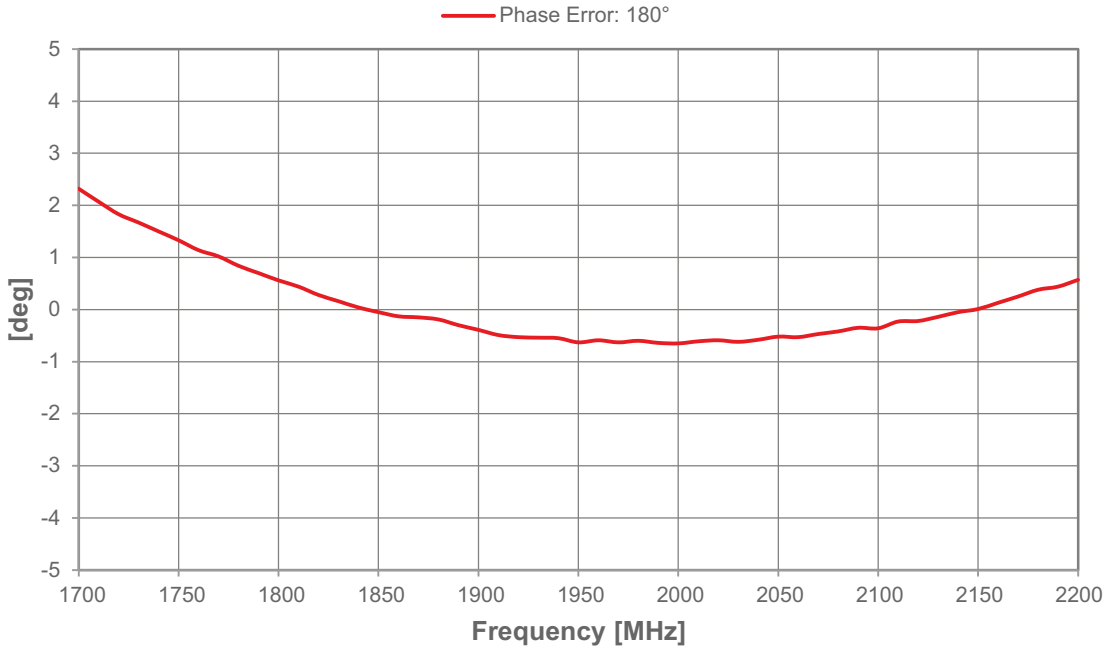


Figure 8 ▪ Relative Phase Error: 90 Deg Bit

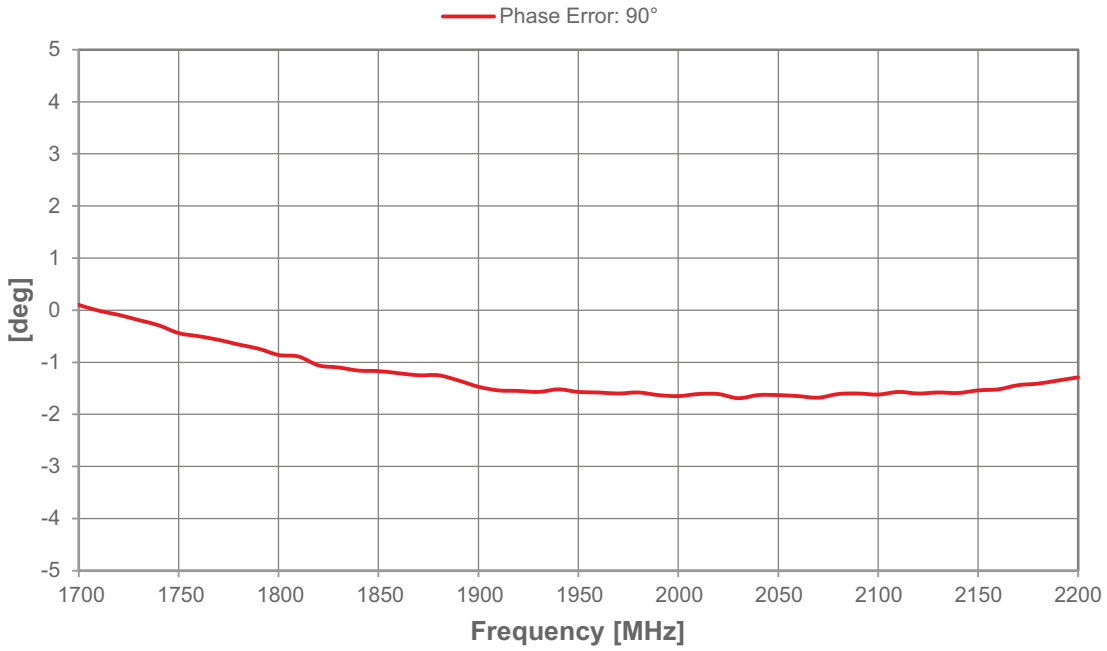


Figure 9 ▪ Relative Phase Error: 45 Deg Bit

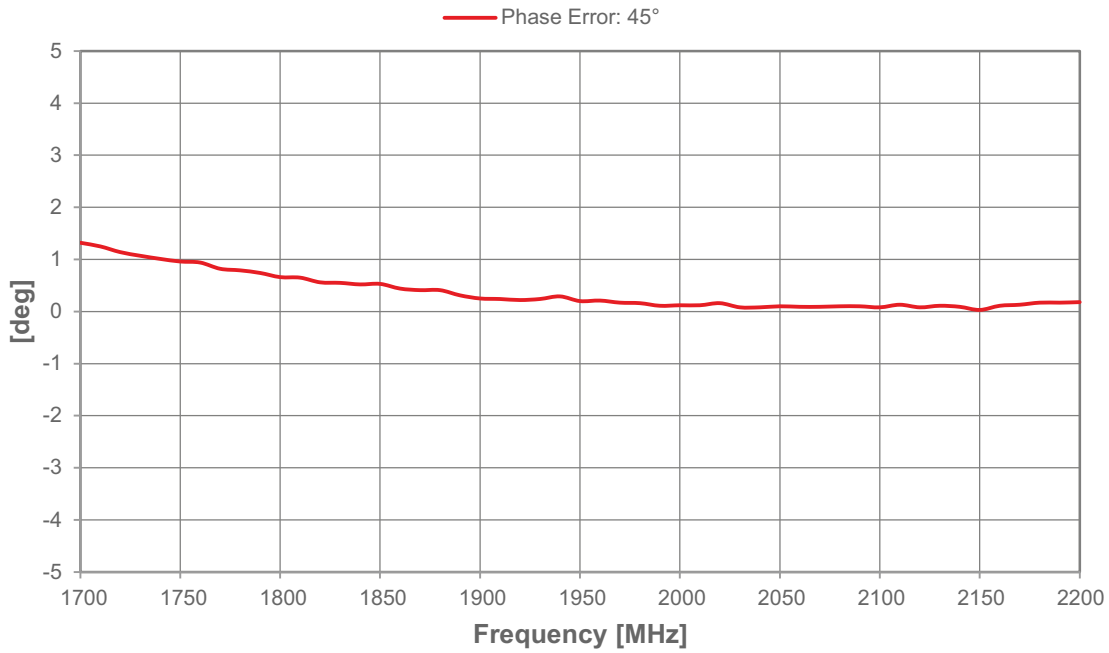


Figure 10 ▪ Relative Phase Error: 22.5 Deg Bit

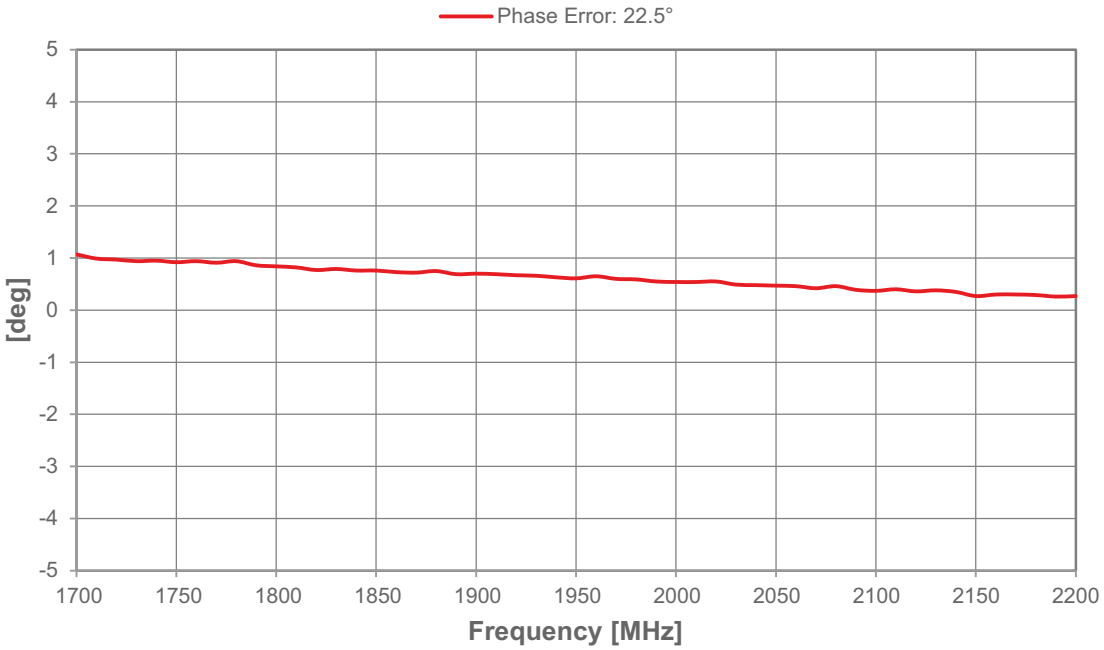


Figure 11 ▪ Relative Phase Error: 11.25 Deg Bit

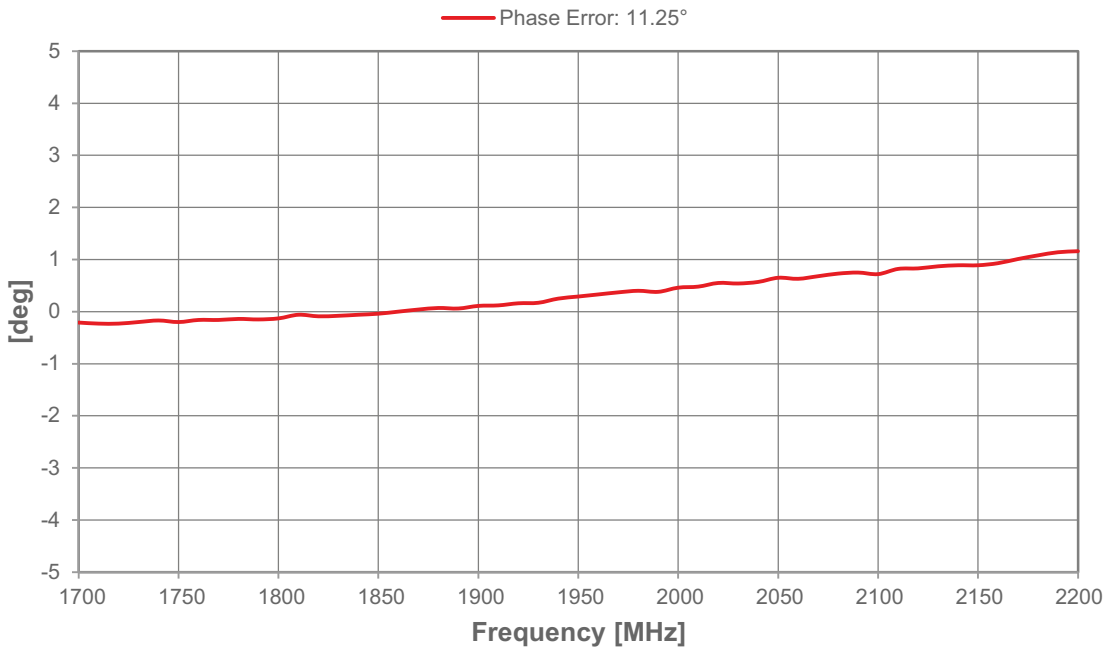


Figure 12 ▪ Relative Phase Error: 5.6 Deg Bit

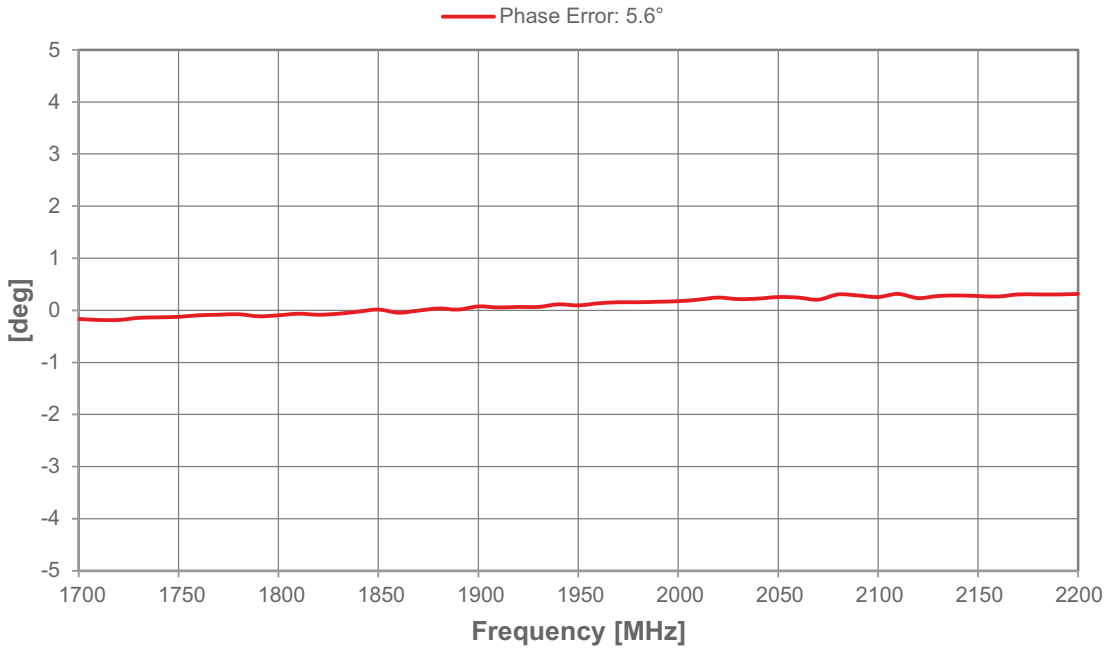


Figure 13 ▪ Relative Phase Error: 2.8 Deg Bit

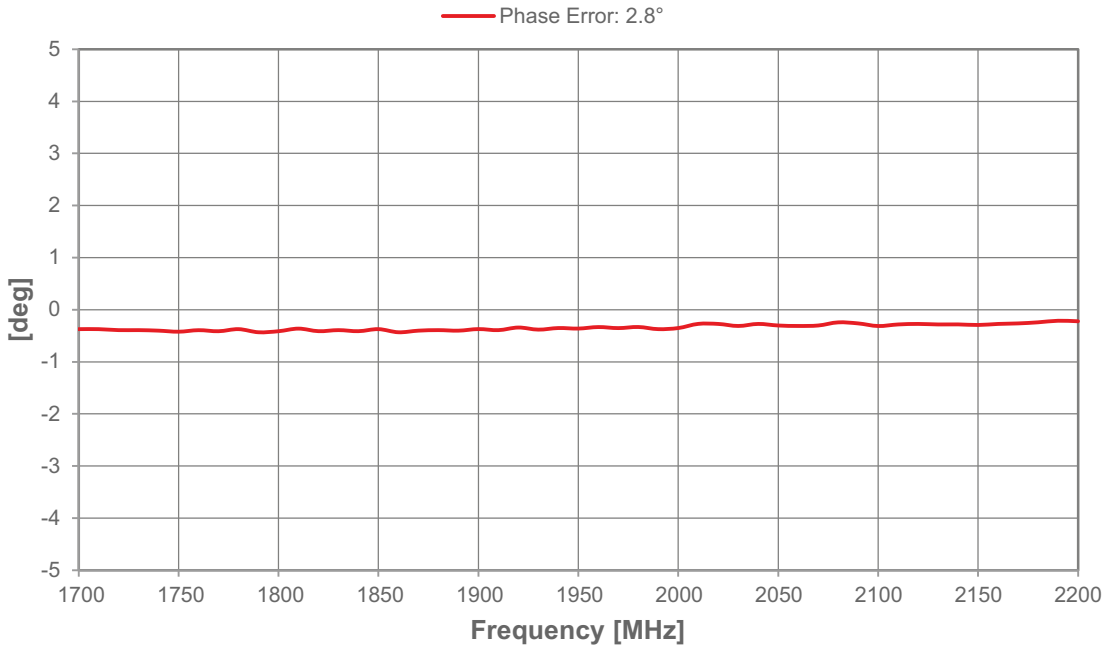


Figure 14 ▪ Relative Phase Error: 1.4 Deg Bit

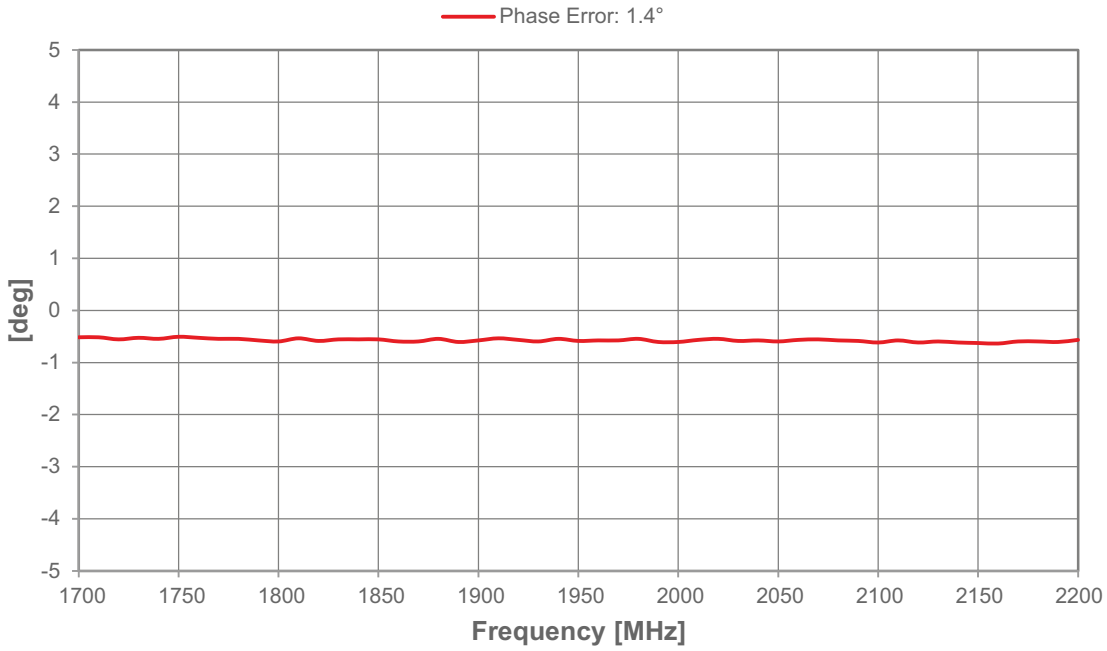


Figure 15 ▪ RMS Amplitude Error

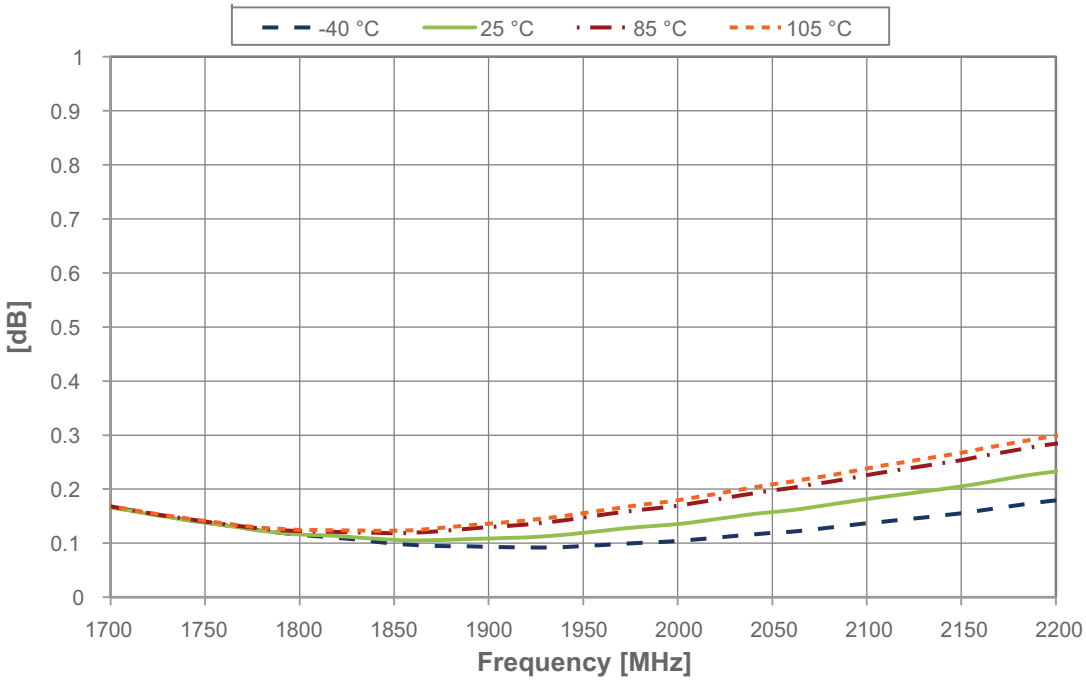


Figure 16 ▪ RMS Phase Error

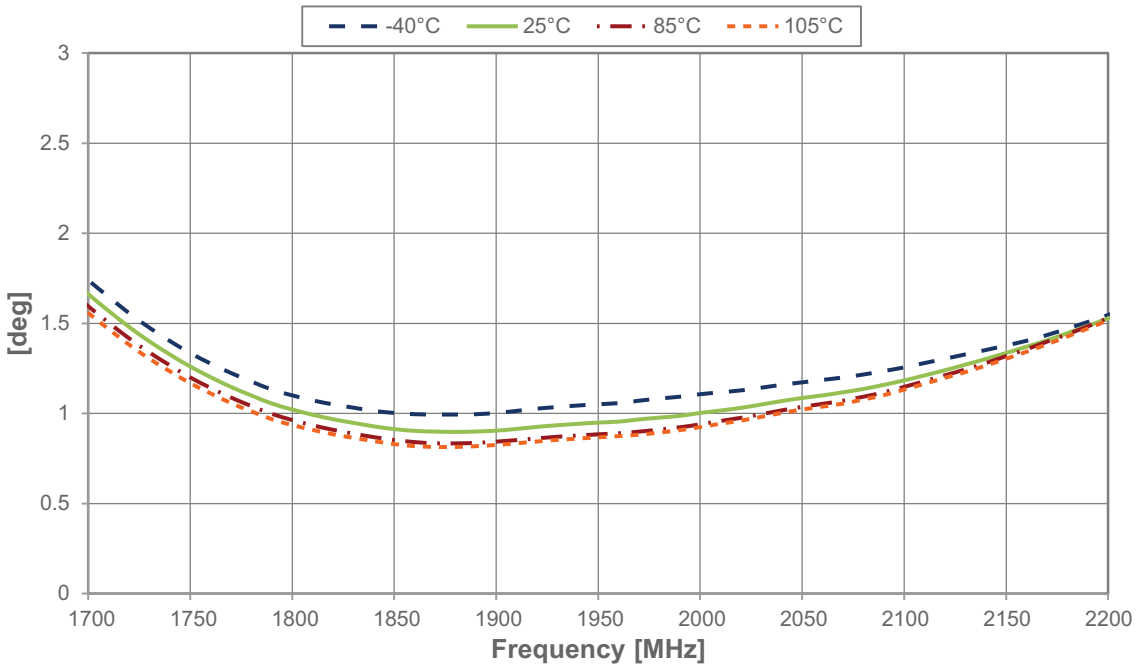


Figure 17 ▪ Maximum Return Loss S11 Over All Major States

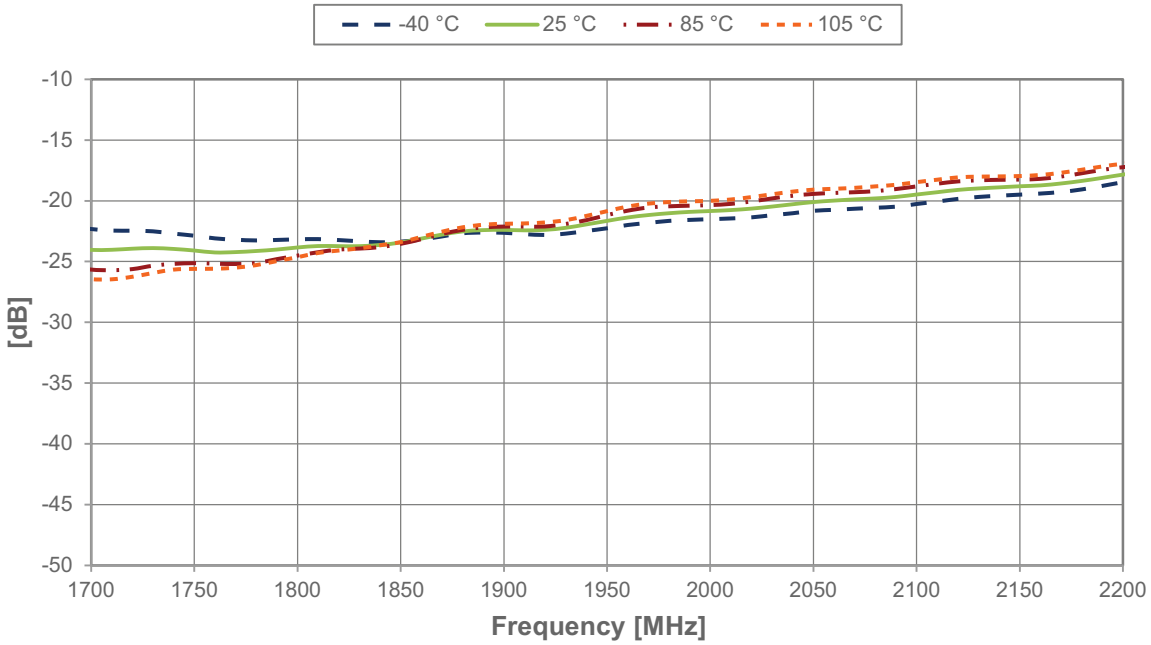


Figure 18 ▪ Maximum Return Loss S22 Over All Major States

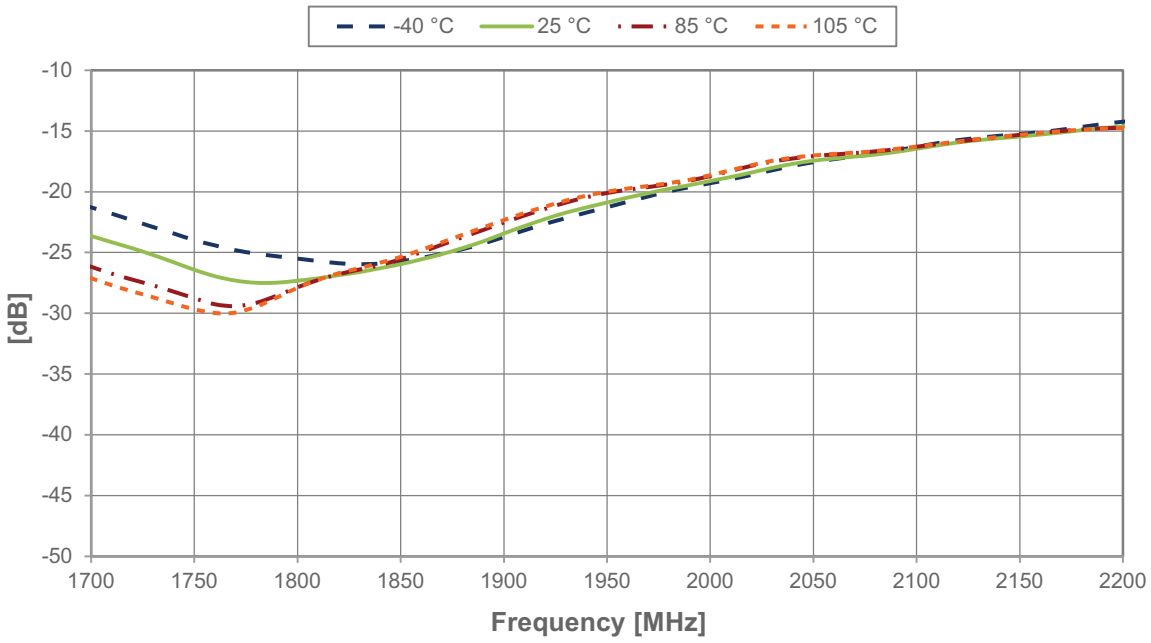
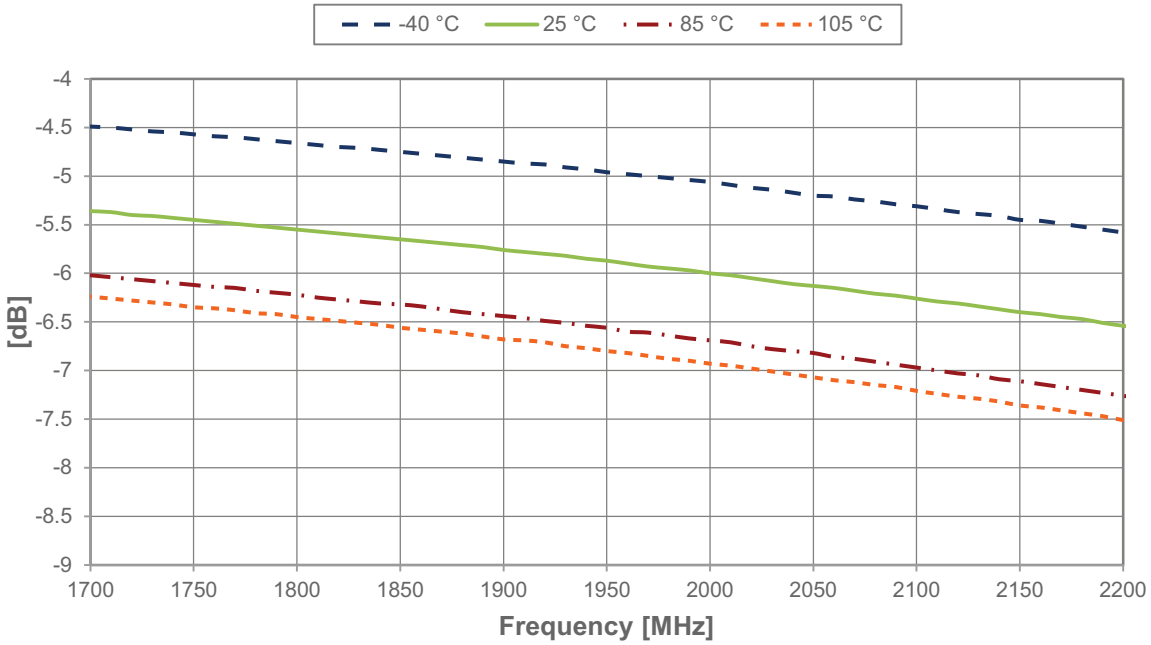


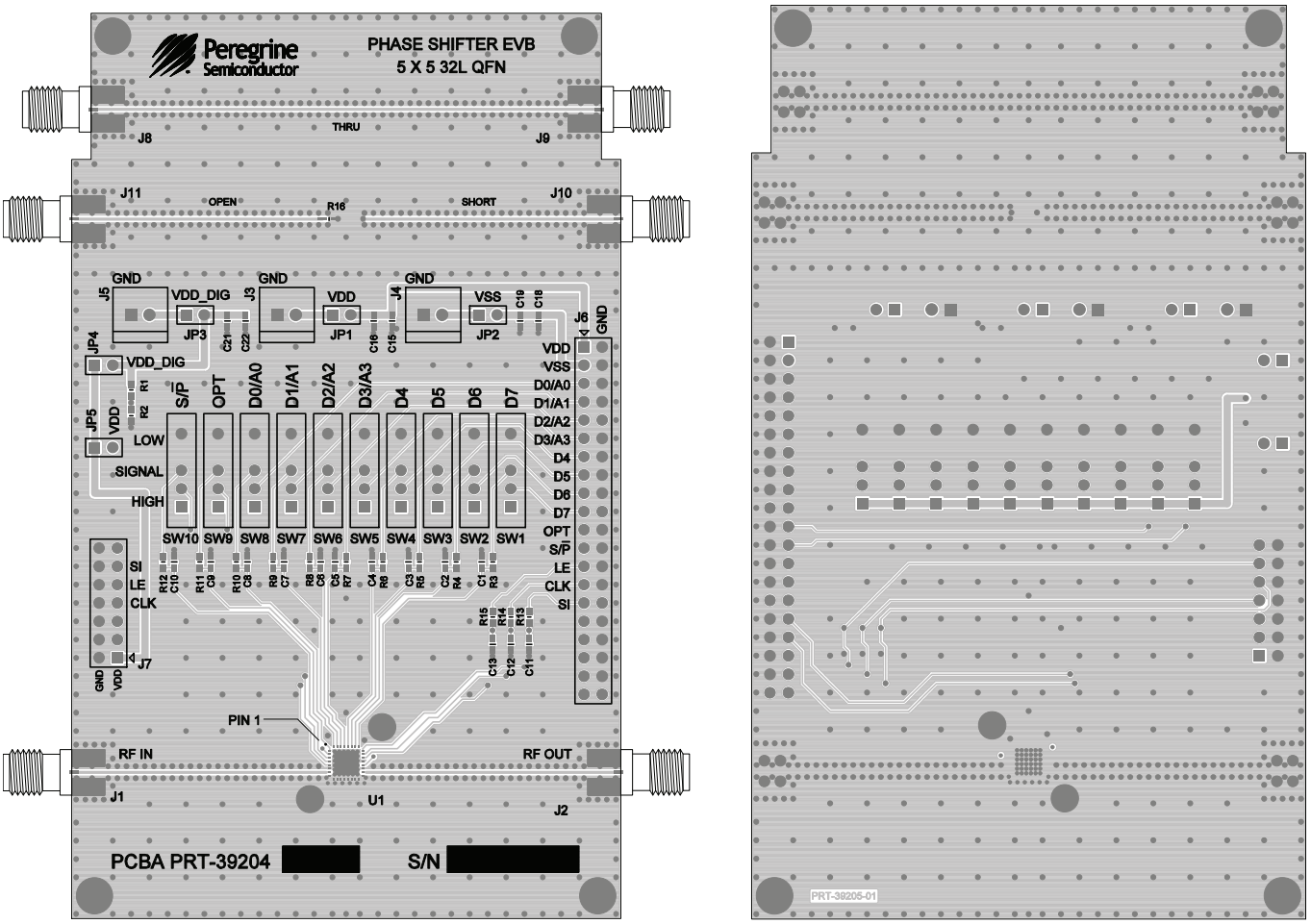
Figure 19 ▪ Insertion Loss—Reference States



Evaluation Kit

The PE44820 evaluation kit (EVK) includes hardware required to control and evaluate the functionality of the DPS. The DPS evaluation software can be downloaded at www.psemi.com and requires a PC running Windows® operating system to control the USB interface board. Refer to the PE44820 Evaluation Kit User's Manual for more information.

Figure 20 ▪ Evaluation Kit Layout for PE44820



Pin Information

This section provides pinout information for the PE44820. Figure 21 shows the pin map of this device for the available package. Table 8 provides a description for each pin.

Figure 21 ▪ Pin Configuration (Top View)

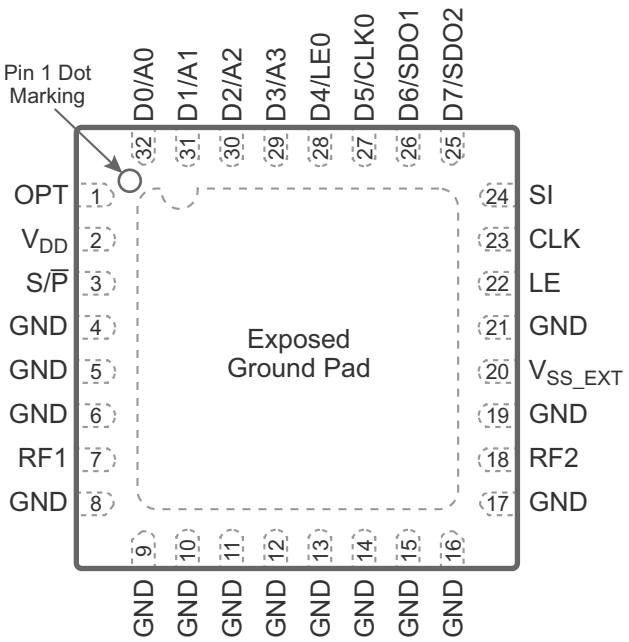


Table 8 ▪ Pin Descriptions for PE44820

Pin No.	Pin Name	Description
1	OPT[1]	Parallel: phase accuracy optimization bit. Serial: not used—must be tied low.
2	V_{DD}	Supply voltage.
3	S/$\overline{P}$	Serial/parallel mode select.
4–6, 8–17, 19, 21	GND	Ground.
7	RF1[2]	RF1 port.
18	RF2[2]	RF2 port
20	V_{SS_EXT}[3]	External V_{SS} negative supply voltage.
22	LE	Parallel: see table note[7]. Serial: serial interface latch enable input.

Table 8 ▪ Pin Descriptions for PE44820 (Cont.)

Pin No.	Pin Name	Description
23	CLK	Parallel: not used, optional tie high or low (internal pullup). Serial: serial interface clock input.
24	SI	Parallel: not used, optional tie high or low (internal pullup). Serial: serial interface data input.
25	D7/SDO2[4][6][8]	Parallel—D7 180° bit/serial data out 2.
26	D6/SDO1[4][6][8]	Parallel—D6 90° bit/serial data out 1.
27	D5/CLKO[6][8]	Parallel—D5 45° bit/serial-buffered CLK out.
28	D4/LEO[6][8]	Parallel—D4 22.4° bit/serial buffered LE out.
29	D3/A3	Parallel—D3 11.2° bit/serial A3 address bit.
30	D2/A2	Parallel—D2 5.6° bit/serial A2 address bit.
31	D1/A1	Parallel—D1 2.8° bit/serial A1 address bit.
32	D0/A0	Parallel—D0 1.4° bit/serial A0 address bit.
Pad	GND	Exposed pad: Ground for proper operation.

Notes:

1) OPT bit is used to optimize the phase accuracy across all states. OPT bit (pin 1) must be synchronized to the 90° bit (pin 26) for normal operation.
2) RF1 and RF2 (pins 7 and 18) are bi-directional.
3) Use V_{SS_EXT} (pin 20) with negative supply (V_{SS_EXT} = –3.4V) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 20) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
4) SDO2 is buffered output of the last bit of the internal shift register.
5) SDO1 is a buffered output of the serial data input.
6) D4–D7 (pins 25–28) are bi-directional pins.
7) LE operation in parallel mode: Holding LE HIGH while changing OPT, D7:D0 will immediately latch phase setting states into the device. Holding LE low while changing OPT,D7:D0 requires a rising edge on LE to latch the phase setting states into the device.
8) If not using buffered output in serial mode, leave floating.

Packaging Information

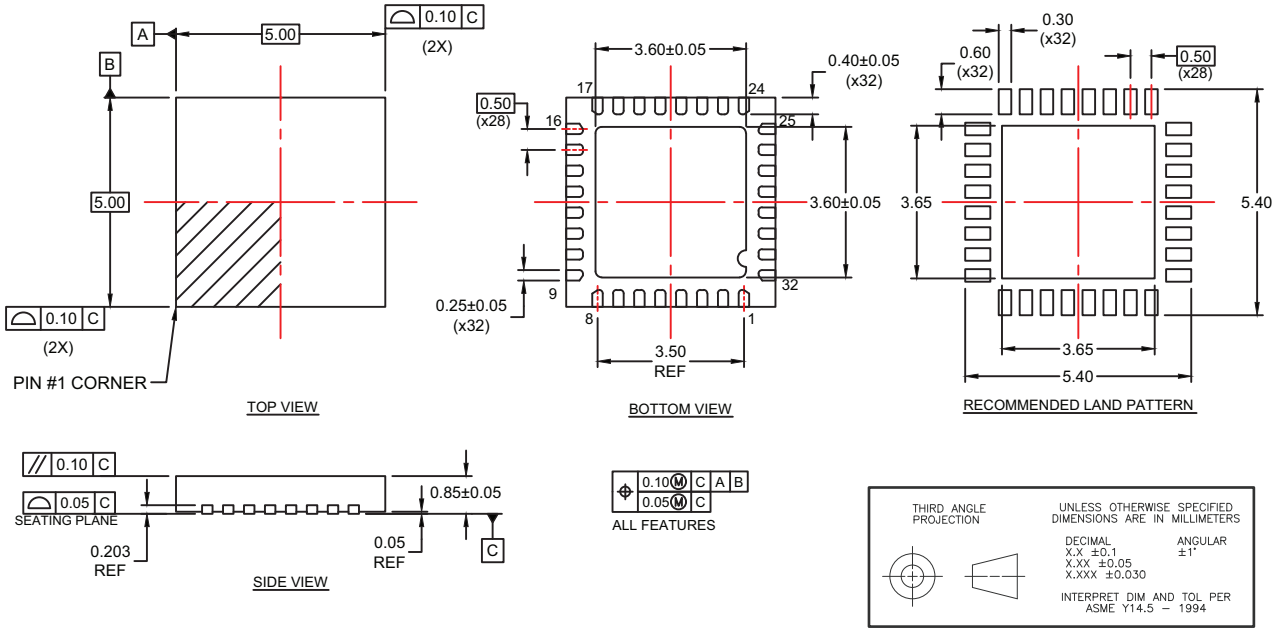
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape and reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE44820 in the 32-lead 5 × 5 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 22 ▪ Package Mechanical Drawing for 32-lead 5 × 5 × 0.85 mm QFN



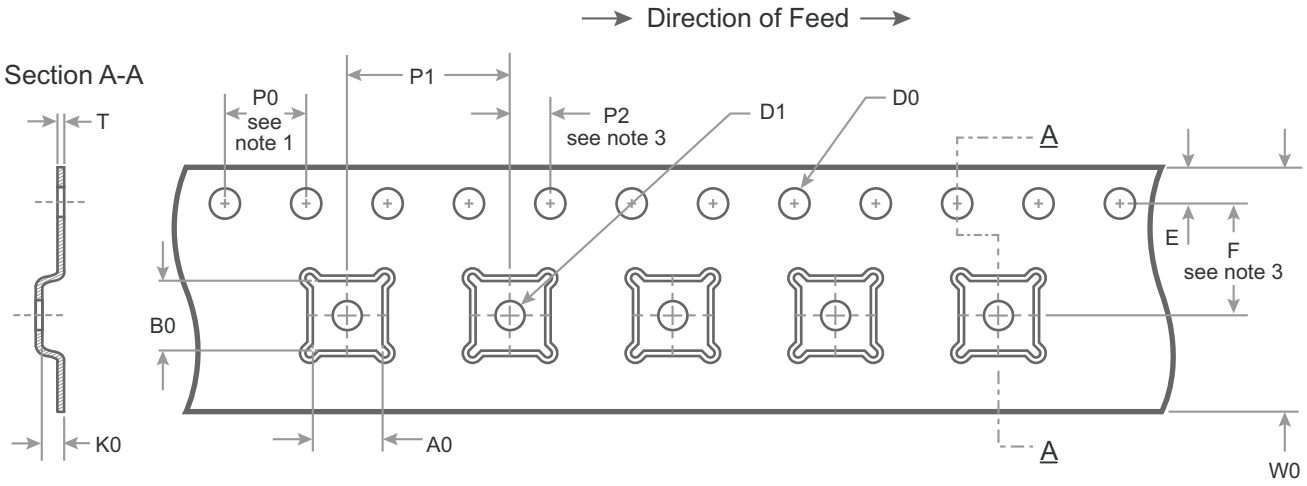
Top-Marking Specification

Figure 23 ▪ Package Marking Specifications for PE44820

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZZ = Assembly lot code (maximum seven characters)

Tape and Reel Specification

Figure 24 ▪ Tape and Reel Specifications for 32-lead 5 × 5 × 0.85 mm QFN

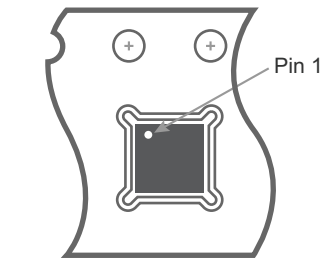


A0	5.25
B0	5.25
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

Ordering Information

Table 9 lists the available ordering codes for the PE44820 as well as available shipping methods.

Table 9 ▪ Order Codes for PE44820

Order Codes	Description	Packaging	Shipping Method
PE44820B–X	PE44820 Digital phase shifter	Green 32-lead 5 × 5 mm QFN	500 units/T&R
EK44820–02	PE44820 Evaluation kit	Evaluation kit	1/Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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