PE44951

Document Category: Advance Information

Monolithic Phase and Amplitude Controller, 6.025–7.525 GHz

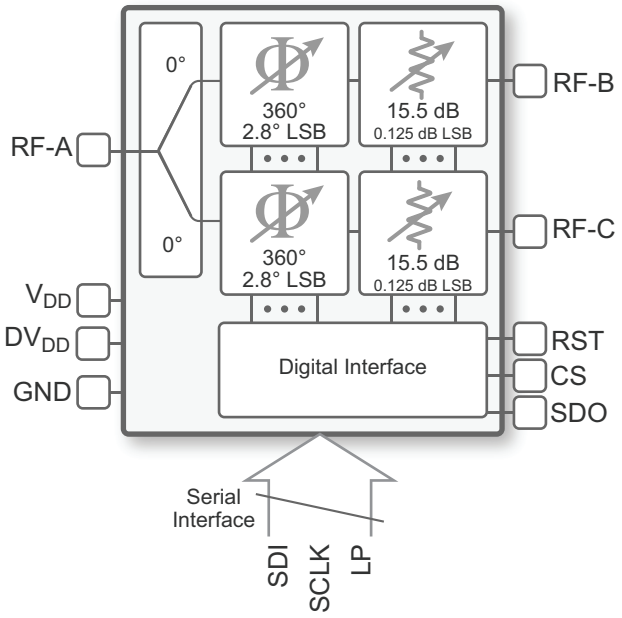
Features

- Highly integrated two-way splitter, phase shift with digital step attenuation
- 7-bit digital phase shifter, phase shift range of 360°, 2.8° resolution
- 7-bit digital step attenuator, 15.5-dB range, 0.125-dB resolution
- Low insertion loss
- High channel isolation
- Fast switching time of 320 ns
- Input IP3 +55 dBm
- +115 °C operating temperature
- Packaging: 32-lead 5 × 5 × 0.7 mm FCLGA

Applications

- Input signals phase and magnitude control for power amplifier
- 4G macro/micro cells/small cells (micro, pico)
- 5G massive MIMO system
- Distributed antenna systems (DAS)
- Precision phase shifter
- Dual polarization antenna alignment
- Analog linearization techniques

Figure 1 • PE44951 Functional Diagram



Product Description

The PE44951 includes highly integrated phase shifters with digitally controlled step attenuators for use across the 6.025 to 7.525 GHz frequency range. Each RF path is independently controlled through the SPI control interface. The PE44951 is ideal for wireless infrastructure applications, such as massive MIMO (mMIMO) macro and micro base stations, next-generation 5G solutions, and small cell applications.

This monolithic phase and amplitude controller is manufactured on the pSemi UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, which features high compactness, excellent isolation and low insertion loss.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings listed in **Table 1** can cause permanent damage. Restrict operation to the limits in **Table 2**. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • PE44951 Absolute Maximum Ratings

Parameter/Condition	Min	Max	Unit
RF input power, CW at each P_{OUT}	–	20	dBm
Operating temperature range: @ Package case, full functionality @ Package case, full performance	 -40 -33	 +115 +115	 °C °C
Storage temperature	-45	+150	°C
Thermal resistance Case = package bottom	–	TBD	°C/W
Maximum junction temperature in worst-case operation	–	+150	°C

Recommended Operating Conditions

Table 2 lists the PE44951 recommended operating conditions. Do not operate devices outside the recommended operating conditions listed below.

Table 2 • PE44951 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply voltage for analog, V_{DD}	3.15	3.3	3.45	V
Supply voltage for digital, D_{VDD}	1.7	–	3.45	V
Supply current	–	–	1	mA
Digital input high	1.17	–	D_{VDD}	V
Digital input low	0	–	0.63	V
Operating temperature range: @ Package case, full functionality @ Package case, full performance	 -40 -33	–	 +115 +115	 °C °C
D_{VDD} supply current(1) Standby Operation	–	–	 TBD TBD	 µA mA
Digital output high level, I_{OUT} = 2 mA	TBD	–	–	–
Digital output low level, I_{OUT} = 2 mA	–	–	TBD	–
RST pulse width, RST = low (active)	10	–	–	ns
LP pulse width, high or low	4	–	–	ns
LP lead/lag SPI command(2)	20	–	–	ns

Notes:
1) RST = CD = high, SCLK = SDI = LP = low, 50-MHz SCLK frequency, CL = 34 pF at the SDO pin.
2) LP low-to-high or high-to-low before/after SPI command 20 ns.

Electrical Specifications

Table 3 lists the PE44951 key electrical specifications at +25 °C, V_{DD} = 3.3V over frequency range 1 unless otherwise specified.

Table 3 • PE44951 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Range 1					
Frequency range 1	Carrier bandwidth	6425	–	7125	MHz
Port A return loss 1	Including external matching network, within frequency range 1,average over DPS states	–	19	–	dB
	Worst-case DPS state	–	13	–	dB
Port B/C return loss 1	Including external matching network, within frequency range 1, average over DPS states	–	17	–	dB
	Worst-case DPS state	–	11	–	dB
Insertion loss, range 1	Including external matching network, within frequency range 1, average over DPS states	–	8.2	–	dB
	Worst-case DPS state	–	9.1	–	dB
Channel isolation range 1	Between port B and C, and port A terminated, average over DPS states	–	31	–	dB
	Worst-case DPS state	–	30	–	dB
Range 2					
Frequency range 2	Linearization bandwidth	6025	–	7525	MHz
Port A return loss 1	Including external matching network, within frequency range 1, average over DPS states	–	15	–	dB
	Worst-case DPS state	–	12	–	dB
Port B/C return loss 1	Including external matching network, within frequency range 1, average over DPS states	–	17	–	dB
	Worst-case DPS state	–	10	–	dB
Insertion loss, range 1	Including external matching network, within frequency range 1, average over DPS states	–	8.5	–	dB
	Worst-case DPS state	–	9.6	–	dB
Channel isolation range 1	Between port B and C, and port A terminated, average over DPS states	–	29.7	–	dB
	Worst-case DPS state	–	27.6	–	dB
Gain ripple (3) For the gain ripple case, the frequency coverage must support frequency range 2 from 6025-7525 MHz. Fc = (Flow + Fhigh)/2	Fc2 ± 350 MHz (6425 – 7125) MHz	–	±0.5	–	dB
	Fc ± 550 MHz (6225 – 7325) MHz	–	0.8	–	dB
	Fc2 ± 350 MHz (6025 – 7525) MHz	–	±1.0	–	dB
Relative phase shift	Phase difference between port B/C without phase change	–	±0.9	–	deg

Table 3 • PE44951 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Group delay variation	Among port B/C with phase change	–	0.55	–	ns
Range 1 using LUT #1					
I.L. variation vs DPS states (no LUT)	Difference Min and Max IL over all the phase states, range 1	–	±0.65	–	dB
I.L. variation vs DPS states (with LUT #1)		–	±0.4	–	dB
Phase shift range		–	360	–	deg
Phase step size	7-bit phase shifter, 2.8-deg step	–	2.84	–	deg
Phase step size error	(DNL), 7-bit DPS, 2.8-deg step	–	1.9	–	deg
		–	-2.1	–	
Phase integrated error*	(INL), 7-bit DPS	–	4.4	–	deg
		–	-5	–	
Attenuation step size		–	0.125	–	dB
Attenuation control range		–	17.0	–	dB
Attenuation step size error	(DNL)	–	0.08	–	dB
		–	-0.17	–	dB
Attenuation integrated error*	(INL)	–	-0.175	–	dB
Phase variation vs DSA state	Difference Min and Max phase across all phase states	–	±1.62	–	deg
Range 1 using LUT #2					
I.L. variation vs DPS states (with LUT #2)		–	±0.22	–	dB
Phase shift range		–	360	–	deg
Phase step size	7-bit phase shifter, 2.8-deg step	–	2.813	–	deg
Phase step size error	(DNL), 7-bit DPS, 2.8-deg step	–	2.6	–	deg
		–	-2.6	–	
Phase Integrated error*	(INL), 7-bit DPS	–	2.5	–	deg
		–	-2.5	–	
Attenuation step size		–	0.125	–	dB
Attenuation control range (4)		–	15.5	–	dB
Attenuation step size error	(DNL)	–	±0.125	–	dB

Table 3 • PE44951 Electrical Specifications (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Attenuation integrated error*	(INL)	–	0.13	–	dB
		–	-0.3	–	
Phase variation vs DSA state	Difference the Min and Max phase across all phase states	–	1.4	–	deg
		–	-1.8	–	
Power handling and linearity					
Input @ 0.1-dB compression point	Overall conditions at port A	–	25.5	–	dBm
	Overall conditions at port B/C	–	22.2	–	dBm
Input IP3	Overall conditions at port A	–	54.6	–	dBm
	Overall conditions at port B/C	–	56	–	dBm
Timing and glitch, phase shifter					
Phase switching time	Insertion loss must be within 0.1-dB deviation from final value and phase within 1 degree from final value.	–	0.32	–	µs
Amplitude switching time	(with any steps change)	–	0.32	–	µs
Amplitude glitch	(with any steps change)	–	3.2	–	dB
Timing and glitch, digital step attenuator					
Amplitude switching time	Insertion loss must be within 0.1-dB deviation from final value.	–	0.144	–	µs
Amplitude glitch	All steps	–	1.8	–	dB
Supply current	In total VDD = 2.3V to 5.5V DVDD = 1.8V to 3.45V	–	0.2	–	mA
Data write baud rate	Serial port interface (SPI)	–	50	–	MHz
Read back baud rate	DVDD = 1.8V to 3.3V	–	10	–	MHz

Notes:

1) All measurements made under nominal conditions, 25°C and VDD/DVDD = 3.3V.
2) A look-up table (LUT) was used to plot the phase and attenuation states, and the phase and attenuation errors were calculated taking the LUT into account. The LUT is provided to the customers, and they must use it in their system to meet the above-mentioned specs. Use the 5.625-degree step LUT if the 2.8-degree step LUT is not precise enough for your application. For the DSA, also use the LUT for 0.25-dB step size to help improve the attenuation error.
3) To fix the gain ripple issue, use LUT#2. If you can implement the LUT in your system, the gain ripple will not be present.
4) The attenuation range is reduced as part of the DSA range gets used up for the I.L. stabilization over the DPS states.
5) For look-up tables, measurement data, and detailed plots of the parameters listed in this table and any interface-related questions, please contact the pSemi Sales and Marketing application team at https://www.psemi.com/global-sales/ or sales@psemi.com.

Pin Information

Figure 2 shows the PE44951 pin map for the 32-lead 5 × 5 × 0.7 mm FCLGA package. **Table 4** lists the description for each pin.

Figure 2 • Pin Configuration (Top View)

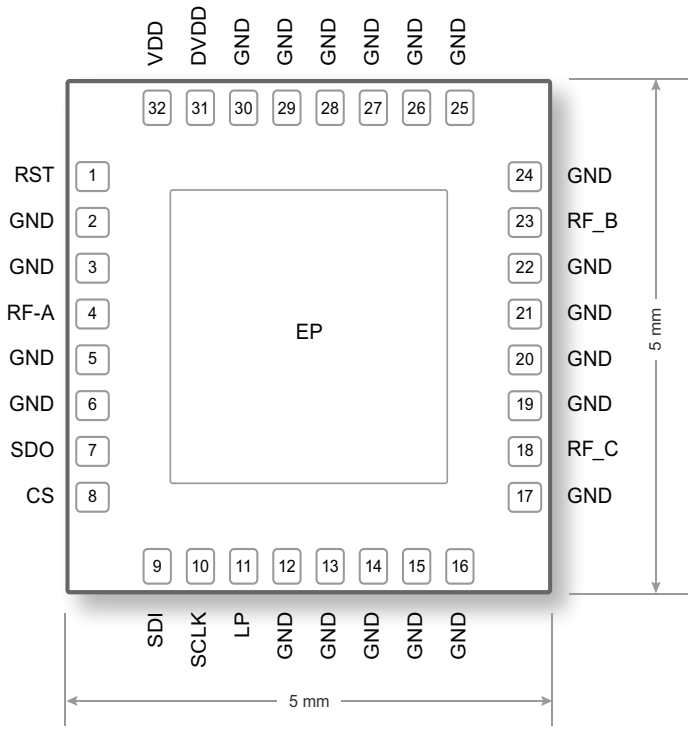


Table 4 • PE44951 Pin Descriptions

Pin No.	Pin Name	Description
–	EP	Exposed ground pad
1	RST	Reset (active low)
2, 3, 5, 6, 12, 13, 14, 15, 16, 17, 19, 20, 21, 22, 24, 25, 26, 27, 28, 29, 30	GND	Ground
4	RF_A	RF input
7	SDO	Serial data output
8	CS	Chip select (active low)
9	SDI	Serial data input
10	SCLK	Serial data clock
11	LP	Latch phase (active high)
18	RF_C	RF output 2
23	RF_B	RF output 1
31	DVDD	Supply voltage for digital
32	VDD	Supply voltage for analog

Evaluation Board Schematic and BOM

Figure 3 shows the evaluation board schematic.**Table 5** lists the evaluation board bill of materials.

Figure 3 • PE44951 Evaluation Board Schematic

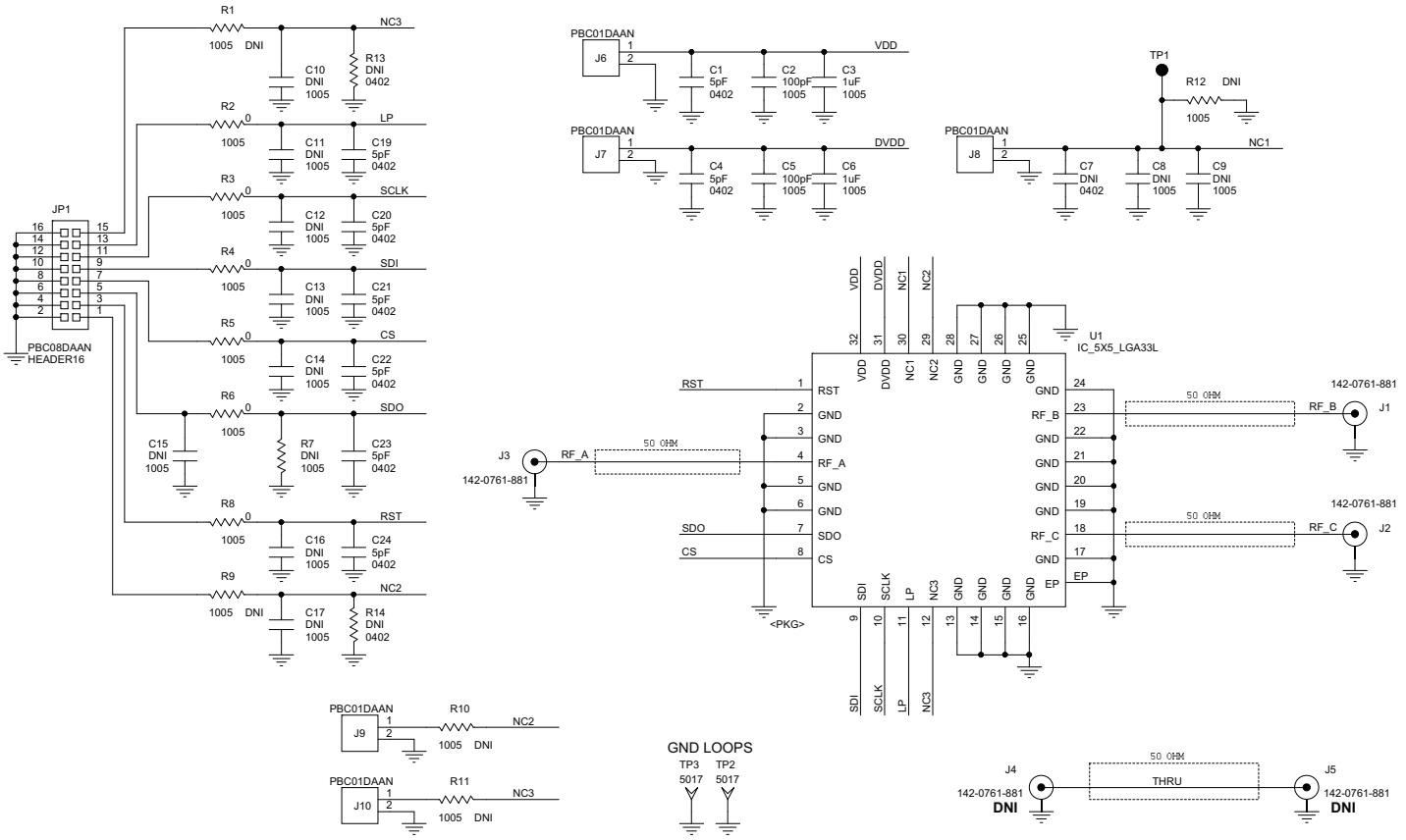


Table 5 • PE44951 Evaluation Board BOM Components

Qty	Reference	Value	Description	Manufacturer	Mfg. part number
8	C1,C4,C19,C20, C21,C22,C23, C24	5 pf	CAP, SMD, CER, 5 pF, 25V, ±5%, C0G, NP0, 01005 (0402 Metric)	Murata Electronics North America	GRM0225C1E5 R0BDAEL
2	C2,C5	100 pf	CAP, SMD, CER, 100 pF, 50V, ±5%, C0G, NP0, 0402 (1005 Metric)	Murata Electronics	GRM1555C1H1 01JA01J
2	C3,C6	1 µf	CAP, SMD, CER, 1 µf, 10V, ±10%, X7R, 0402 (1005 metric)	Murata Electronics North America	GRM155Z71A1 05KE01
1	C7	DNI	CAP, SMD, CER, DNI, n/a, n/a, n/a, 01005 (0402 Metric)	–	–
10	C8,C9,C10,C11, C12,C13,C14, C15,C16,C17	DNI	CAP, SMD, CER, DNI, n/a, n/a, n/a, 0402 (1005 Metric)	–	–
1	JP1	PBC08DAAN	CONN, Rectangular Connectors - Headers, Male Pins, Header Unshrouded Breakaway, TH, Male, 2.54 mm X 2.54 mm, 16 POS	Sullins Connector Solutions	PBC08DAAN
5	J1,J2,J3,J4,J5	142-0761-881	CONN, Coaxial Connectors (RF), SMA, SMD, Jack, Female Socket, 50 Ohm	Cinch Connectivity Solutions Johnson	142-0761-881
5	J6,J7,J8,J9,J10	PBC01DAAN	CONN, Rectangular Connectors - Headers, Male Pins, Header, Breakaway, TH, Male, 2.54 mm, 2 pin	Sullins Connector Solutions	PBC01DAAN
1	PCB1	PCB	PCB, Pirouni LGA EVK	pSemi Corporation	PRT-84425-01
6	R2,R3,R4,R5,R6, R8	0	RES, SMD, Thick Film, 0, Jumper, 1/16W, 0402 (1005 Metric)	Samsung Electro-Mechanics America, Inc.	RC1005J000CS
6	R1,R7,R9,R10, R11,R12	DNI	RES, SMD, Thick Film, DNI, n/a, n/a, 0402 (1005 Metric)	–	–
2	R13,R14	DNI	RES, SMD, Thick Film, DNI, n/a, n/a, 01005 (0402 Metric)	–	–
1	TP1	TESTPAD_ 0p762MM_SMT	CONN, Test Pads, Probe Pad, 0.762 mm dia pad, Testpad SMT, PAD, ICT	–	–
2	TP2,TP3	5017	CONN, Test and Measurement, Test Points, SMD, Male	Keystone Electronics Corp.	5017
1	U1	IC_5X5_ LGA33L	Monolithic Phase and Amplitude Controller	pSemi Corporation	PE44951

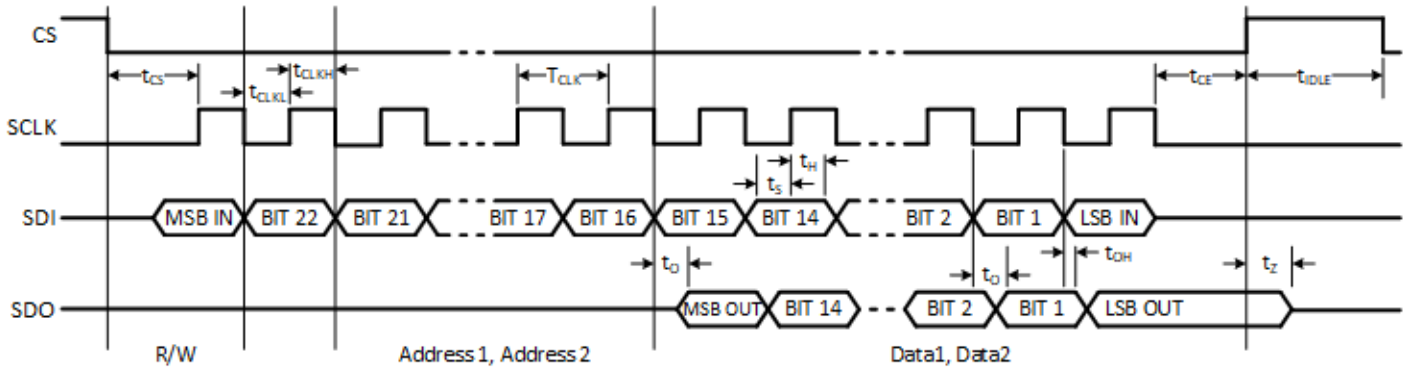
SPI Timing Specifications

Table 6 lists the PE44951 serial-parallel interface (SPI) timing specifications over the recommended operating conditions, unless otherwise specified. **Figure 4** shows the PE44951 SPI timing diagram.

Table 6 • PE44951 SPI Timing Specifications

Parameter	Condition	Min	Max	Unit
SCLK cycle time t_{CLK}		20	–	ns
Command start time t_{CS}		10	–	ns
Command end time t_{CE}		10	–	ns
SCLK low time t_{CLKL}		9	–	ns
SCLK high time t_{CLKH}		9	–	ns
SDI setup time t_S		5	–	ns
SDI hold time t_H		0	–	ns
SDO data valid t_O	C_L = 34 pF on SDO pin	–	6	ns
SDO disable time t_Z		–	5	ns
SDO hold time t_{OH}		0	–	ns
Time between commands t_{IDLE}		10	–	ns

Figure 4 • PE44951 SPI Timing Diagram

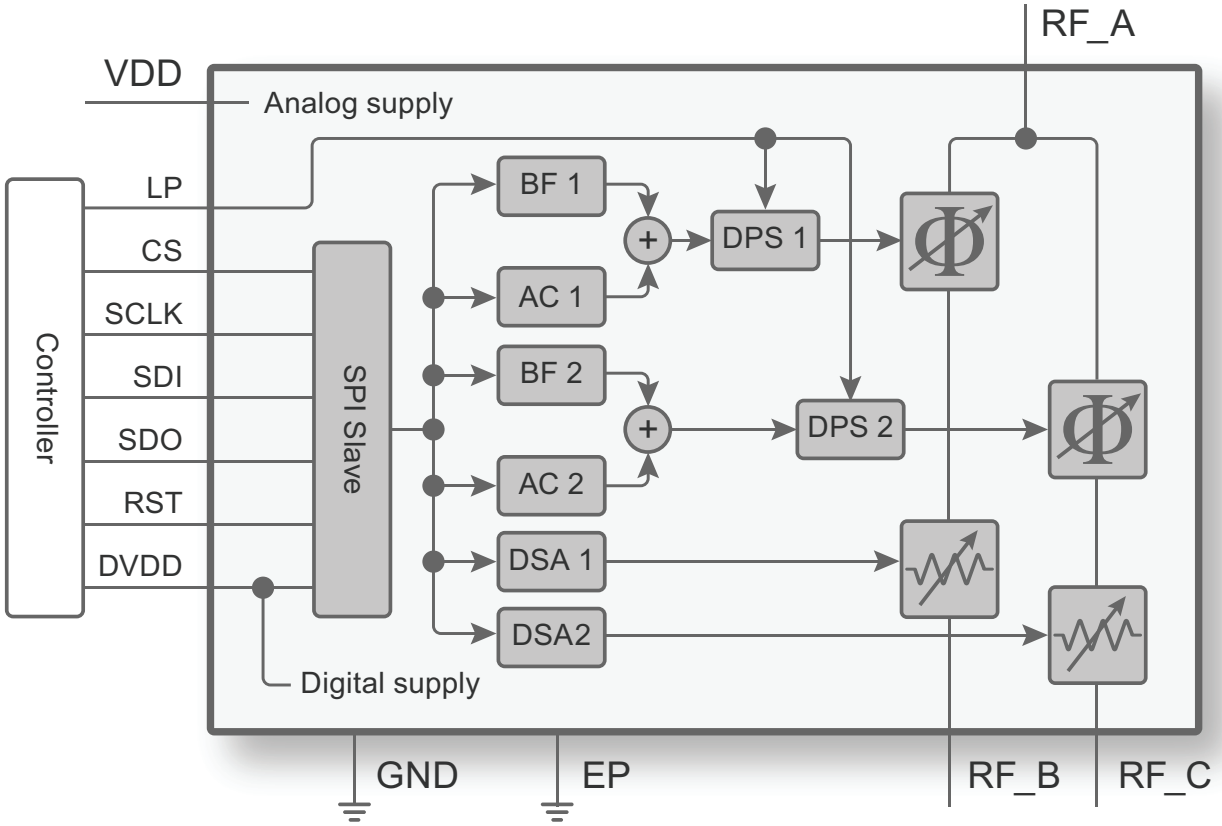


Detailed Description

The PE44951 monolithic phase and amplitude controller implements two RF paths with independent digital phase shift and digital step attenuation. Each phase shift value is set by the sum of an 8-bit beamformer phase buffer and an 8-bit AC phase buffer. These sums are computed automatically by on-chip digital logic. Each attenuation value is set by an 8-bit register. Precise control of the switching time of the phase shifters can be achieved through use of the latch phase (LP) input pin.

Access to the beamformer and AC phase buffers and attenuator control registers is provided through an SPI slave interface operating at up to 50 MHz.

Figure 5 • PE44951 Functional Block Diagram



Beamformer Phase Buffers

There are two 8-bit beamformer (BF) phase buffers BF1 and BF2, one for each path. The typical phase setting is the value of the buffer multiplied by the phase step size: beamformer phase = BF buffer × 1.4°. This gives a typical range for the beamformer phase of 0 (decimal) = 0° to 255 (decimal) = (255 × 1.4°) = 357°.

AC Phase Buffers

There are two 8-bit AC phase buffers AC1 and AC2, one for each path. The typical phase setting for these buffers is the same as for the beamformer buffers: AC phase = AC buffer × 1.4°. This gives a typical range for the AC phase of 0 (decimal) = 0° to 255 (decimal) = (255 × 1.4°) = 357°.

Phase Summation Function

The sum of the BF phase buffer and the AC phase buffer determine the phase shift for each path. This sum is computed on-chip using the function listed in **Table 7**.

Table 7 • Phase Summation

BF phase	–	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AC phase	–	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sum	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Phase	–	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The sum of the two 8-bit values can produce a result requiring 9 bits to store but this potential ninth bit is truncated from the final phase shift value. Therefore, if the sum N of BF phase and AC phase would be greater than 255 (decimal), then the actual phase shift computed would be (N – 256). Translating to typical phase shift using the typical phase step, if the sum N of BF and AC phase would be greater than 357°, then the actual phase shift would be (N – 358.4°). **Table 8** lists a selection of summation results and phase shift values to show this behavior.

Table 8 • Phase Summation Results and Typical Phase Shifts

Sum[8:0]	Sum (decimal)	Phase[7:0]	Phase (decimal)	Typical phase shift	
0 0000 0000	0	0000 0000	0	0 × 1.4°	0°
0 0000 0001	1	0000 0001	1	1 × 1.4°	1.4°
0 0000 0010	2	0000 0010	2	2 × 1.4°	2.8°
…	…	…	…	…	…
0 1111 1110	254	1111 1110	254	254 × 1.4°	355.6°
0 1111 1111	255	1111 1111	255	255 x 1.4°	357°
1 0000 0000	256	0000 0000	0	0 × 1.4°	0°
1 0000 0001	257	0000 0001	1	1 × 1.4°	1.4°
1 0000 0010	258	0000 0010	2	2 × 1.4°	2.8°
…	…	…	…	…	…
1 1111 1101	509	1111 1101	253	253 × 1.4°	354.2°
1 1111 1110	510	1111 1110	254	254 × 1.4°	355.6°

Attenuator Control Registers

There are two 8-bit attenuator control registers DSA1 and DSA2, one for each path. The seven least significant bits of these registers, bits [6:0], set the attenuation for the path. The most significant bit [7] is ignored. The typical attenuation setting is given by the value of bits [6:0] multiplied by the step size: attenuation = DSA[6:0] × 0.125 dB. This gives a typical range for the attenuation of 0 (decimal) = 0 dB to 127 (decimal) = 15.875 dB.

Table 9 lists examples of DSA register values and the resulting typical attenuation.

Table 9 • Example DSA Register Settings and Typical Attenuation

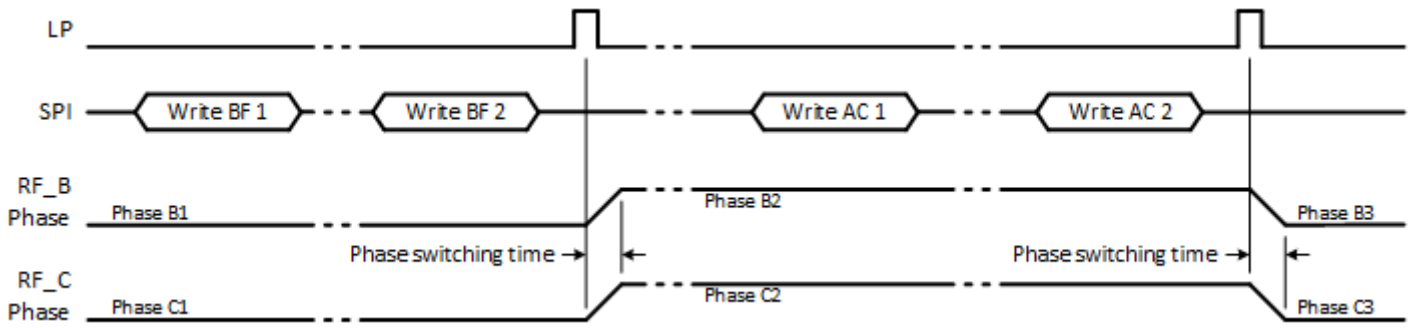
DSA[6:0]	DSA (decimal)	Typ. attenuation		DSA[6:0]	DSA (decimal)	Typ. attenuation
000 0000	0	0 dB		100 0000	64	8.000 dB
000 0001	1	0.125 dB		111 1101	125	15.375 dB
000 0010	2	0.25 dB		111 1110	126	15.75 dB
011 1111	63	7.875 dB		111 1111	127	15.875 dB

Phase Latching

The PE44951 stores the phase shift computed by the phase summation function in D-type latches. The voltage level of the latch phase (LP) input pin determines whether new data enters the latches, or the previous state is maintained. There are separate phase latches for each RF path, both controlled by the LP pin.

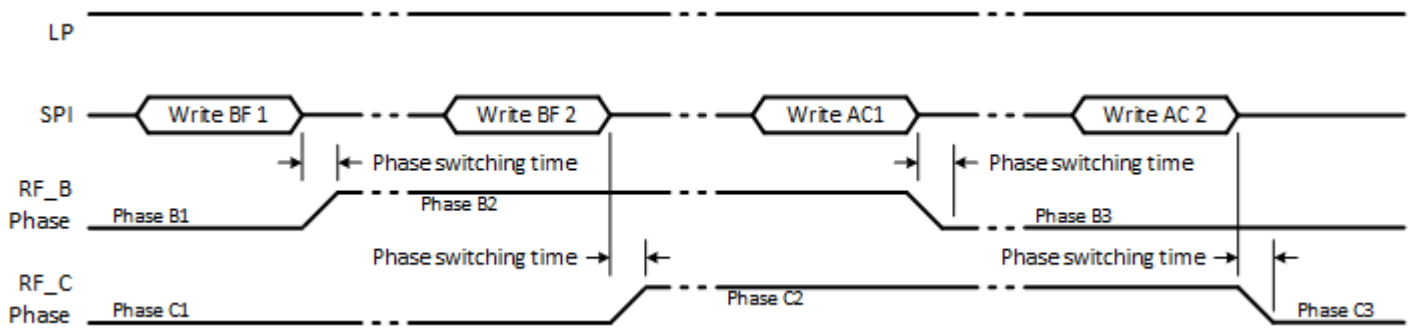
When LP is low, the phase shift is latched in its last state. Writing new data to the beamformer or AC phase buffers while LP is low does not alter the phase shift. When LP is brought high, the phase shift switches to the new value as shown in **Figure 6**. Returning LP low latches this new state.

Figure 6 • Phase Latch Operation



Holding LP high effectively bypasses the phase latches. When LP is held high, the phase shift updates each time a new value is written to the beamformer or the AC phase buffer. **Figure 7** shows this behavior.

Figure 7 • Phase Latch Bypass



Serial Peripheral Interface (SPI)

The PE44951 is compatible with the SPI serial bus specification operating as a slave. SPI transmissions consist of 24-bit write and read commands. One command consists of one read/write (R/W) bit, one unused bit, a 3-bit first address, a 3-bit second address, an 8-bit first data field, and an 8-bit second data field. **Table 10** lists the PE44951 SPI command format. Bit 23 is transmitted first and bit 0 last.

Table 10 • SPI Command Format

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	–	Addr1[2:0]			Addr2[2:0]			Data1[7:0]								Data2[7:0]							

The chip select (CS) input must be low during command transmission. CS resets the interface when high and must be brought high between successive commands.

The interface operates in SPI mode 0. The serial clock (SCLK) input is normally low and is pulsed high once for each bit. Data on SDI is captured on the rising edge of SCLK and register data is shifted out to SDO on the falling edge of SCLK. Address and data fields are transmitted most significant bit first.

SDO is normally in a high-impedance state and is only driven by the PE44951 when the CS input is low. SDO is driven low for the first 8 bits of a read command and for all 24 bits of a write command.

R/W bit low defines a write command. A write command stores the value in the first data field to the register at the first address and the value of the second data field to the register at the second address. If both addresses are the same in a write, then no write occurs and the PE44951 registers remain unchanged.

R/W bit high defines a read command. A read command returns the value of the register at the first address in the first data field and the value of the register at the second address in the second data field. If both addresses are the same in a read, then the same data is returned in both data fields.

Figure 8 • SPI Write Command

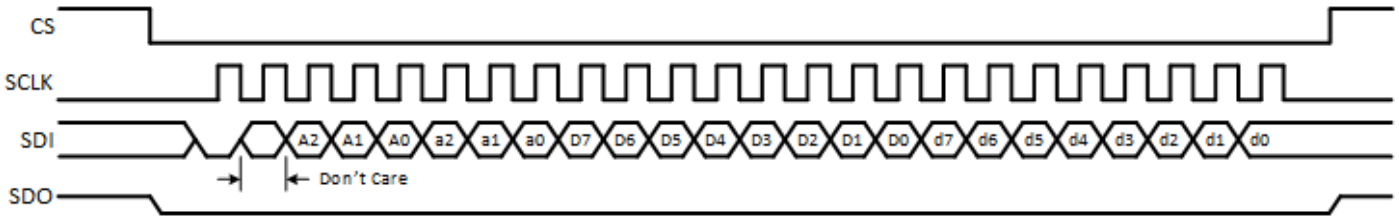
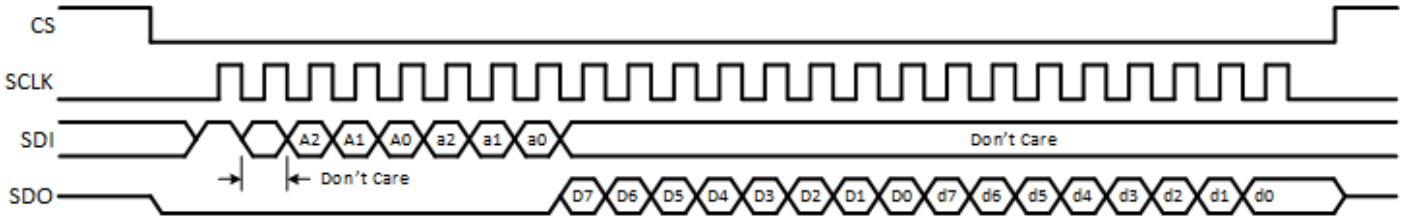


Figure 9 • SPI Read Command



Register Map

Table 11 lists the addresses and bit fields of the PE44951 registers. The default value of all register bits is 0.

Table 11 • PE44951 Register Map

Address	Register	D7/d7	D6/d6	D5/d5	D4/d4	D3/d3	D2/d2	D1/d1	D0/d0
000	BF1	Beamformer phase 1 × 1.4° (typ)							
001	BF2	Beamformer phase 2 × 1.4° (typ)							
010	AC1	AC phase 1 × 1.4° (typ)							
011	AC2	AC phase 2 × 1.4° (typ)							
100	DSA1	Ignored	Attenuator control 1 × 0.125 dB (typ)						
101	DSA2	Ignored	Attenuator control 2 × 0.125 dB (typ)						
110	Unused	Writes ignored, reads 00h							
111	Unused	Writes ignored, reads 00h							

Packaging Information

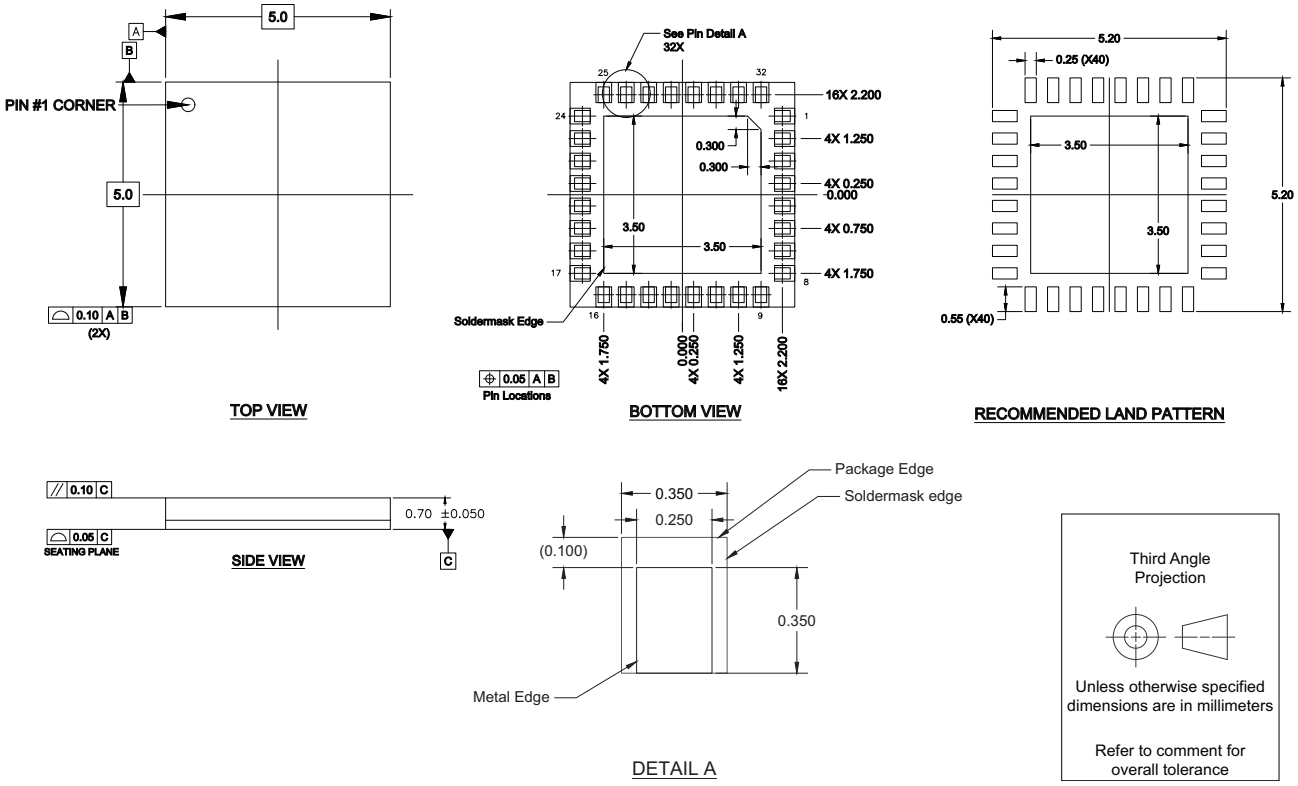
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape and reel information.

Moisture Sensitivity Level

The PE44951 moisture sensitivity level rating for the 32-lead 5 × 5 × 0.7 mm FCLGA package is MSL 3.

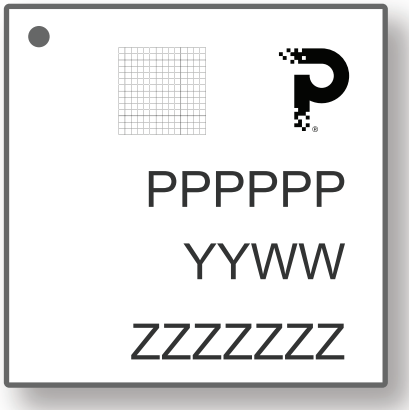
Package Drawing

Figure 10 • Package Mechanical Drawing for the 32-lead 5 × 5 × 0.7 mm FCLGA



Top-Marking Specification

Figure 11 • PE44951 Package Marking Specification

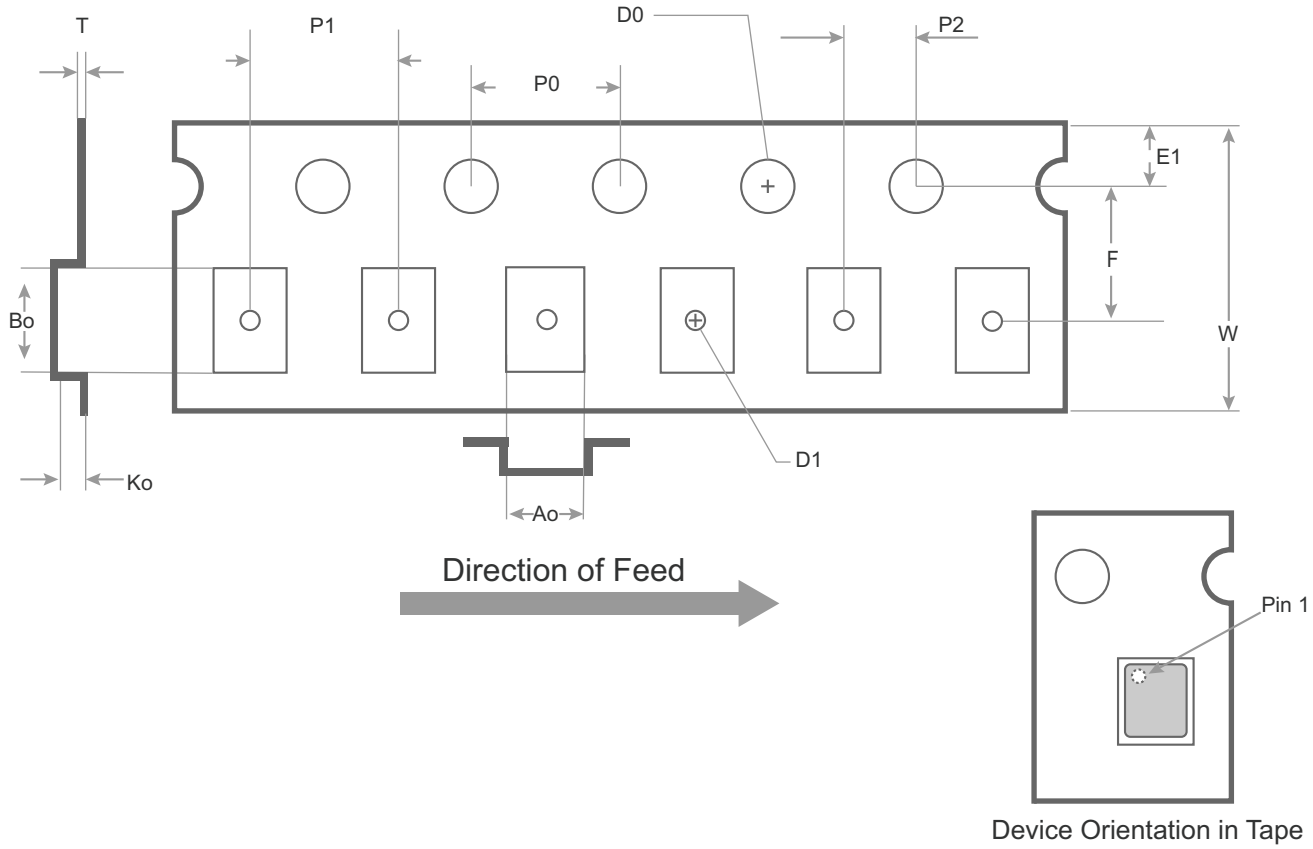


● = Pin 1 indicator
PPPPPP = Product part number
YY = Last two digits of assembly year (2022 = 22)
WW = Work week of assembly lot start date (01, ..., 52)
ZZZZZZZ = Assembly lot code (max six characters)

DOC-114717-1

Tape and Reel Specification

Figure 12 • Tape and Reel Specification for the 32-lead 5 × 5 × 0.7 mm FCLGA



Notes:

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Table 12 • Tape and Reel Dimensions

Carrier Tape Dimensions					
Pocket	**Nominal**	**Tolerance**	**Pocket**	**Nominal**	**Tolerance**
Ao	5.25	±0.05	**D1**	1.00	±0.05
Bo	5.25	±0.05	**D0**	1.50	+0.10/-0.0
Ko	0.85	±0.05	**E1**	1.75	±0.10
P1	8.00	±0.10	**P0**	4.00	±0.10
W	12.00	+0.30/-0.10	**P2**	2.00	±0.05
F	5.50	±0.05	**T**	0.30	±0.05

Ordering Information

Table 13 • PE44951 Order Codes and Shipping Methods

Order codes	Description	Packaging	Shipping method
PE44951A-Z	Monolithic Phase and Amplitude Controller	32-lead 5 × 5 × 0.7 mm FCLGA	3000 units/tape and reel
EK44951-01	PE44951 Evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark