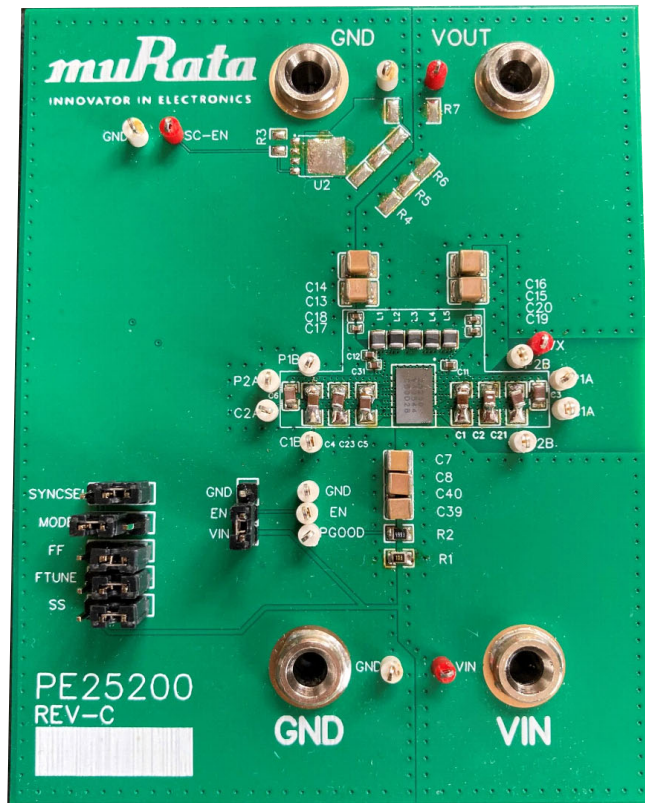


# Evaluation Kit User's Manual

### *Divide-by-2 and -3, 10A Charge Pump, Capacitor Divider*



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## Introduction

The PE25200 is an ultra-high efficiency DC-DC converter solution that you can configure to divide down an input voltage by two or three and deliver up to 45W output at up to 95.4% peak efficiency. The PE25200 supports the following input voltages and is available in a wafer-level chip scale package (WLCSP):

- 10V maximum in divide-by-2 mode
- 15V maximum in divide-by-3 mode

The PE25200 evaluation kit (EVK) is intended and made available for evaluation and testing purposes only.

## Evaluation Kit Overview

The PE25200 evaluation kit (EVK) is a hardware platform that allows customers to test the step-down DC-DC converter. High-current connections are through 4-mm sockets (banana plug style) with test hoops for connecting sensing and test equipment probes. Several customer-adjustable PCB headers can be used to invoke alternate operational modes. For more information about the PE25200, see the *PE25200 Data Sheet*.

## Document Overview

This *PE25200 Evaluation Kit (EVK) User's Manual* includes information about the external hardware required to control and evaluate the DC-DC converter functionality.

## EVK Contents and Requirements

### Kit Contents

Table 1 lists the hardware required for evaluation.

*Table 1. EVK Contents*

Quantity	Description	Part Number
1	PE25200 DC-DC converter evaluation board assembly	PE25200-REV-C

### Hardware Requirements

To evaluate the performance of the evaluation board, the following equipment is required:

- Bench DC power supply capable of providing 10V–15V at 5A minimum with sense lines
- Two high-accuracy digital multimeters
- Four-channel oscilloscope with probes (optional to view waveforms)
- Electrical load)

**Warning:** The PE25200 EVK contains components that could be damaged by exposure to voltages higher than the maximum specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals, or to signal inputs and outputs.

Note that the input is at the **bottom** of the board marked **GND** and **VIN** in bold, as shown in Figure 1.

Before you connect the EVK to the source power supply, verify that the power supply is off. Connecting the EVK to a live power supply could induce failures. Also verify that the output load is disconnected.

## Quick Start Guide

The evaluation board is designed to ease your evaluation of the PE25200 DC-DC converter. This section guides you through the hardware configuration and the start-up procedures.

### Evaluation Board Overview

The evaluation board contains the following:

- Input/output terminals
- Test point hoops provide voltage sense points and connections for voltmeters, oscilloscopes, and the like.
- PCB headers with jumpers to change the mode of operation

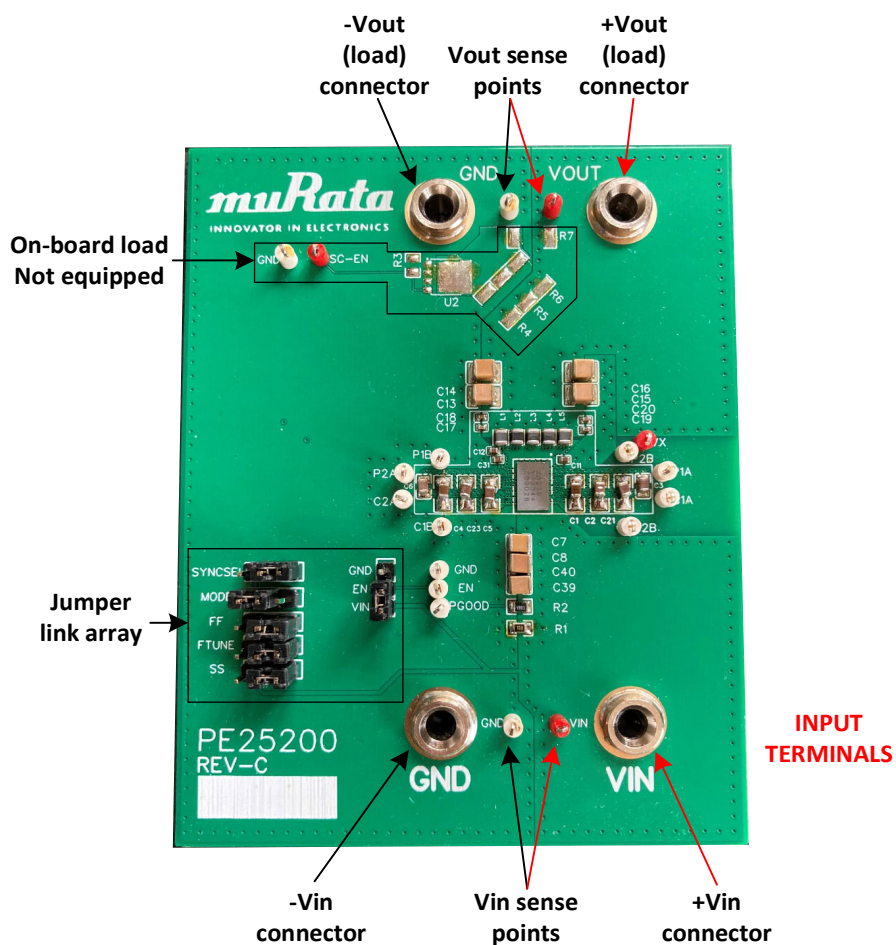


Figure 1. PE25200 Evaluation Board Assembly

## PCB Header Jumper Settings

The enable (EN) jumper settings enable the EVK by connecting the EN pin directly to the VIN potential. You can drive the EN pin externally by connecting a DC voltage potential between EN and GND.

Table 2. VIN and Enable (EN) Function

VIN	Function
< 0.4V	Disabled
> 1.3 V	Enabled

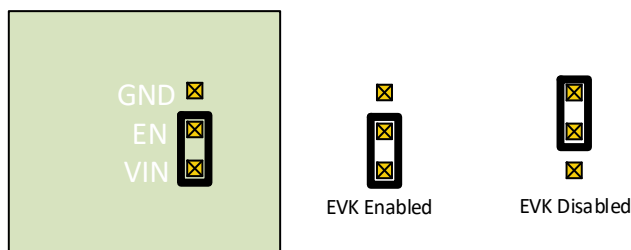


Figure 2. Enable (EN) Jumper Settings

Table 3 lists information about the remaining three-way PCB headers.

Table 3. Three-way PCB Headers Information

Signal	Function	Notes
SYNCSEL	Not functional for this version of the EVK	–
MODE	Sets the VIN-to-VOUT ratio by divide-by-2 or divide-by-3	<ul style="list-style-type: none"> <li>VIN divide-by-2 max = 10V</li> <li>VIN divide-by-3 max = 15V</li> </ul>
FF	Sets fixed, asynchronous, or cycle skip operation	All pins open (with no installed jumpers) have functionality.
FTUNE	Sets nominal, plus 15% or minus 15% of operational frequency	All pins open (with no installed jumpers) have functionality.
SS	Sets the soft start current at 600 mA, 2.1A, or 1.1A	All pins open (with no installed jumpers) have functionality.

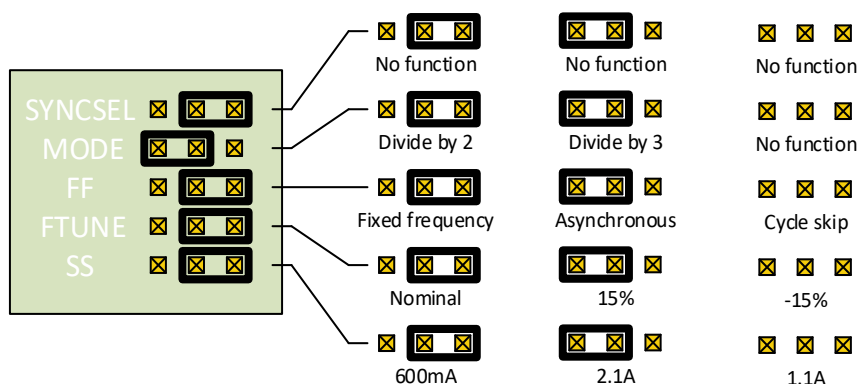
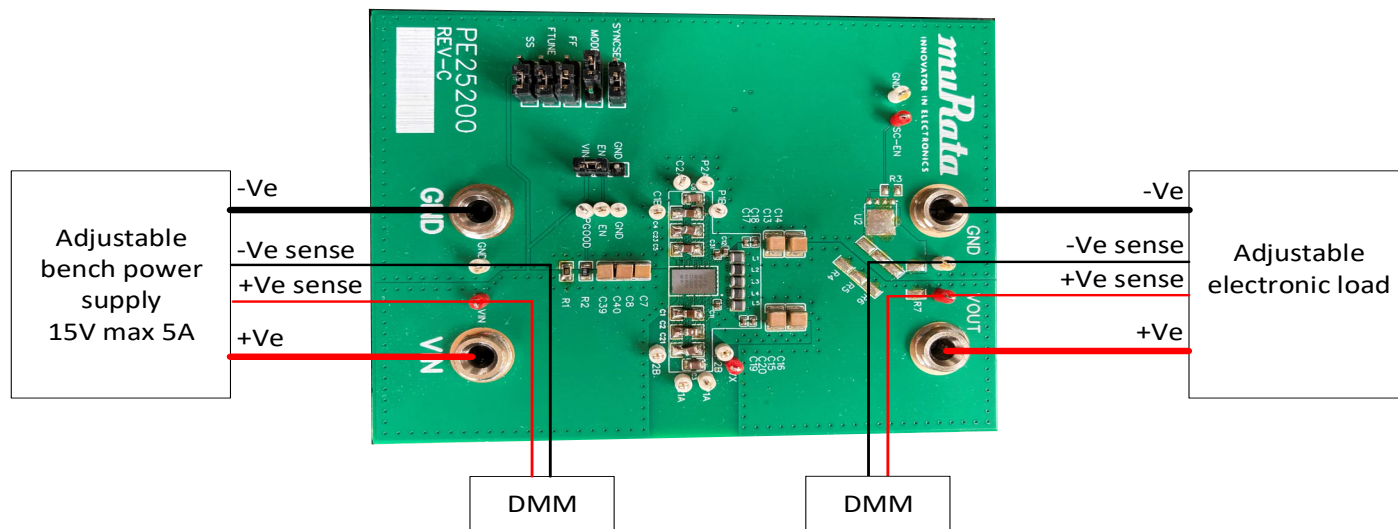


Figure 3. Typical Jumper Settings and Options

## EVK Connection

Connect the EVK and the measuring equipment as shown in *Figure 4*.



*Figure 4. EVK Connection Example*

## Hardware Operation

This section includes the general guidelines for operating the EVK. To configure the EVK and achieve optimal performance, follow these steps:

1. Verify that the jumpers are set for the preferred mode and division ratio.
2. Apply the input voltage to the input terminals.
3. Apply the output load after the PGOOD signal goes high.

Figure 5 shows the typical startup sequence traces.

- Yellow trace = 15V from source
- Green trace = PGOOD
- Blue trace = VOUT



Figure 5. Typical Startup Sequence

## EVK Startup

When starting the EVK, start it with no load.

If the EVK starts with a load, it might not start due to the soft-start current limit being exceeded.

## Test Results

Figure 6–Figure 17 show the typical performance of the PE25200 evaluation board.

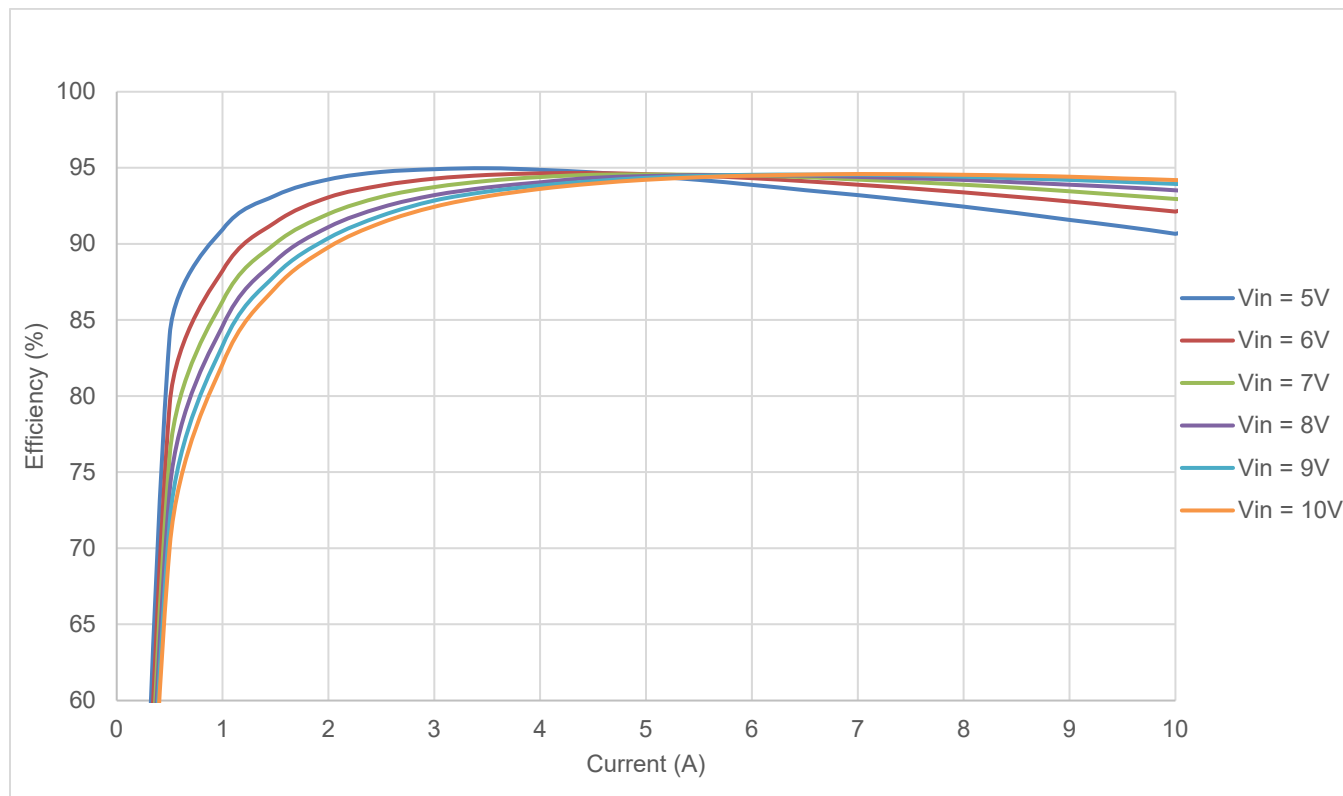


Figure 6. Divide-by-2 Internal Sync Efficiency vs. Output Current



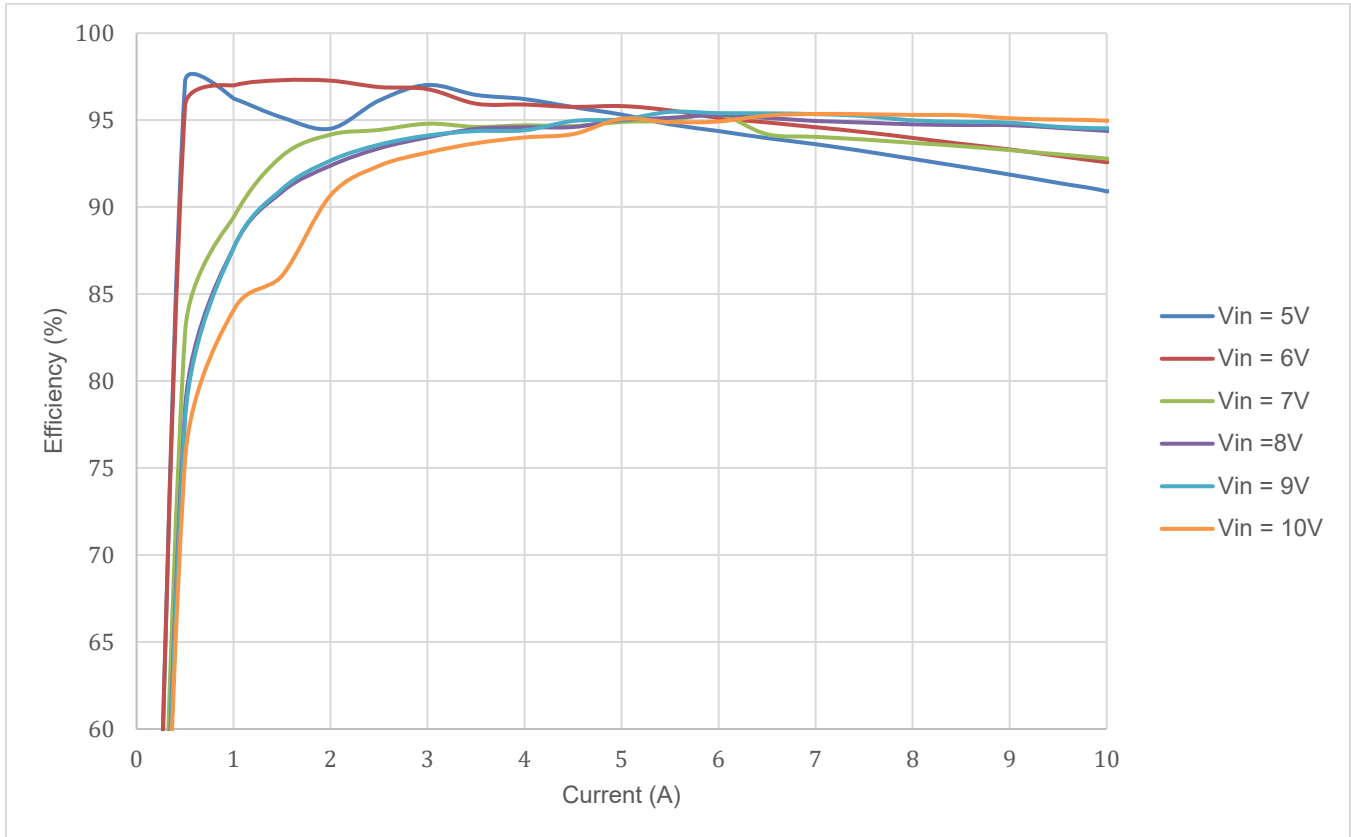


Figure 7. Divide-by-2 Internal Sync Cycle Skip Efficiency vs. Output Current

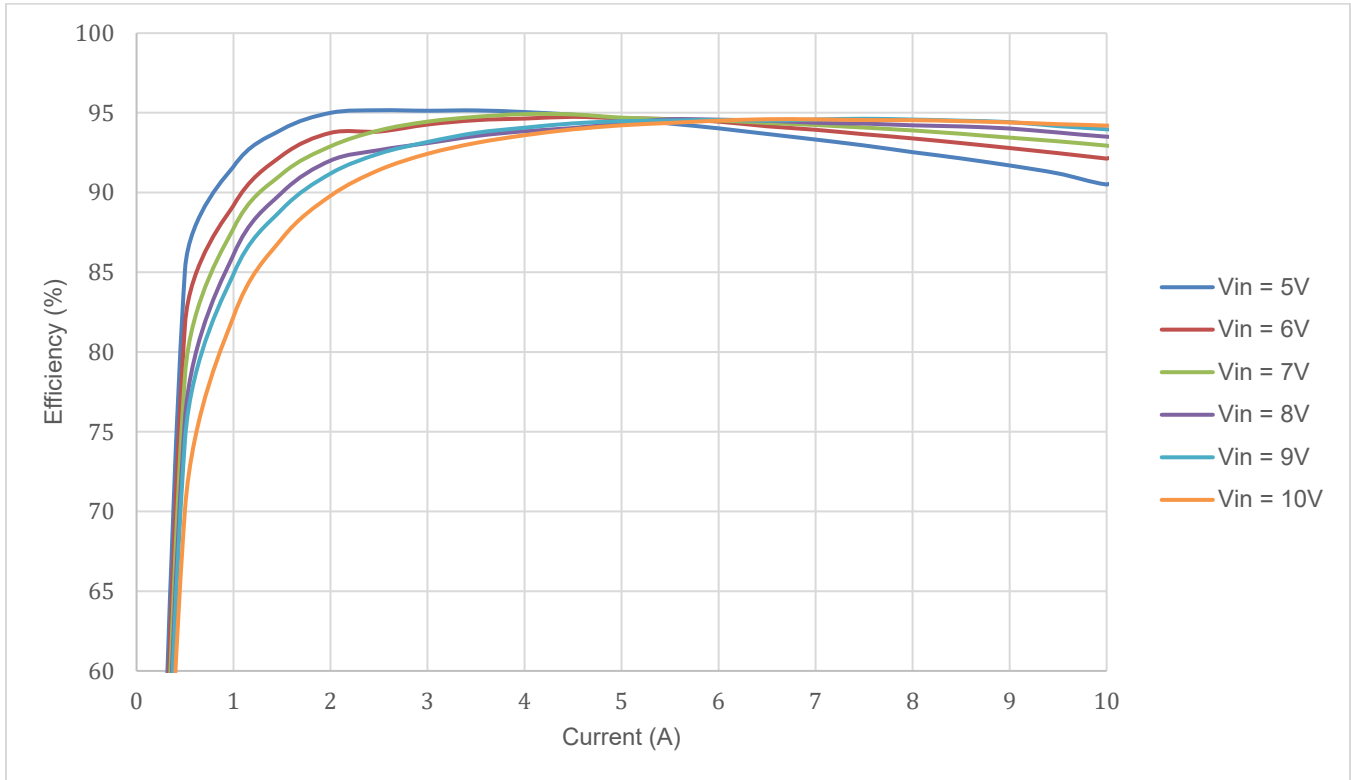


Figure 8. Divide-by-2 Internal Sync Async Efficiency vs. Output Current

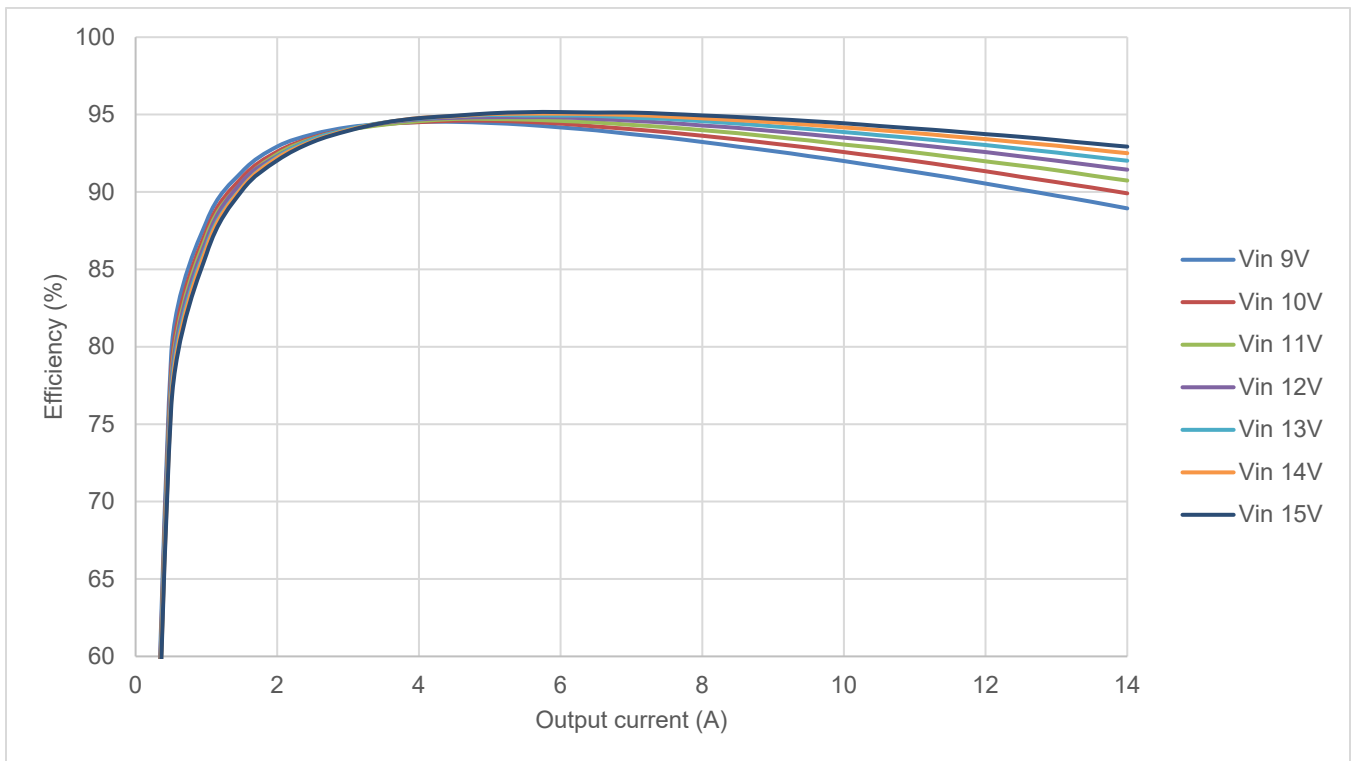


Figure 9. Divide-by-3 Internal Sync Efficiency vs. Output Current

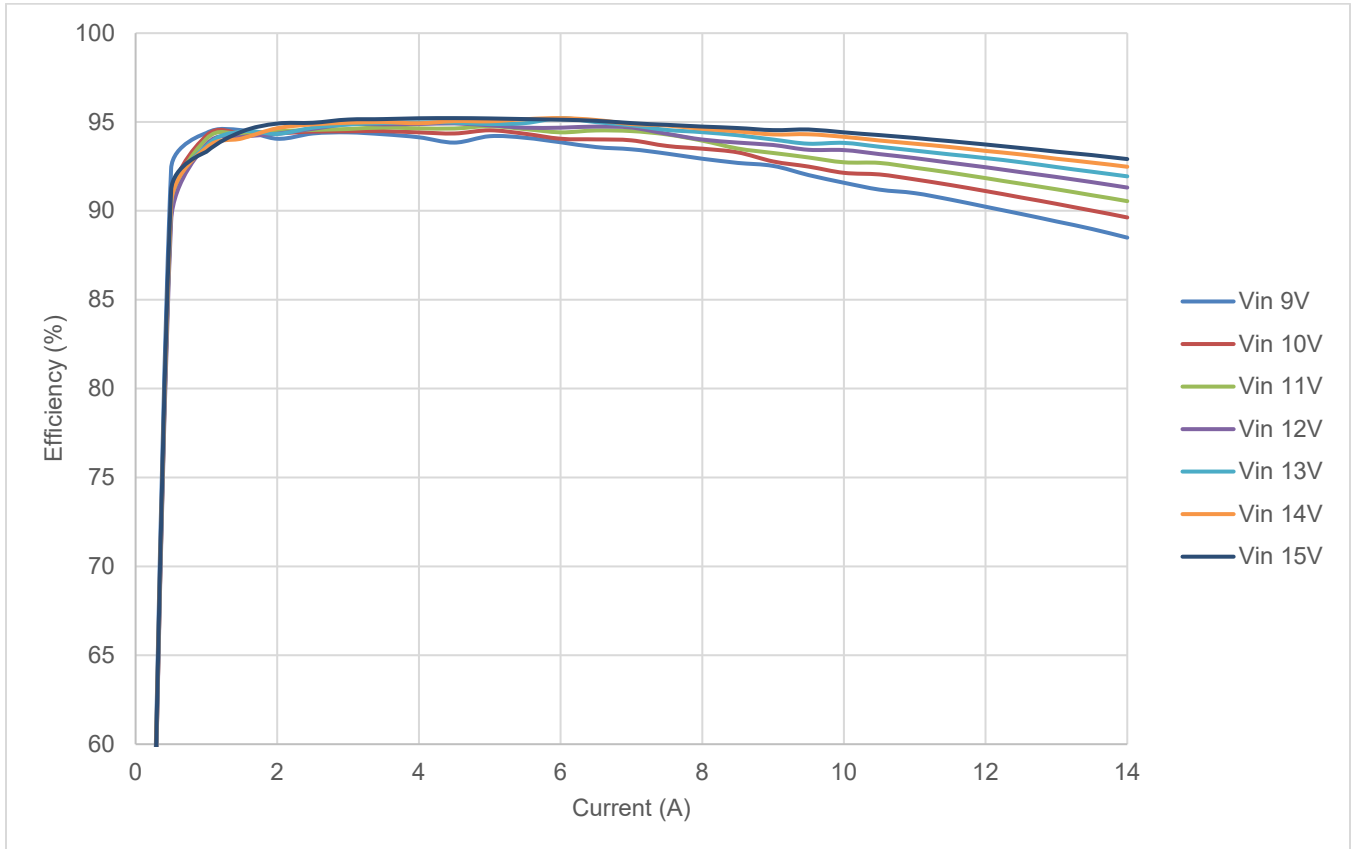


Figure 10. Divide-by-3 Internal Sync Cycle Skip Efficiency vs. Output Current

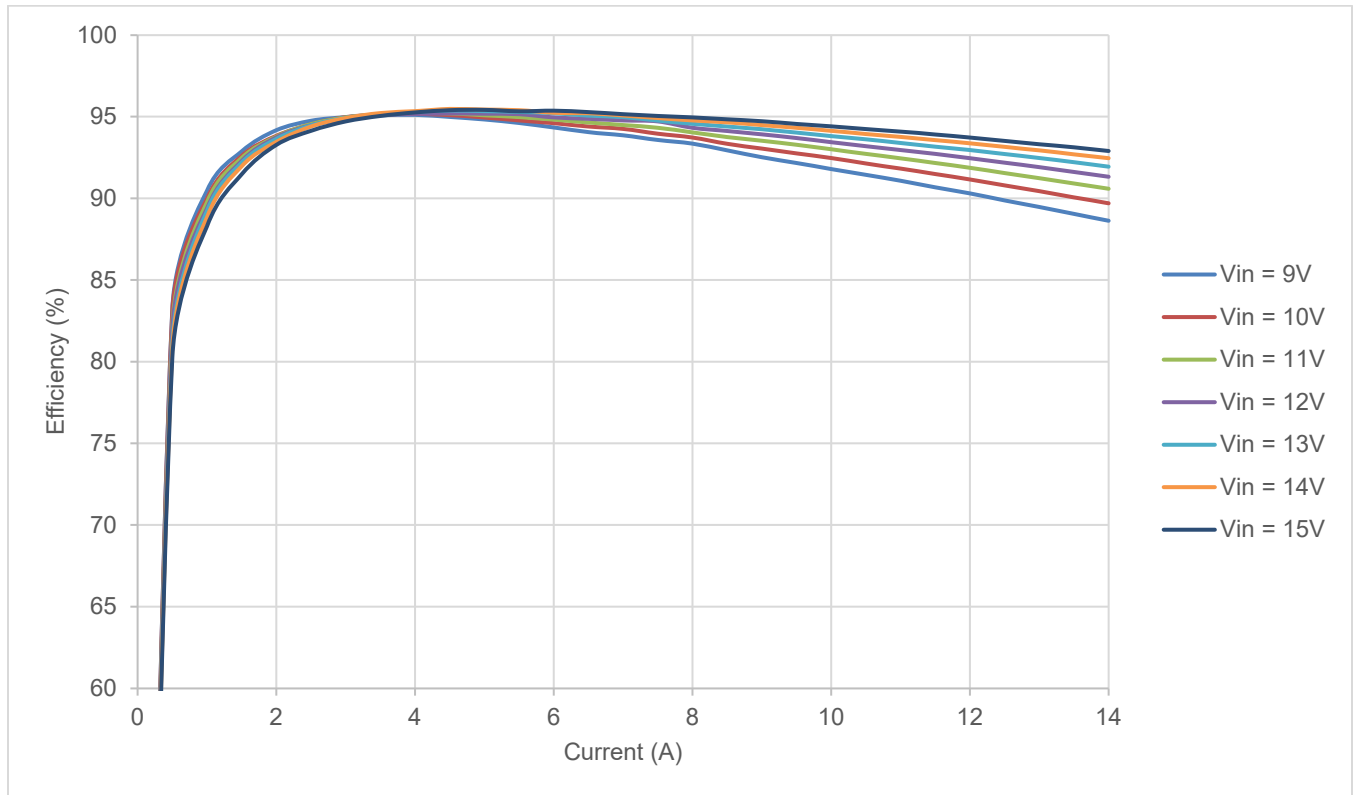


Figure 11. Divide-by-3 Internal Sync Async Efficiency vs. Output Current

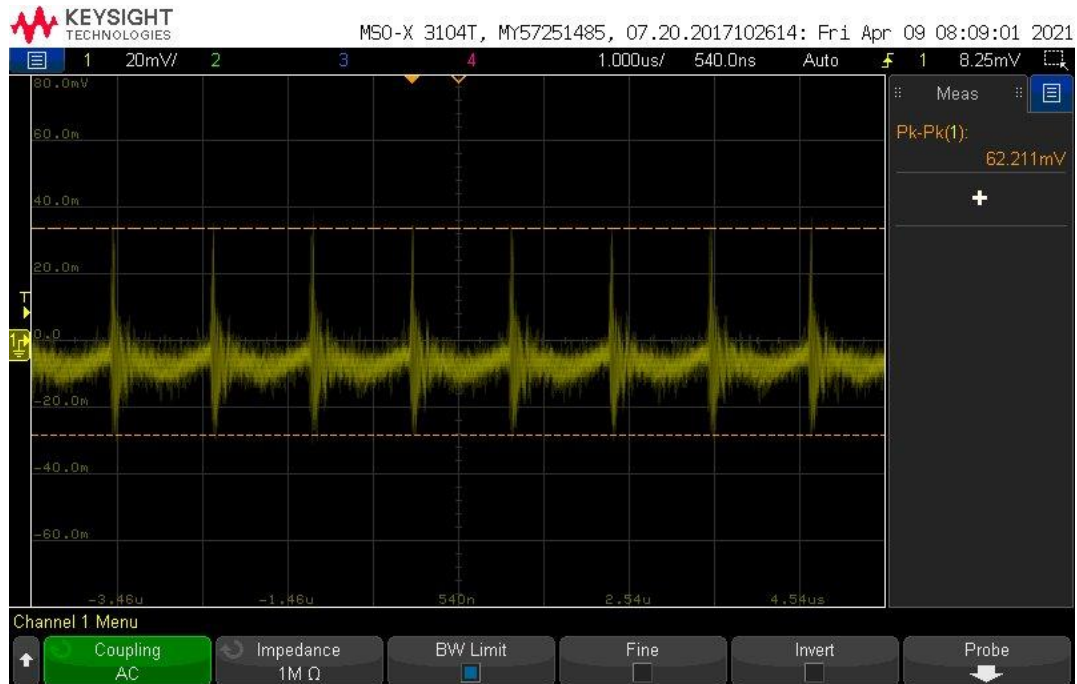


Figure 12. Output Ripple Divide-by-3, No Load

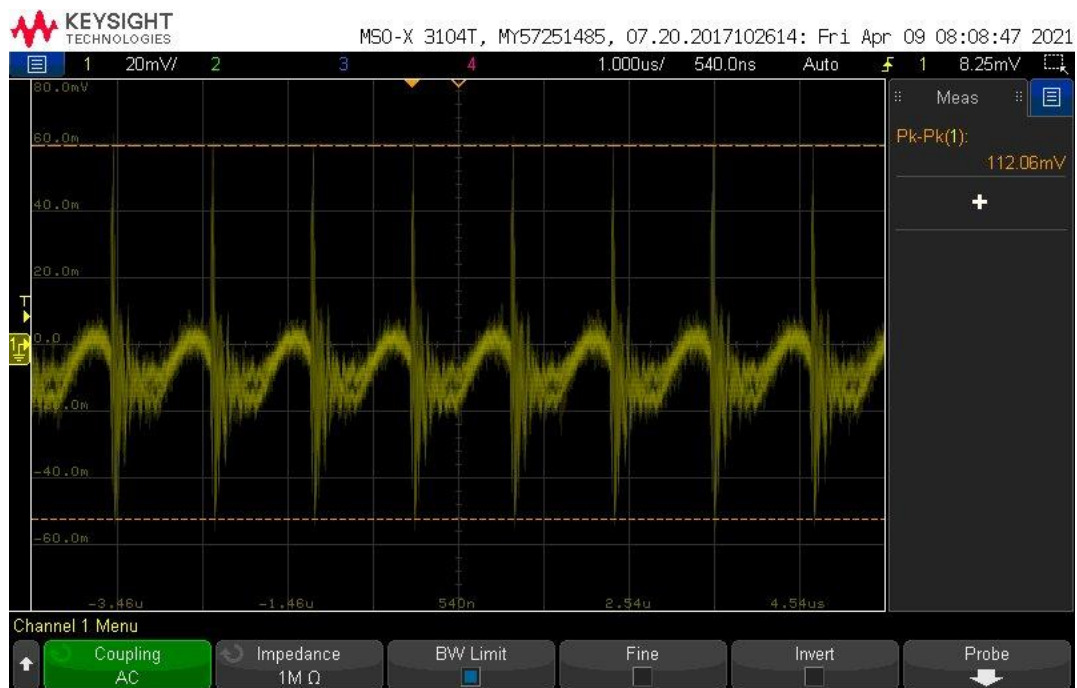
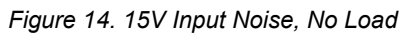


Figure 13. Output Ripple Divide-by-3, 10A



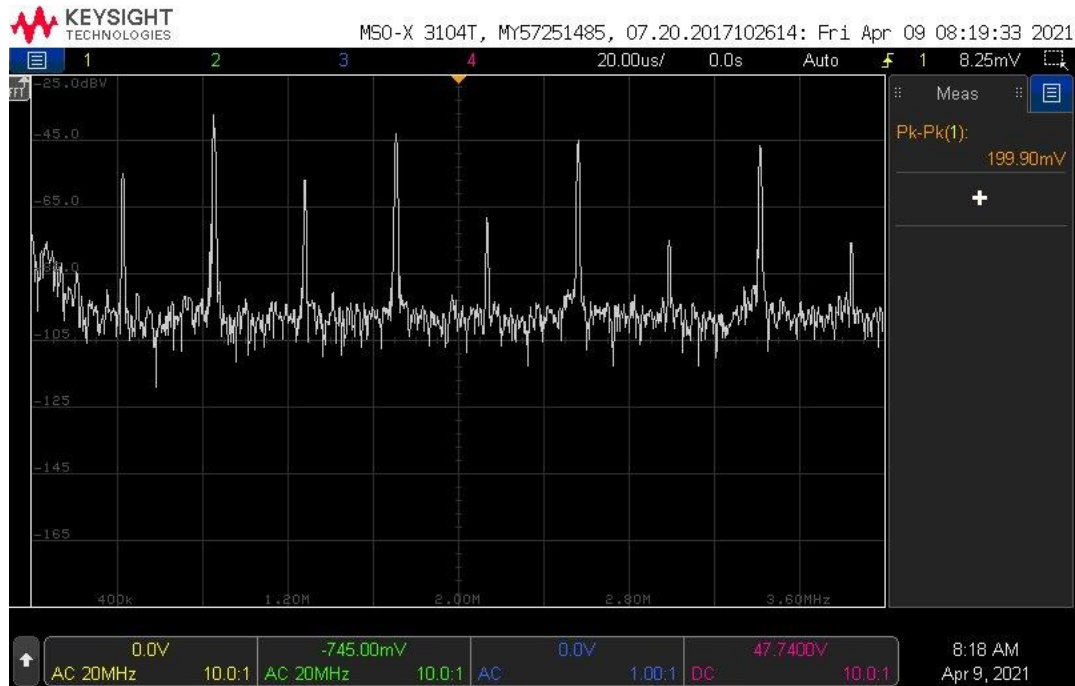


Figure 16. 15V Input Noise, 10A



Figure 17. 15V Output Noise, 10A

Figure 18 shows a 1A to 9A dynamic load applied at 1 kHz. The output voltage variation is typically 400 mV.

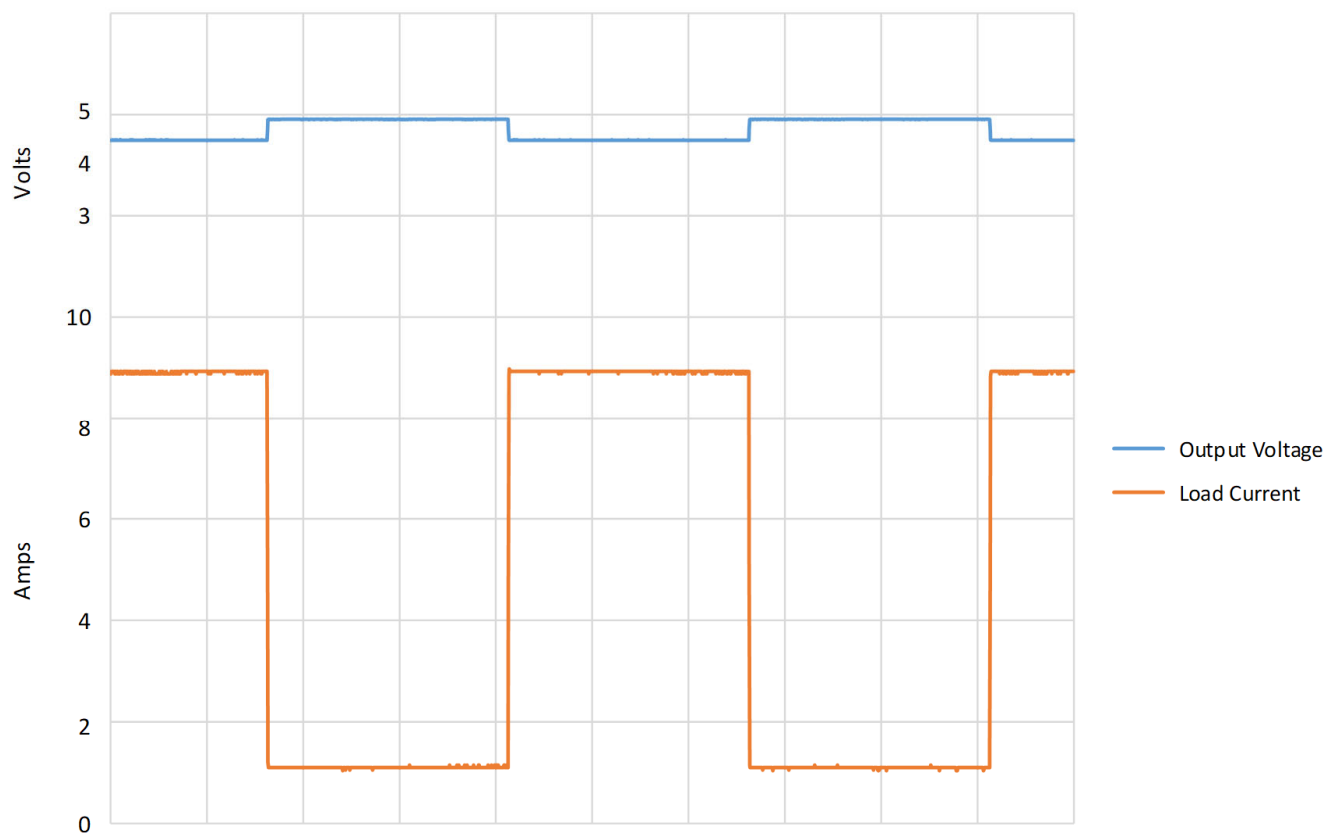


Figure 18. Transient Load Response

For more waveforms and test data, see the *PE25200 Data Sheet*.



## PCB Layout Information

Figure 19–Figure 22 show a Type-III PCB evaluation board layout example using a 4-layer board.

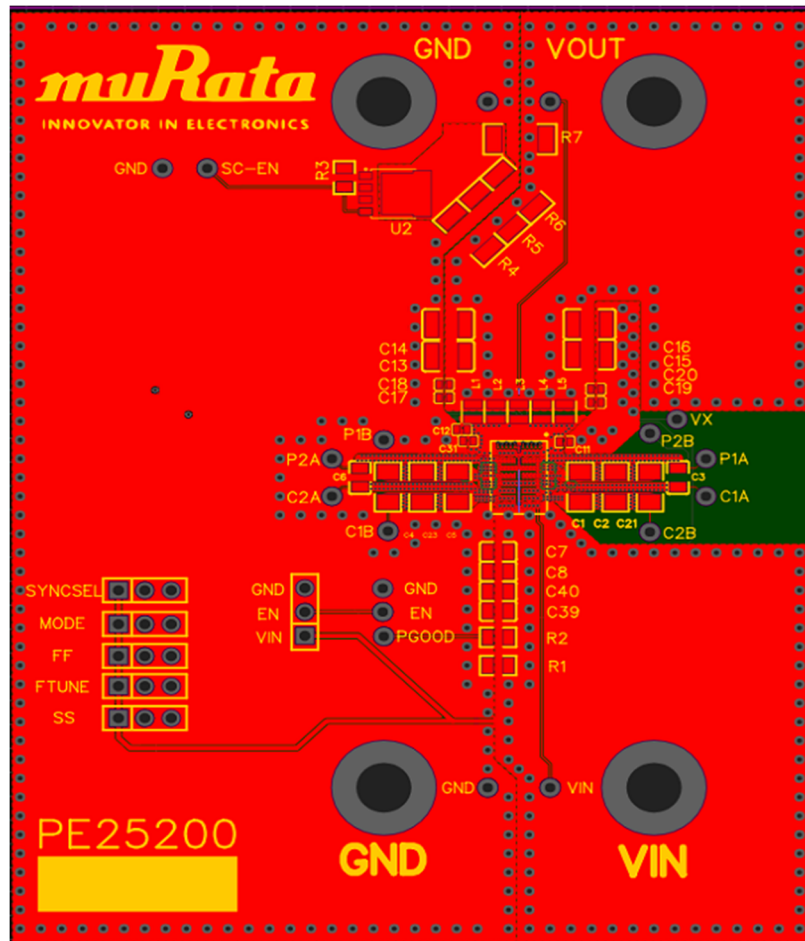


Figure 19. Top Layer

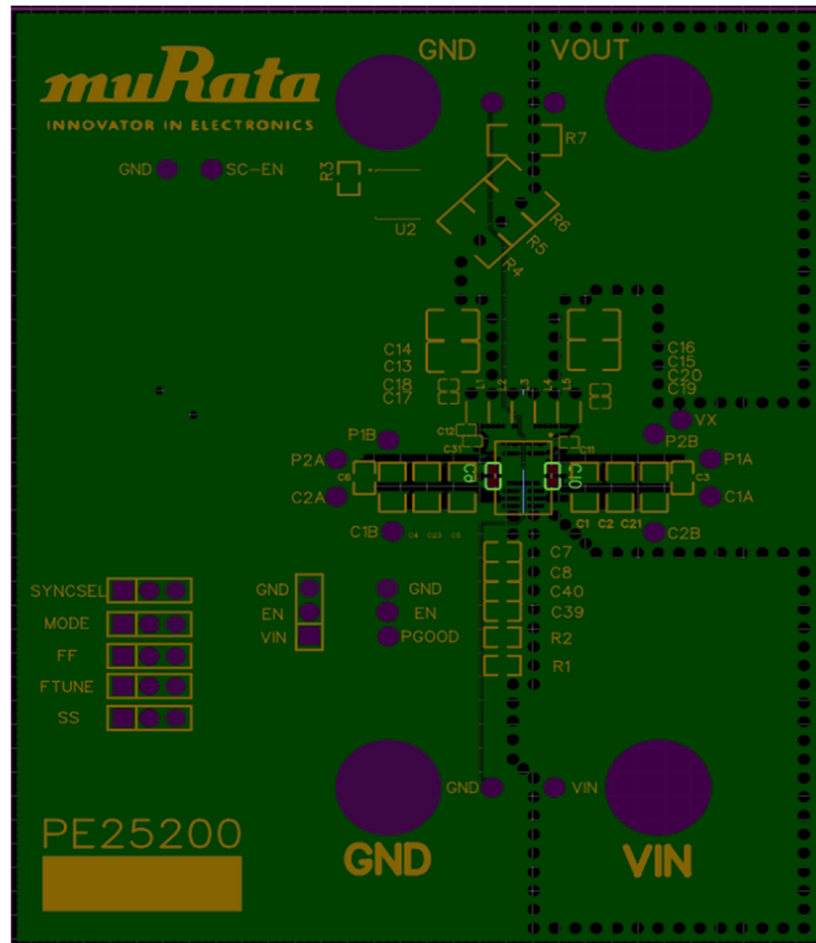
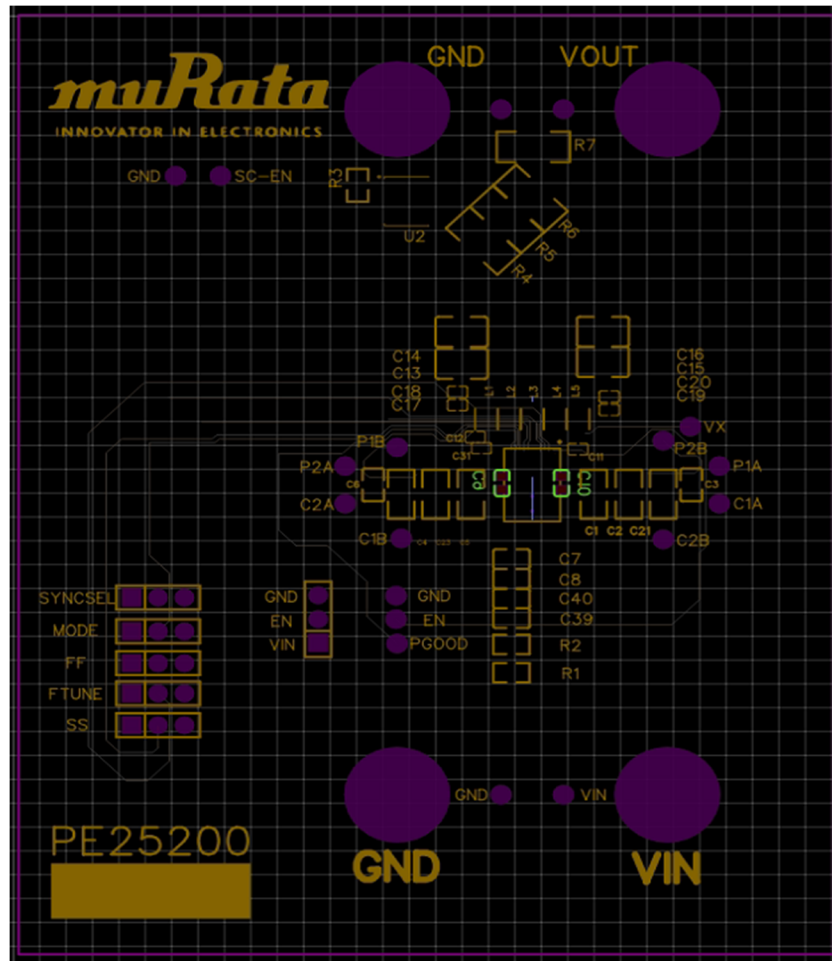


Figure 20. Inner Copper Layer 1



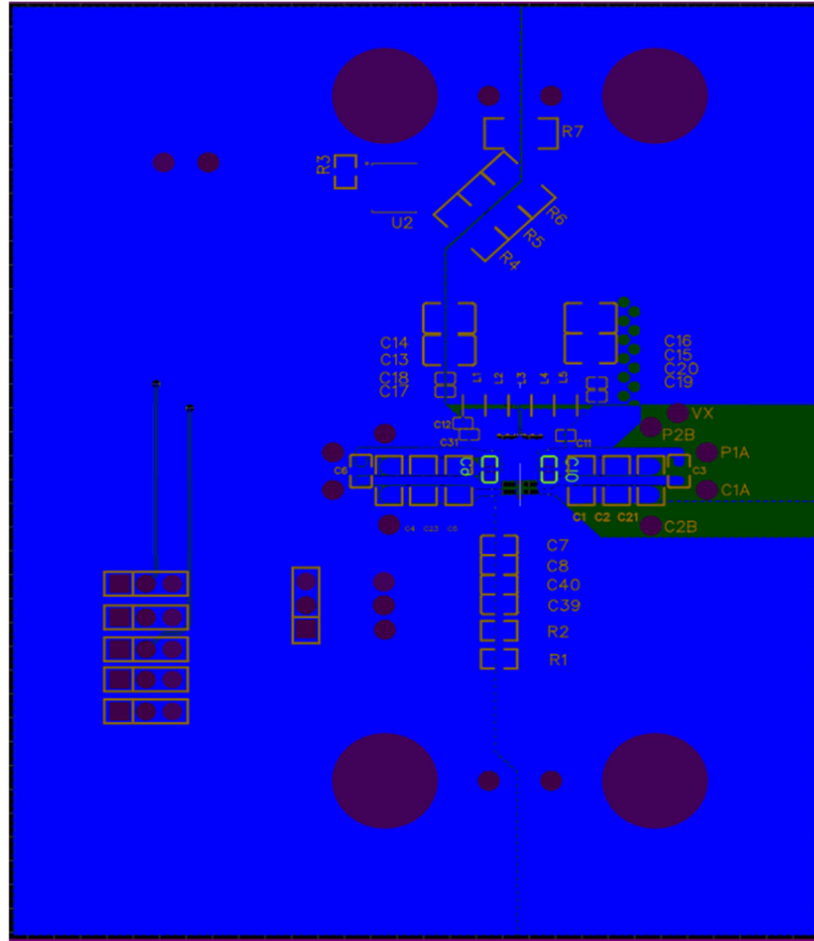


Figure 22. Bottom Copper Layer

## EVK PCB Schematic

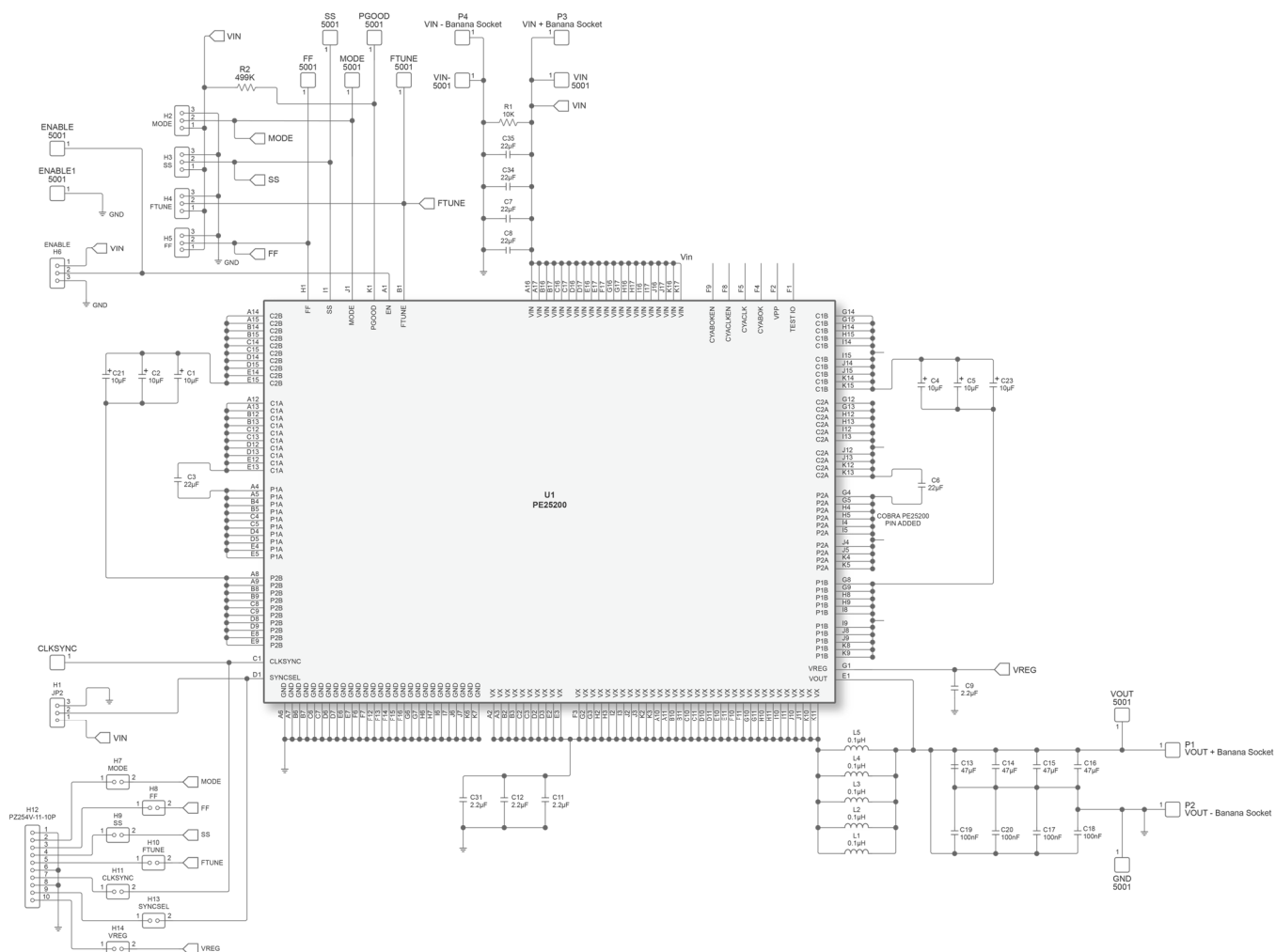


Figure 23. Evaluation Board Schematic

## Application Circuit Part List

Table 4 lists the recommended components.

Table 4. Recommended Components

Reference	Value	Description	Mfr. part number
C1, C2, C4, C5, C21, C23	10 $\mu$ F	CAP, SMD, CER, 10 $\mu$ F, 16V, +/-10%, X7S, 0805 (2012 Metric)	GRM21BC71C106KE11L
C3, C6	22 $\mu$ F	CAP, SMD, CER, 22 $\mu$ F, 6.3V, +/-20%, X7T, 0805 (2012 Metric)	GRM21BD70J226ME44L
C7, C8, C34, C35	22 $\mu$ F	CAP, SMD, CER, 22 $\mu$ F, 25V, +/-20%, X6S, 1206 (3216 Metric)	GRM31CC81E226ME11L
C9, C11, C12, C31	2.2 $\mu$ F	CAP, SMD, CER, 2.2 $\mu$ F, 10V, +/-10%, X7R, 0402 (1005 Metric)	GRM155C71A225KE11D
C13–C16	47 $\mu$ F	CAP, SMD, CER, 47 $\mu$ F, 6.3V, +/-10%, X7R, 1210 (3225 Metric)	GCM32ER70J476KE19L
C17–C20	0.1 $\mu$ F	CAP, SMD, CER, 0.1 $\mu$ F, 25V, +/-20%, X7R, 0402 (1005 Metric)	GRM155R71E104ME14D
C1A, C1B, C2A, C2B, CLK, CYABOK, CYABOKEN, CYACLK, CYACLKEN, EN_TP, FF, FTUNE, MODE, P1A, P1B, P2A, P2B, PGOOD, SS, TESTIO, VPP	5002	CONN, Test Points, PC Test Point, Miniature, Test Point TH, Male, THM, 5002 - White	5002
C22, C24, C27, C30	DNI	DNI	DNI
C25, C26, C28, C29	DNI	DNI	DNI
JP2, JP6, JP7, JP15–JP18	TSW-103-07-G-S	CONN, Rectangular Connectors - Headers, Male Pins, Header, TH, Male, TSW, (3-POS)	TSW-103-07-G-S
L1–L5	0.1 $\mu$ H	IND, SMD, Multilayer - Power - Automotive, LQM2MPZ_JH, 0.1 $\mu$ H, 4000mA(85 C), 3000mA(125 C), 0.019 Ohms, 0806 (2016 metric)	LQM2MPZR10MJH
P1	PREC010S AAN-RC	CONN, Rectangular Connectors - Headers, Male Pins, Header, TH, Male, 0.100" (2.54mm), 10 POS	PREC010SAAN-RC
PCB1	PCB	MISC, DOC, PCB, PE25200 DEVICE EVK	PRT-72806-01
R1	10K	RES, SMD, Thick Film, 10K, +/-1%, 1/8W, 0805 (2012 metric)	CRCW080510K0FKEA
R2	499K	RES, SMD, Thick Film, 499K, +/-1%, 1/8W, 0805 (2012 Metric)	CRCW0805499KFKEA
R3, R4	DNI	DNI	DNI
TP1	5016	CONN, Test Points, PC Test Point, Compact, Test Point SMD, Male	5016
U1	PE25200	IC, SMD, pSemi IC, BGA	EK.25200-HDI

## Technical Resources

Additional technical resources are available for download in the Products section at [www.psemi.com](http://www.psemi.com). These include the product specification datasheet, S-parameters, zip file, evaluation kit schematic, bill of materials, material declaration form, and PC-compatible software file.

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