PE42448

Evaluation Kit User's Manual

High-linearity UltraCMOS© SP4T RF Switch, 10 MHz–6 GHz

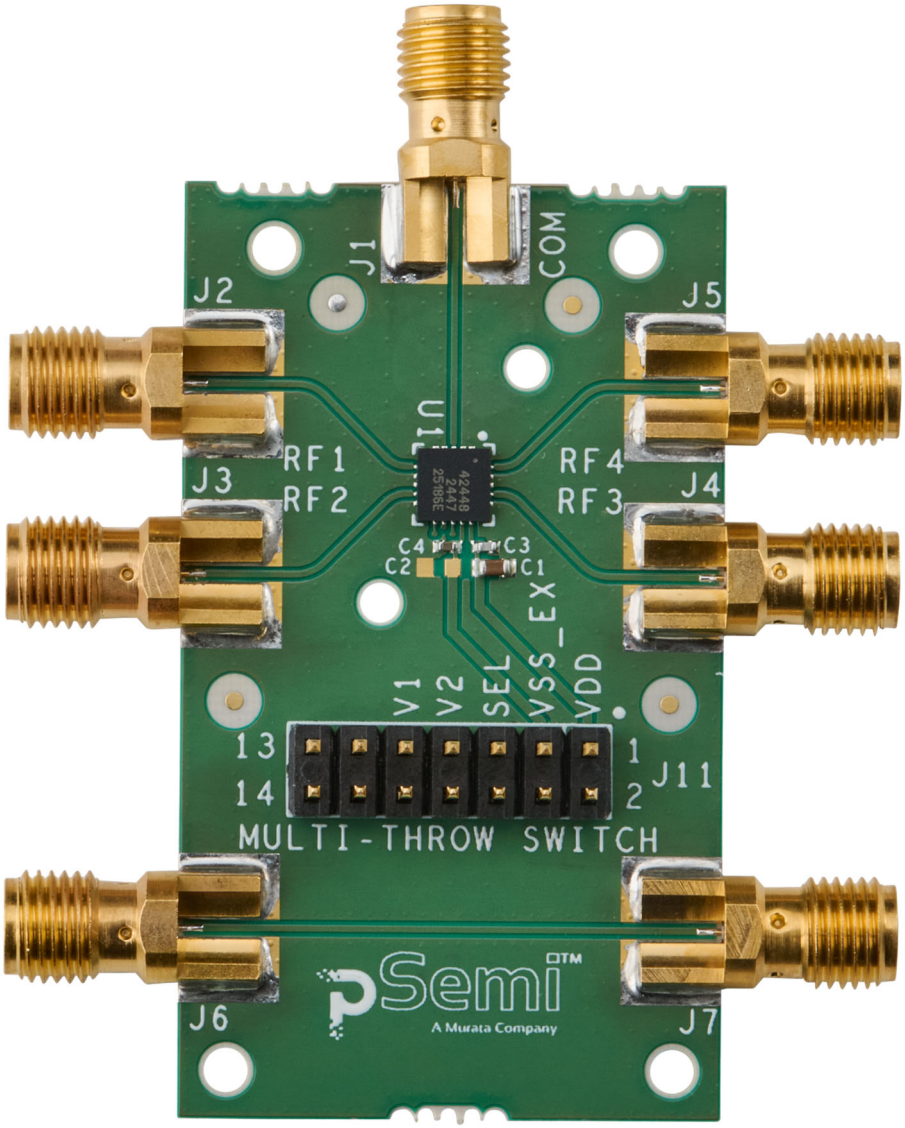

Table of Contents

Introduction

The PE42448 is a HaRP™ technology-enhanced SP4T RF switch that supports a frequency range from 10 MHz to 6 GHz. It delivers extremely low insertion loss and high linearity with a high input power handling capability, making this device ideal for hybrid analog beamforming and for 5G massive multi-input multi-output (MIMO) applications. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42448 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology. pSemi's HaRP technology enhancements deliver high isolation, linearity, and excellent harmonics performance.

The PE42448 evaluation kit (EVK) is intended and made available for evaluation and testing purposes only.

Evaluation Kit Overview

The PE42448 EVK is a hardware platform that allows you to easily test the SP4T RF switch. For more information about the PE42448, see the *PE42448 Data Sheet*.

Document Overview

This *PE42448 Evaluation Kit (EVK) User's Manual* includes information about the hardware required to control and evaluate the high-linearity SP4T RF switch functionality.

EVK Contents and Requirements

Kit Contents

Table 1. EVK Contents

Quantity	Description	Part Number
1	High-linearity UltraCMOS© SP4T RF Switch, 10 MHz–6 GHz, evaluation board assembly	PRT-88620-01

Hardware Requirements

To test the performance of the evaluation board, you will need the following test equipment:

- Vector network analyzer
- Vector signal generator
- Signal/spectrum analyzer

You will also need 50Ω loads to terminate any unused RF connectors.

Warning: The PE42448 EVK contains components that could be damaged by exposure to voltages higher than the maximum specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals, or to signal inputs and outputs.

Quick Start Guide

The evaluation board is designed to ease your evaluation of the PE42448. This section guides you through the hardware configuration and testing procedures.

Evaluation Board Overview

The evaluation board EVB is assembled with the following:

- PE42448 high-linearity SP4T RF switch
- One PCB header
- Seven SMA connectors

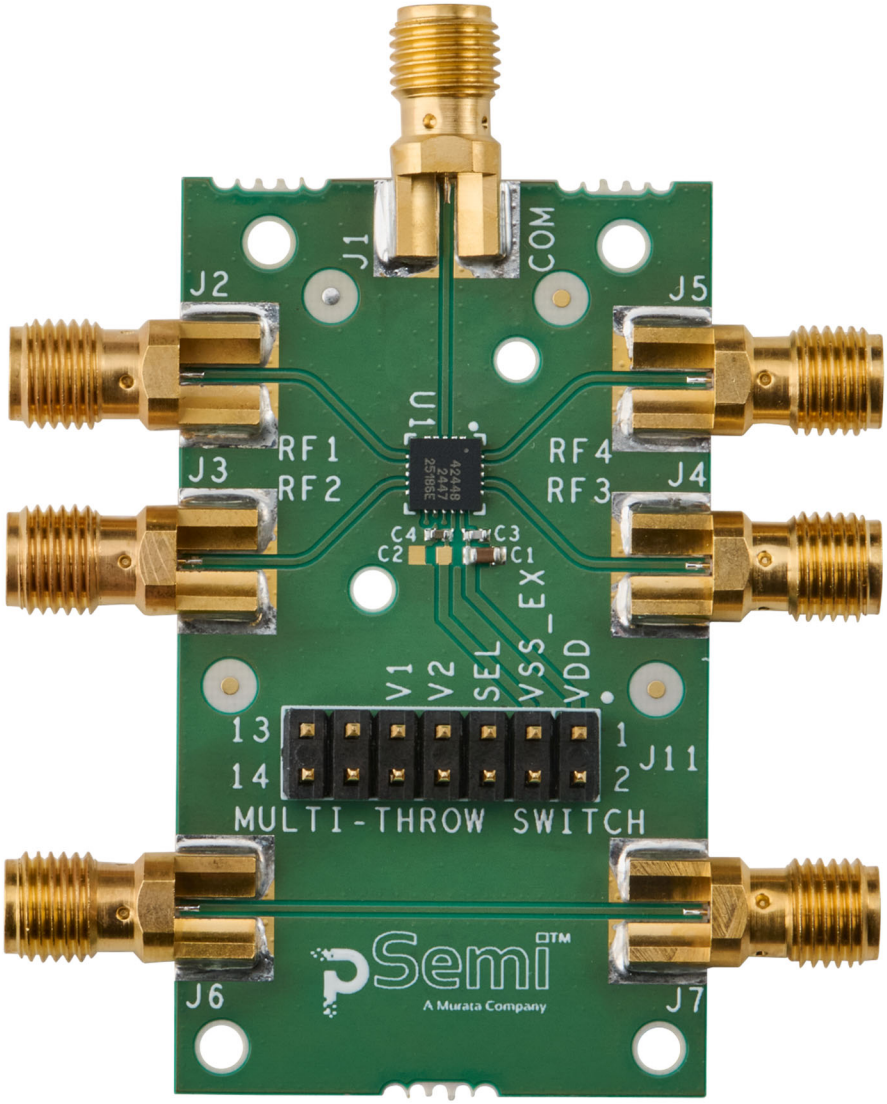

Figure 1. PE42448 Evaluation Board Assembly

Evaluation Board Schematic

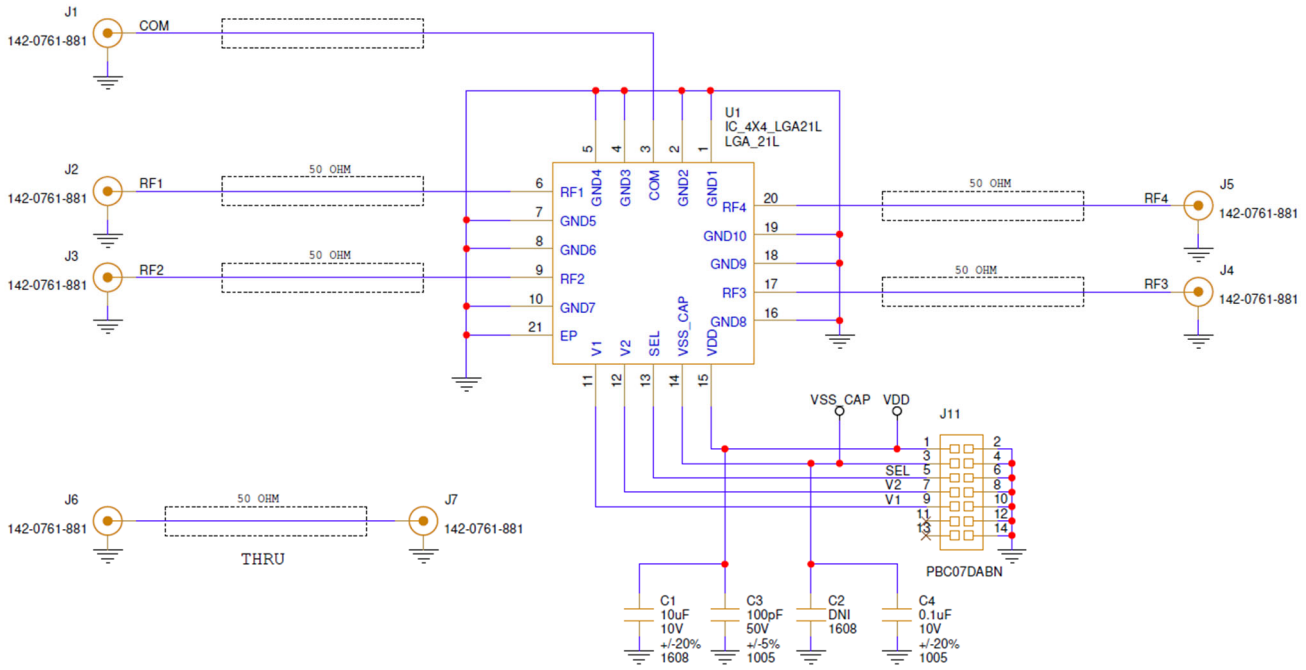

Figure 2. PE42448 Evaluation Board Schematic

Bill of Materials

Table 2. PE42448 Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part number	Description	Size
C1	10 uF	Murata Corporation	GRM188D71A106MA73D	CAP, SMD, CER, XR7	0603 (1608 Metric)
C2	DNI	–	–	–	0603 (1608 Metric)
C3	100 pF	Murata Corporation	GRM1555C1H101JA01D	CAP, SMD, CER, C0G	0402 (1005 Metric)
C4	0.1 uF	Murata Corporation	GRM155R61A104MA01D	CAP, SMD, CER, XR5	0402 (1005 Metric)
J1, J2, J3, J4, J5, J6, J7	–	Cinch Connectivity	142-0761-881	CONN, COAX, SMA, JACK, FEMALE, 50 OHM	–
J11	–	Sullins Connector	PBC07DABN	CONN, RECT Headers, MALE Pins, 14 POS	–
PCB1	–	pSemi Corporation	PRT-88621-01	PCB	–
U1	–	pSemi Corporation	PE42448	SP4T RF switch	4 × 4 mm

Hardware Configuration

When testing the PE42448 evaluation board, the RF signals, DC power, and control signals are easily connected using J1, J2, RFC, and RF1–4 on the PCB assembly.

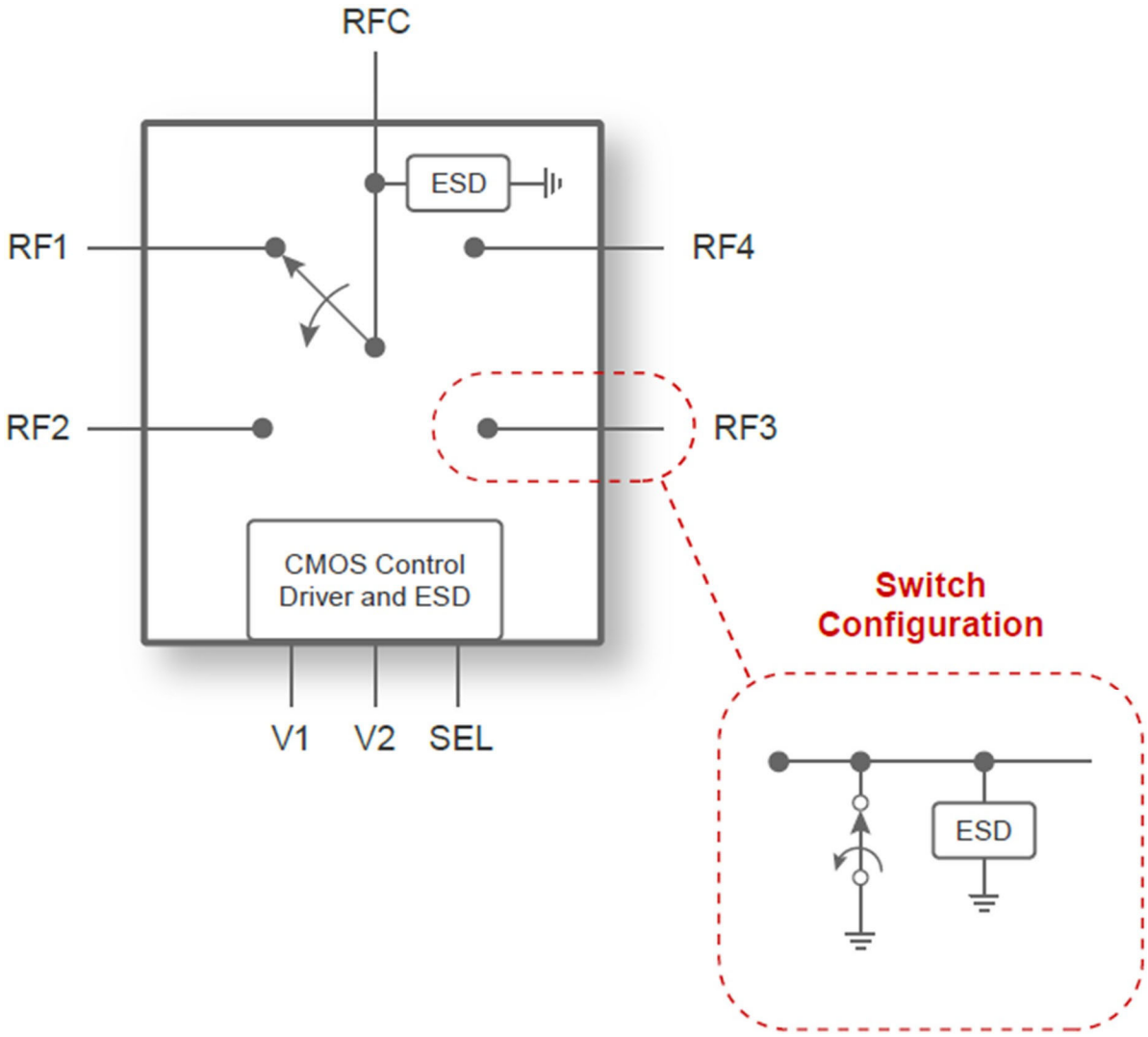

Figure 3. PE42448 Block Diagram

Pin Configuration

Figure 4 shows the PE42448 pin map for the 20-lead 4 × 4 mm LGA package, and Table 3 lists the description for each pin.

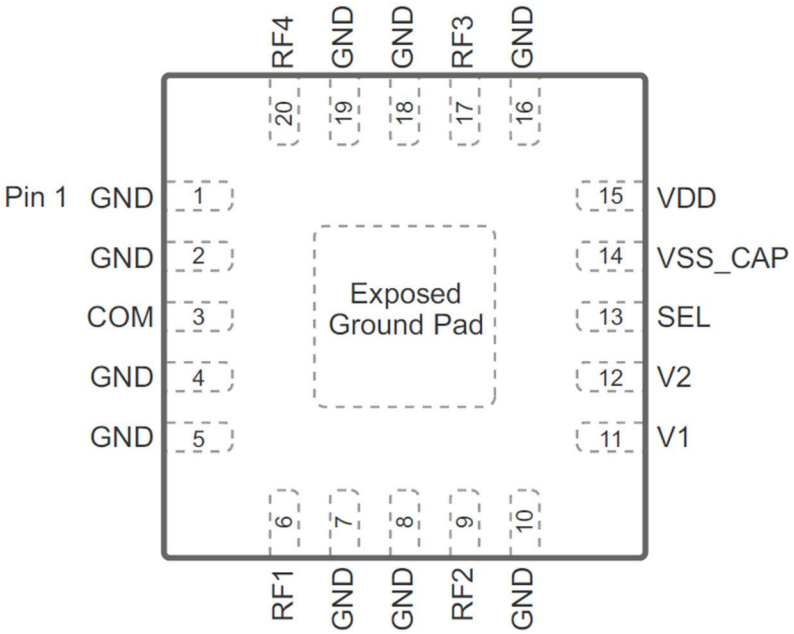

Figure 4. PE42448 Pin Configuration (Top View)

Table 3. PE42448 Pin Descriptions

Pin number	Pin name	Description
1,2,4,5,7,8,10,16,18,19	GND	Ground
3(1)	COM	RF common
6(1)	RF1	RF port 1
9(1)	RF2	RF port 2
11	V1	Digital control logic input 1
12	V2	Digital control logic input 2
13(2)	SEL	Logic select used to determine the definition for the V1 and V2 pins
14(3)	VSS_CAP	Bypass capacitor to V_{SS}
15	VDD	Supply voltage
17(1)	RF3	RF port 3
20(1)	RF4	RF port 4
PAD	GND	Exposed pad. Ground for proper operation.

Note:

1. RF pins 3, 6, 9, 17, and 20 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. An internal pull-up resistor sets SEL (pin 13) to logic high if the pin is floating. To set a logic low, ground pin 13.
3. Install a capacitor on VSS_CAP (pin 14) to GND. Do not apply DC to or ground this pin. Either leave the pin open or connect a supply 100 nF or above. The larger the capacitor value, the longer the circuit startup time.

EVK Connector Configuration

Table 4. Evaluation Board DC, Logic, and RF Signal Interface

Connector	Name	Description	Min VDC	Typ VDC	Max VDC	RF input power RMS (dBm)
J11-1	VDD	Supply voltage	4.5	5	5.5	–
J11-2, 4, 6, 8, 10, 12, 14	GND	GND	–	0	–	–
J11-3	VSS_CAP	Bypass capacitor for VSS	0	–	3.6	–
J11-5	SEL	Logic select	0	–	3.6	–
J11-7	V2	Digital control logic 2	0	–	3.6	–
J11-9	V1	Digital control logic 1	0	–	3.6	–
J11-11	–	NC	–	–	–	–
J11-13	–	NC	–	–	–	–
J1	RFC	RF common	–	–	–	+40
J2	RF1	RF port 1	–	–	–	+40
J3	RF2	RF port 2	–	–	–	+40
J4	RF3	RF port 3	–	–	–	+40
J5	RF4	RF port 4	–	–	–	+40
J6	–	Thru	–	–	–	–
J7	–	Thru	–	–	–	–

Absolute Maximum RF Ratings

Table 5. Absolute Maximum RF Ratings

Parameter	Min	Max	Unit
VDD positive supply voltage	-0.3	5.5	V
Digital input voltage	-0.3	3.6	V
Power HANDLING: 9W average power with the following conditions at the same time: Within operation temperature range. 20 MHz TD-TLE signal with 11 dB PAR, duty cycle 8.8 ms, 88%	–	9	W
No damage power handling requirement: Average power 42.5 dBm; peak power 50.5 dBm; keep 10 ms in one time; frequency one time/month, total 120 times in 10 years, lifetime.	–	+42.5	dBm
Storage temperature	-45	150	°C
Maximum junction temperature(*)	-65	150	°C
Note: * Maximum junction temperature ≤ 115 °C + (power dissipation of insertion loss-induced power) × thermal resistance.			

SP4T Control Logic

Table 6. PE42448 Truth Table

ON port	V2	V1	SEL
RF1	0	0	0
RF2	0	1	0
RF3	1	0	0
RF4	1	1	0
Transpose			
RF1	1	1	1 or no-connect
RF2	1	0	1 or no-connect
RF3	0	1	1 or no-connect
RF4	0	0	1 or no-connect

Hardware Operation

This section includes the general guidelines for operating the EVK. To configure the EVK and achieve optimal performance, follow these steps for the power-up sequence:

1. Before you power-up the EVK, verify that no RF signal is applied to the RFC and RFx connectors.
2. Set V_{DD} to 5V.
3. Set the V1, V2, and SEL logic for the preferred RF path, as listed in Table 6.
4. The device is safe to operate after 30 µs.
5. Terminate the unused RF ports with 50Ω loads.
6. Apply the preferred RF signal to the preferred path (RFC to RFx).
7. The maximum RF input is +40 dBm.

Technical Resources

For any technical inquiries regarding the evaluation kit, see the applications support at www.psemi.com (for the fastest response) or call +1-858-731-9400.

Trademarks are subject to trademark claims.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademarks

Corporate Headquarters

9369 Carroll Park Drive, San Diego, CA, 92121 USA
+1-858-731-9400