

PE566212

EVK User Manual

2.4 GHz SOI Front-end Module



Evaluation kit overview

The PE566212 is a high-performance, fully integrated front-end module (FEM) designed for Thread, Zigbee, and Bluetooth Low Energy. This highly versatile FEM features an integrated PA with up to +20 dBm output power, adjustable output power with a 22.5-dB range, and an integrated LNA (1.8 dB noise figure) with a low-loss bypass path.

This PE566212 evaluation kit (EVK) user guide includes information about the hardware required to control and evaluate the functionality of the 2.4 GHz SOI IoT front-end module.

Application support

For any technical inquiries regarding the evaluation kit or software, visit applications support at www.psemi.com (fastest response) or call +1-858-731-9400.

Evaluation kit contents and requirements

Kit contents

The PE566212 EVK includes the following hardware required to evaluate the 2.4 GHz SOI front-end IoT module.

Table 1. PE566212 evaluation kit contents

Quantity	Description
1	PE566212 2.4 GHz SOI front-end IoT module evaluation board assembly

Hardware requirements

To evaluate the performance of the evaluation board, use the following test equipment:

- Vector network analyzer (VNA)
- Vector signal generator (VSG)
- Signal/spectrum analyzer (SA)

Caution: The PE566212 2.4 GHz SOI front-end IoT module EVK contains components that could be damaged by exposure to voltages greater than the specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals and signal inputs and outputs.

Evaluation board overview

The evaluation board (EVB) is assembled with a PE566212 2.4 GHz SOI IoT front-end module, two headers, and two SMA connectors.

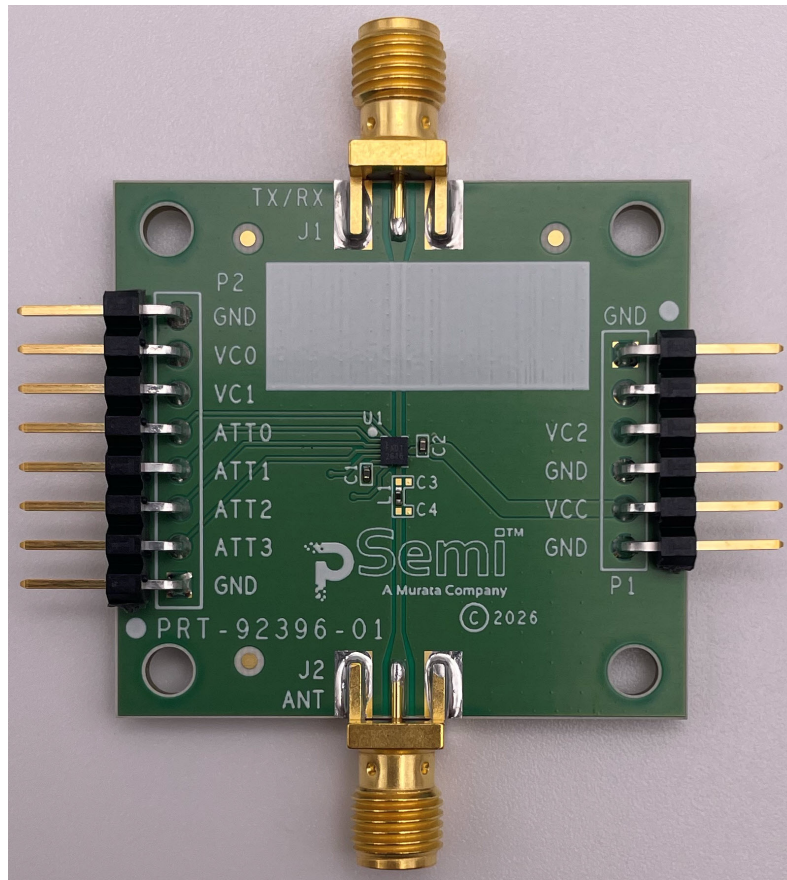


Figure 1. Evaluation board assembly

Evaluation board schematic and BOM

Figure 2 shows the evaluation board schematic, and Table 2 lists the evaluation board bill of materials.

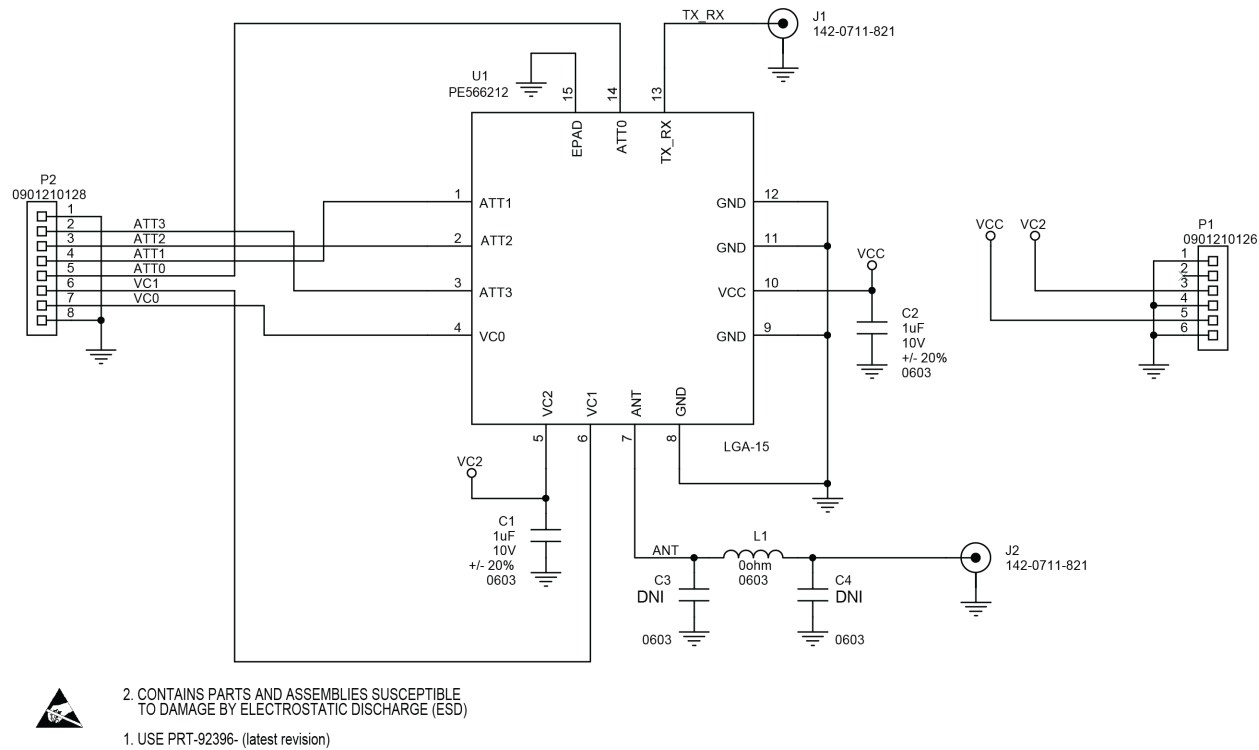


Figure 2. Evaluation board schematic

Table 2. Evaluation board bill of materials

Reference	Value	Description	Manufacturer	Mfr. part no.
C1, C2	1 μ F	CAP, SMD, CER, 1uF, 10V, $\pm$ 20%, X6S, 0201 (0603 Metric)	Murata Electronics	GRM033C81A105ME05D
C3, C4	DNI	–	–	–
J1, J2	142-0711-821	CONN, Coaxial Connectors (RF), SMA, SMD, Jack, Female Socket, 50 Ω	Cinch Connectivity Solutions Johnson	142-0711-821
L1	0 Ω	RES, SMD, Thick Film, 0, Jumper, 1/20W, 0201 (0603 Metric)	Panasonic Electronic Components	ERJ-1GN0R00C
PCB1	PCB	PCB, PE566212 EVB	pSemi Corporation	PRT-92396-01
P1	901210126	CONN, Rectangular Connectors - Headers, Male Pins, Header, Breakaway, TH-RA, Male Pin, C-Grid III 90121	Molex, Inc.	901210126
P2	901210128	CONN, Rectangular Connectors - Headers, Male Pins, Header, Breakaway, TH-RA, Male Pin, C-Grid III 90121	Molex, Inc.	901210128
U1	PE566212	IC, SMD, pSemi IC, LGA, 1.8mm x 1.8mm	pSemi Corporation	PE566212

Hardware configuration

pSemi designed the evaluation board (EVB) to ease your evaluation of the PE566212 2.4 GHz SOI IoT front-end module using varying test conditions and system integration.

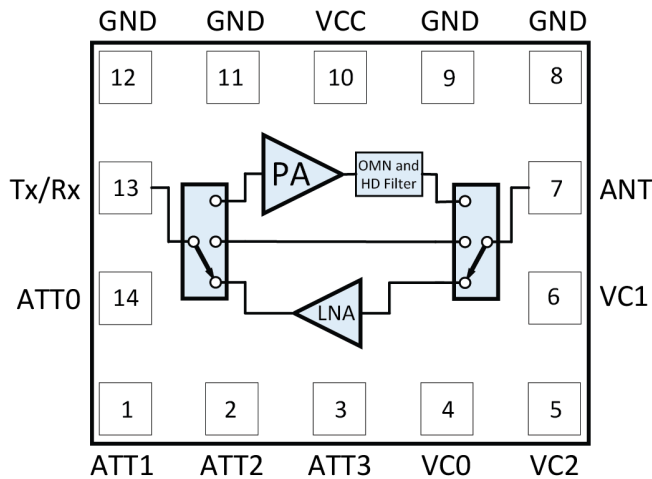


Figure 3. PE566212 block diagram

RF signals, DC power, and control signals are easily connected using J1, J2, P1, and P2 on the PCB assembly.

Pin configuration

Figure 4 shows the PE566212 pin configuration for the 14-lead $1.8 \times 1.8 \times 0.63$ mm LGA package, and Table 3 lists the description for each pin.

Table 3. Pin descriptions

Pin no.	Pin name	Description
1	ATT1	Gain control bit (3 dB)
2	ATT2	Gain control bit (6 dB)
3	ATT3	Gain control bit (12 dB)
4	VC0	Mode control pin 0
5	VC2	Mode control pin 2
6	VC1	Mode control pin 1
7	ANT	Antenna
8, 9, 11, 12	GND	Ground
10	VCC	Supply voltage
13	Tx/Rx	Transmit/receive
14	ATT0	Gain control bit (1.5 dB)

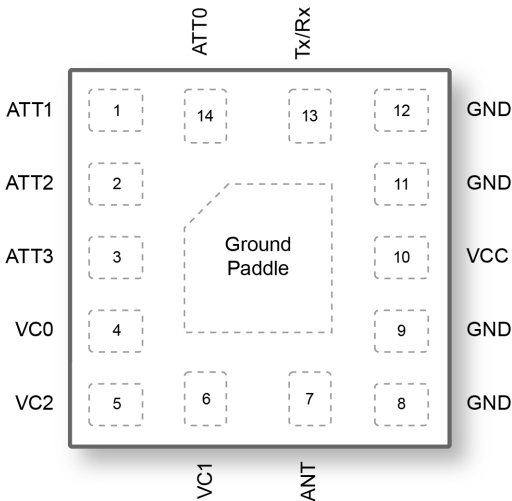


Figure 4. Pin configuration, top view

EVK connector configuration

Table 4. Evaluation board DC and logic interface

Connector	Name	Description	Min	Typ	Max	Unit
P2-1	GND	Ground	–	0	–	V
P2-2	ATT3	12-dB step	–	1.8	–	V
P2-3	ATT2	6-dB step	–	1.8	–	V
P2-4	ATT1	3-dB step	–	1.8	–	V
P2-5	ATT0	1.5-dB step	–	1.8	–	V
P2-6	VC1	Tx control	–	1.8	–	V
P2-7	VC0	Rx control	–	1.8	–	V
P2-8	GND	Ground	–	0	–	V
P1-1	GND	Ground	–	0	–	V
P1-2	NC	Not connected	–	–	–	–
P1-3	VC2	Supply voltage	–	1.8	–	V
P1-4	GND	Ground	–	0	–	V
P1-5	VCC	Supply voltage	1.7	3.3	3.6	V
P1-6	GND	Ground	–	0	–	V

Table 5. Absolute maximum RF ratings

Parameter	Symbol	Min	Max	Unit
Transmit input power at Tx/Rx port	P _{IN_Tx}	–	+5	dBm
Receive input power at ANT ports	P _{IN_Rx}	–	+15	dBm
Bypass input power at ANT ports	P _{IN_Bypass}	–	+20	dBm

Control logic

Table 6. Mode control logic

ATTN3/2/1/0	VC2	VC1	VC0	Bluetooth mode	Description
X	0	0	0	Bluetooth off	High isolation mode
X	1	0	1	Rx LNA	Rx LNA mode
X	1	0	0	Sleep	Sleep mode
See Table 7	1	1	0	Bluetooth Tx	Tx mode. Adjust the PA input attenuator based on the ATT GPIOs.
X	1	1	1	Bypass	Tx or Rx bypass mode

Table 7. Tx mode attenuation control logic

ATT3	ATT2	ATT1	ATT0	Attenuation
0	0	0	0	0
0	0	0	1	1.5
0	0	1	0	3
0	0	1	1	4.5
0	1	0	0	6
0	1	0	1	7.5
0	1	1	0	9
0	1	1	1	10.5
1	0	0	0	12
1	0	0	1	13.5
1	0	1	0	15
1	0	1	1	16.5
1	1	0	0	18
1	1	0	1	19.5
1	1	1	0	21
1	1	1	1	22.5

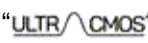
Hardware operation

This section lists the general guidelines for operating the hardware evaluation board. Follow these steps to configure the hardware for optimum performance.

Power-up sequence

1. Verify that no RF signals are applied to J1 and J2.
2. Set VC0, VC1, and ATT<X> to 0V.
3. Set VCC to 3.3V.
4. Set VC2 to 1.8V. The device is safe to operate after 30 μ S.
5. Set the GPIO signals for the target mode. See [Table 6](#).
6. Set the GPIO signals for the target attenuation. See [Table 7](#).
7. Apply the preferred RF signal to J1/J2:
 - a. Max RF input J2 (LNA mode): +15 dBm
 - b. Max RF Input J1 (Tx mode): +5 dBm
 - c. Max RF Input J1/J2 (bypass mode): +20 dBm

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